

MITSUBISHI 1965 SEMICONDUCTORS

BIPOLAR DIGITAL IC LSTTL



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MITSUBISHI SEMICONDUCTORS



BIPOLAR DIGITAL IC

HR BOX

MITSUBISHI ELECTRIC

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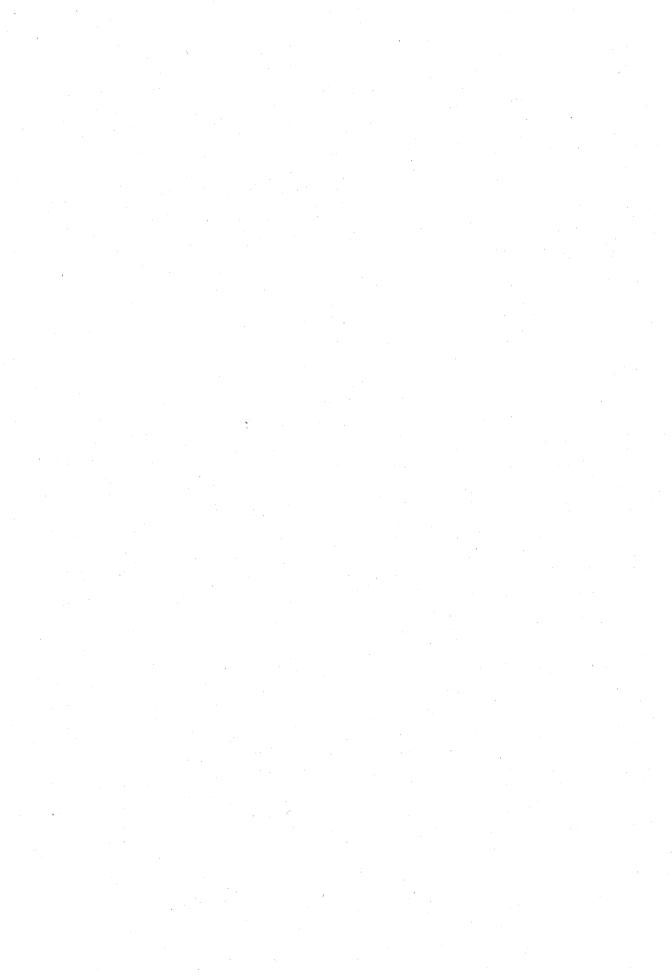
★: New product





GUIDANCE 1

TYPE DESIGNATION TABLE INDEX BY FUNCTION SYMBOLOGY PACKAGE OUTLINES



MITSUBISHI LSTTLs

TYPE DESIGNATION TABLE

TYPE DESIGNATION TABLE

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INDEX BY FUNCTION

INDEX BY FUNCTION (Recommended operating conditions $V_{CC} = 5V \pm 5\%$, $T_{opr} = -20 \sim +75^{\circ}C$)

INVERTERS, NAND GATES

	Type of	output		Турі	cal electric	al characte	eristics	Δ		
Circuit function	Active pull-up	Open collector	Туре	Propa- gation time (ns)	Power dissipa- tion (mW)	Low-level output current (mA)	High-level output current (mA)	Package Outlines	Interchangeable products	Page
lex Inverter	0	_	M74LS04P	6	12	8	0.4	14P4	74LS04	2-15
		0	M74LS05P	10	12	8	_	14P4	74LS05	2-17
Quadruple 2-Input Positive NAND Gate	0	_	M74LS00P	6	8 .	- 8	0.4	14P4	74LS00	2-9
	_	0.	M74LS03P	10	8	8		14P4	74LS03	2-13
Triple 3-Input Positive NAND Gate	.0		M74LS10P	8	6	8	0.4	14P4	74LS10	2-23
Triple 3-triput Positive NAND Gate	_	0	M74LS12P	13	6.3	.8	-	14P4	74LS12	2-27
Dual 4-Input Positive NAND Gate	0	. —	M74LS20P	10	4	8	0.4	14P4	74LS20	2-39
Dual 4-Input Positive NAND Gate		0	M74LS22P	18	4	8	_	14P4	74LS22	2-43
Single 8-Input Positive NAND Gate	0	_	M74LS30P	11	2.4	8	0.4	14P4	74LS30	2-49
Single 13-Input Positive NAND Gate	0	_	M74LS133P	11	2.4	8	0.4	16P4	74LS133	2-143

AND GATES

Quadruple 2-Input Positive AND Gate	0		M74LS08P	10	17	. 8	0.4	14P4	74LS08	2-19
Juadrupie 2-Input Positive AND Gate		10	M74LS09P	13	17	8		14P4	74L S09	2-21
Triple 3-Input Positive AND Gate	0	_	M74LS11P	10	12.8	8	0.4	14P4	74LS11	2-25
Triple 3-riput rositive AND date	_	0	M74LS15P	, 13	12.8	8	_	- 14P4 74LS09 2 4 14P4 74LS11 2 - 14P4 74LS15 2	2-33	
Dual 4-Input Positive AND Gate	0	_	M74LS21P	10	8.5	8	0.4	14P4	74LS21	2-41

NOR GATES

Quadruple 2-Input Positive NOR Gate	0	. —	M74 LS02P	6	10	8	0.4	14P4	74LS02	2-11
Triple 3-Input Positive NOR Gate	0		M74LS27P	6	13.5	8	0.4	14P4	74LS27	2-47

OR GATE

· · · · · · · · · · · · · · · · · · ·									
Quadruple 2-Input Positive OR Gate	0 -	M74LS32P	7	20	8 .	0.4	14P4	74LS32	2-51

EXCLUSIVE OR GATES

	0	_	M74LS86P	10	. 30 . 5	. 8	0.4	1.4P4	74LS86	2-90
Quadruple 2-Input Exclusive OR Gate		0	M74LS136P	13	30.5	8		14P4	74LS136	2-145
	0	_	M74LS386P	10	30.5	8	0.4	14P4	74LS386	2-366

EXCLUSIVE NOR GATE

Quadruple 2-Input Exclusive NOR Gate	_	0	M74LS266P	15	40	8	_	14P4	74LS266	2-302
										_ 000

AND-OR-INVERT GATE

Dual 2-Wide 2-Input AND-OR-INVERT Gate		_	M74LS51P	7	5.5	8	0.4	14P4	74LS51	2-69	
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BUFFERS/LINE DRIVERS

	Type	of out	put		Тур	ical elec	trical ch	naracteri				
Circuit function .	Active pull-up	Open collector	3-state	Type		Power dissipa- tion (mW)	output	High- level output current (mA)	C(V _{T+} -V _{T-})	Package Outlines	Interchangeable products	Page
			ı	M74LS240P	8	120	24	15	0.4	20P4	74LS240	2-256
· ·		_	Ν	M74LS241P	9	126.7	24	15	0.4	20P4	74LS241	2-259
Octal Buffer/Line Driver			Ζ	M74LS244P	9	126.7	24	15	0.4	20P4	74LS244	2-269
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		_	Ν	M74LS541P	10	133.3	24	15	0.4	20P4	74LS541	2-388
		_	Ν	M74LS245P	10	290	24	15	0.4	20P4	74LS245	2-272
		_	1	M74LS620P	10	290	24	15	0.4	20P4	74LS620	2-399
· · · · · · · · · · · · · · · · · · ·	_	_	1	M74LS640P	10	290	24	15	0.4	20P4	74LS640	2-402
		_	- 1	M74LS640-1P	10	290	48	15	0.4	20P4	74LS640-1	2-405
	_	Ν	_	M74LS641P	18	290	24	-	0.4	20P4	74LS641	2-408
		N	_	M74LS641-1P	18	290	48	_	0.4	20P4	74LS641-1	2-411
Octol Bus Transcouver	. —	I	_	M74LS642P	15	290	24		0.4	20P4	74LS642	2-414
Octal Bus Transceiver		1	_	M74LS642-1P	15	290	48	_	0.4	20P4	74LS642-1	2-417
·		_	١٠N	M74LS643P	10	290	24	15	0.4	20P4	74LS643 ·	2-420
		_	١٠N	M74LS643-1P	10	290	48	15	0.4	20P4	74LS643-1	2-423
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		_	1	M74LS368AP	7	59	24	2.6		16P4	74LS368A	2-350
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0 1 1 5 5 4		_	N	M74LS125AP	9	51.8	24	2.6	_	14P4	74LS125A	2-137
Quadruple Bus Buffer Gate		_	N	M74LS126AP	9	59	24	2.6	_	14P4	74LS126A	2-139
Out of the Desire		_	ī	M74LS242P	8	133.3	24	15	0.4	14P4	74LS242	2-263
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Dual 4-Input Positive NAND Buffer	ī	_	_	M74LS40P	14	8.6	24	1.2	_	14P4	74LS40	2-57

^{1:} With inverted output N: With noninverted output I•N: With both inverted and noninverted output

SCHMITT TRIGGER NAND GATES/INVERTERS

	Туре о	f output	,	Typica	al electr	ical chara	cteristics			
Circuit function	Active pull-up	Open collector	Type	Propaga- tion time (ns)	Power dissipa- tion (mW)	Positive- going threshold voltage (V)	Negative- going threshold voltage (V)	Package Outlines	Interchangeable products	Page
Hex Schmitt Trigger Inverter	I	_	M74LS14P	12	51.5	1.6	0.8	14P4	74LS14	2-31
	11	_	M74LS19P	13	67	1.9	1.0	14P4	74LŞ19	2-37
Quadruple 2-Input Positive NAND	1		M74LS132P	13	35.3	1,.6	0.8	14P4	74LS132	2-141
Schmitt Trigger	ı	_	M74LS24P	19	44	1.9	1.0	14P4	74LS24	2-45
Dual 4-Input Positive NAND Schmitt	1	_	M74LS13P	. 16	17.5	1.6	0.8	14P4	74LS13	2-29
Trigger	I	_	M74LS18P	25	22.5	1.9	1.0	14P4	74LS18	2-35

^{1:} With inverted output

J-K FLIP-FLOPS

		Typic	al electrica	al characte	eristics				0) 10		
Circuit function	Туре	Operating frequency (MHz)	time	Hold time (ns)	Power dissipation (mW)	Trigger	Preset	Reset	Package Outlines	Interchangeable products	Page
Dual J-K Negative Edge-Triggered Flip- Flop with Reset	M74LS73AP	0~45	. 20	0	20	Ł	_	IJ	14P4	74LS73A	2-71
Dual J-K Negative Edge-Triggered Flip- Flop with Set and Reset	M74LS76AP	0~45	20	0	20	Ł	T	T	16P4	74LS76A	2-80
Dual J-K Negative Edge-Triggered Flip- Flop with Reset	M74LS107AP	0~45	20	0	20	PL.	_	IJ	14P4	74LS107A	2-112
Dual J-K Positive Edge-Triggered Flip- Flop with Set and Reset	M74LS109AP	0~45	20	5	. 20	7	J	J	16P4	74LS109A	2-115
Dual J-K Negative Edge-Triggered Flip- Flop with Set and Reset	M74LS112AP	0 ~ 45	20	0	20	Z	T	U	16P4	74LS112A	2-118
Dual J-K Negative Edge-Triggered Flip- Flop with Set	M74L S 113AP	0 ~ 45	20	0	20	Ł	I	_	14P4	7-ILS113A	2-121
Dual J-K Negative Edge-Triggered Flip-Flop with Set Common Reset and Common Clock	M74LS114AP	0~45	20	0	20	Ł	IJ	U	14P4	74LS114A	2-124

✓: Positive-going edge ✓: Negative-going edge ✓: Active low-level

D-Type FLIP FLOPS

		Typic	al electrica	al characte	ristics						
		Operating	Setup	Hold	Power	ē			age	Interchangeable	_
Circuit function	Type	frequency	time	time	dissipa-	gg	rese	eset	- 중 ==	products	Page
		(MHz)	(ns)	(ns)	(mW)	Ē	ď	Re	Pa		
Dual D-Type Edge-Triggered Flip-Flop with Set and Reset	M74LS74AP	0~50	20	5	20	F	T	T	14P4	74LS74A	2-74
Hex D-Type Flip-Flop with Reset	M74LS174P	0~47	20	5	80	1	_	T	16P4	74LS174	2-214
Quadruple D-Type Elip-Flop with Reset	M74LS175P	0~50	20	5	55	1	-	75	16P4	74LS175	2-217
Octal Positive Edge-Triggered D-Type Flip- Flop with Reset	M74LS273P	0~40	20	5	85	7	-	T	20P4	74LS273	2-304
Octal Positive Edge-Triggered D-Type Flip- Flop with 3-State Outputs	M74LS374P	0~40	20	4	135	7	-	-	20P4	74LS374	2-356
Octal Positive Edge-Triggered D-Type Flip- Flop with Enable	M74LS377P	0~40	25	5	85	<u>_</u>	-	_	20P4	74LS377	2-363

√: Positive-going edge

 \coprod : Active low-level

LATCHES, REGISTERS

		Туріс	al electrica	al characte	ristics					
Circuit function	Type	Power dissipa- tion (ns)	Setup time (ns)	Hold time (ns)	Power dissipa- tion (mW)	Enable	Reset	Package Outlines	Interchangeable products	Page
4-Bit Bistable Latch	M74LS75P	9	20	8	31.5	Л	-	16P4	74LS75	2-77
4-bit bistable Latch	M74LS375P	9	20	8	31.5	Л	_	16P4	74LS375	2-360
Dual 4-Bit Addresable Latch	M74LS256P	13	15	5	100	-	U	1'6P4	74LS256	2-288
8-Bit Addressable Latch	M74LS259P	13	15	5	100	_	\mathbb{T}	16P4	74LS259	2-298
Quadruple R-S Latch	M74LS279P	10	_	_	19	-	-	16P4	74L S2 79	2-307
Octal D-Type Transparent Latch with 3-State Outputs	M74LS373P	12	5	20	120	Л	-	20P4	74LS373	2-353
4-Bit D-Type Register with 3-State Outputs	M74LS173AP	23	17	6	85	F	Л	16P4	74LS173A	2-210

☐: Active high-level

 \coprod : Active low-level

√: Positive-going edge

MITSUBISHI LSTTLs **INDEX BY FUNCTION**

SHIFT REGISTERS

			electrical teristics			M	ode				
Circuit function	Туре	Operating frequency	Power dissipation	set	shift	shift	el load	Hold (Do nothing)	ackage	Interchangeable products	Page
		(MHz)		Re	Right	Left s	Parallel	(Do n	P. O		
8-Bit Universal Shift/Storage Register	M74LS299P	0~28	165	Α	0	0	0	0	20P4	74LS299	2-328
8-Bit Offiversal Stiff(/Storage Register	M74LS323P	0~28	165	S	0	0	0	0	20P4	74LS323	2-332
4-Bit Bidirectional Universal Shift Register	M74LS194AP	0~45	75	Α	0	0	0	0	16P4	74LS194A	2-236
5-Bit Shift Register	M74LS96P	0~45	60	Α	0	-	0	-	16P4	74LS96	2-108
4-Bit Cascadable Shift Register with 3-State Outputs	M74LS395AP	0~40	83.8	Α	0	-	0	-	16P4	74LS395	2-374
4-Bit Parallel Access Shift Register	M74LS195AP	0~60	70	Α	0	-	0	-	16P4	74LS 195A	2-239
4-Bit Parallel Access Shift Register	M74LS95BP	0~50	65	_	0	-	0	_	14P4	74LS95B	2-105
4-Bit Shift Register with 3-State Outputs	M74LS295BP	0~40	72.5	_	9	_	0	_	14P4	74LS295B	2-322
8-Bit Serial-In Parallel-Out Shift Register	M74LS164P	0~50	80	Α	0	_	-	-/	14P4	74LS164	2-196
8-Bit Shift Register	M74LS91P	0~60	60	_	0	_	_	_	14P4	74LS91	2-95
8-Bit Parallel-Load Shift Register	M74LS165AP	0~38	105	_	0	_	_	<u> </u>	16P4	74LS165A	2-199
8-Bit Shift Register	M74LS166AP	0~38	100	Α	0	_	-	_	16P 4	74LS166A	2-203
8-Bit Shift Register/Latch with 3-State Output	M74LS595P			Α	0	_	-	0	16P4	74LS595	2-391
8-Bit Shift Register/Latch with Open Collector Output	M74LS596P			Α	0	_	-	0	16P4	74LS596	2-395

A: Asynchronous S: Synchronous

ASYNCHRONOUS COUNTERS

	lion		Typical e	electrical eristics	٠, _			ge		
Circuit function	Organization	Туре	Clock frequency (MHz)	Power dissipation (mW)	Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Decade Counter	2×5	M74LS90P	0~75 0~30	45	P	"9" set	Л	14P4	74LS90	2-92
Decade Counter	2×5	M74LS290P	0~75 0~30	45	7	"9" set	Л	14P4	74LS290	2-316
Presettable Decade Counter/Latch	2×5	M74LS196P	0~80 0~25	80	الح	Α	T	14P4	74LS196	2-242
A.B., B. Causas	2×8	M74LS93P	0~60 0~35	45	¥	_	Л	14P4	74LS93	2-101
4-Bit Binary Counter	2×8	M74LS293P	0~60 0~35	45	7	_	Л	14P4	74LS293	2-319
Presettable 4-Bit Binary Counter/Latch	2×8	M74LS197P	0~80 0~35	80	لح	Α	U	14P4	74LS197	2-246
Divide-by-Twelve Counter	2×6	M74LS92P	0~80 0~30	45	₽		JL	14P4	74LS92	2-98
Dual Decade Counter	2×5	M74LS390P	0~80 0~35	100	[-]	-	Л	16P4	74LS390	2-368
Dual 4-Bit Decade Counter	2×5	M74LS490P	0~35	75	¥	_	Л	16P4	74LS490	2-382
Dual 4-Bit Binary Counter	16	M74LS393P	0~75	100	7	_	T	14P4	74LS393	2-371

[:] Negative-going edge

A : Asynchronous

[&]quot;9" set: Output QA and QD can be set to high directly, and output QB and QC to low.

SYNCHRONOUS COUNTERS

Circuit function	Туре	Typical e charact Clock frequency (MHz)		Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Synchronous Presettable Decade Counter with Direct Reset	M74LS160AP	0~55	92.5	4	s	Α	16P4	74LS160A	2-180
Fully Synchronous Presettable Decade Counter	M74LS162AP	0~55	92.5	7	s	s	16P4	74LS162A	2-188
Synchronous Presettable Up/Down Decade Counter with Mode Control	M74LS190P	0~38	100	7	Α	_	16P4	74LS190	2-220
Synchronous Presettable Up/Down Decade Counter	M74LS192P	0~38	95	<u></u>	Α	Α	16P4	74LS192	2-228
Synchronous Presettable 4-Bit Binary Counter with Direct Reset	M74LS161AP	0~55	92.5	Ŧ	s	Α	16P4	74LS161A	2-184
Fully Synchronous Presettable 4-Bit Binary Counter	M74LS163AP	0~55	92.5	<u></u>	S	s	16P4	74LS163A	2-192
Synchronous Presettable Up/Down 4-Bit Binary Counter with Mode Control	M74LS191P	0~40	100	7	Α	_	16P4	74LS191	2-224
Synchronous Presettable Up/Down 4-Bit Binary Counter	M74LS193P	0~38	95	玉	Α	Α	16P4	74LS193	2-232
Synchronous Up/Down Decade Counter	M74LS668P	0~45	100	工	S	_	16P4	74LS668	2-438
Synchronous Up/Down 4-Bit Binary Counter	M74LS669P	0~30	100	丕	S	_	16P4	74LS669	2-444

A : Asynchronous

S : Synchronous

MONOSTABLE MULTIVIBRATORS

	,	Typic	al electr	rical characteristics	ge es		
Circuit function	Туре	Output pulse width		External timing resistor /capacitor for setting output pulse width	Package Outlines	Interchangeable products	Page
Retriggerable Monostable Multivibrator with Reset	M74LS122P	70ns~∞	30	5~260kΩ/No limit	14P4	74LS122	2-127
Dual Retriggerable Monostable Multivibrator with Reset	M74LS123P	70 ns~ ∞	60	5~260kΩ/No limit	16P4	74LS123	2-132
Dual Retriggerable Monostable Multivibrator with Reset	M74LS423P	70ns~∞	60	5~260k Ω/No limit	16P4	74LS423	2-377
Dual Monostable Multivibrator	M74LS221P	33ns~∞	62.5	1.4~100kΩ/0~1000μF	16P4	74LS221	2-250

DATA SELECTORS/MULTIPLEXERS

		Typical power	Typical prop	pagation t	ime (ns)	s de		
Circuit function	Туре	dissipa- tion (mW)	From strobe (enable) input to output	From data input to output	From data input to inverted output	Package Outlines	Interchangeable products	Page
8-Line to 1-Line Data Selector/Multiplexer with Strobe	M74LS151P	30	15	15	8	16P4	74LS151	2-165
8-Line to 1-Line Data Selector/Multiplexer with 3-State Output	M74LS251P	33	13	15	7	16P4	74LS251	2-281
Dual 4-Line to 1-Line Data Selector/ Multiplexer with Strobe	M74LS153P	31	12	10	_	16P4	74LS153	2-168
Dual 4-Line to 1-Line Data Selector/ Multiplexer with 3-State Output	M74LS253P	38.8	12	10		16P4	74LS253	2-285
Dual 4-Line to 1-Line Data Selector/ Multiplexer with Strobe(Inverted)	M74LS352P	31	11	_	7 .	16P4	74LS352	2-336
Dual 4-Line to 1-Line Data Selector/ Multiplexer with 3-State Output (Inverted)	M74LS353P	38.8	13		8	16P4	74LS353	2-338
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer	M74LS157P	48 .5	12	8	_	16P4	74LS157	2-176
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer (Inverted)	M74LS158P	24	8	_	5	16P4	74LS158	2-178
Quadruple 2-Line to 1-Line Data-Selector/ Multiplexer with 3-State Output	M74LS257AP	47	9	7	_	16P4	74LS257A	2-292
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer with 3-State Output (Inverted)	M74LS258AP	42.2	10		7	16P4	74LS258A	2-295
Quadruple 2-Input Multiplexer with Storage	M74LS298P	65	12 From clock input	_	. —	16P4	74LS298	2-325



DISPLAY DECODERS/DRIVERS

Circuit function	Output active level	Туре	Power	Low-level current output(mA)		Package Outlines	Interchangeable products	Page
BCD-to-Decimal Decoder/Driver	"L"	M74LS145P	35	24	15	16P4	74LS145	2-156
BCD-to-7-Segment Decoder/Driver	"L"	M74LS47P	35	24	15	16P4	74LS47	2-62
BCD-to-7- Segment Decoder/Driver	"H"	M74LS48P	125	6	Vcc	16P4	74LS48	2-66
BCD-to-7-Segment Decoder/Driver	"L"	M74LS247P	35	24	15	16P4	74LS247	2-275
BCD-to-7-Segment Decoder/Driver	"H"	M74LS248P	125	6	Vcc	16P4	74LS248	2-278

Segment Identification of M74LS47P, M74LS48P

Decimal number	0	1	2	3	. 4	5	6	7	8	. 9	10	11	12	13	14	15
Segment identification	0	1	2	3	T	S	Ь	<u></u>	8	٩	C	כ	Ü	_	T	

Segment Identification of M74LS247P, M74LS248P

Decimal number	0	1	2	3	4	5	6	7	8 .	9	10	11	12	13	14	15
Segment identification			\Box	3	Τ.	5	5		8	9	C	כ	U	_ _	F	

DECODERS DEMULTIPLEXERS

		Typical	Typical propag	ation time (ns)	യ്			
Circuit function	Туре	power dissipation (mW)	From strobe (enable) input to output	From data input to output	Package Outlines	Interchangeable products	Page	
BCD-to-Decimal Decoder	M74LS42P	35	_	12	16P4	74LS42	2-59	
3-Line to 8-Line Decoder/Demultiplexer with Address Latch	M74LS137P	. 55	10	12	16P4	74LS137	2-147	
3-Line to 8-Line Decoder/Demultiplexer	M74LS138P	31.5	12	14	16P4	74LS138	2-151	
Dual 2-Line to 4-Line Decoder/Demultiplexer	M74LS139P	34	10	13	16P4	74LS139	2-154	
Dual 2-Bit Binary to 4-Line Decoder/ Demultiplexer with Strobe	M74LS155P	30.5	16	13	16P4	74LS155	2-170	
Dual 2-Bit Binary to 4-Line Decoder/ Demultiplexer with Open Collector Outputs	M74LS156P	30.5	23	19	16P4	74LS156	2-173	

ENCODER

		Typic	Typical electrical characteristics					
Circuit function	Туре	Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Packag Outline	Interchangeable products	Page
10-Line to 4-Line Priority Encoder	M74LS147P	16	55	8	0.4	16P4	74LS147	2-159
8-Line to 3-Line Priority Encoder	M74LS148P	15	55	8	0.4	16P4	74LS148	2-162

MITSUBISHI LSTTLS INDEX BY FUNCTION

COMPARATOR

		Туріс	al electrica	al charact	eristics	a s			
Circuit function	Туре	Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Package Outlines	Interchangeable products	Page	
4-Bit Magnitude Comparator	M74LS85P	13	55	. 8	0.4	16P4	74LS85	2-86	
	M74LS682P	20	210	24	0.4	20P4	74LS682	2-452	
	M74LS683P	24	210	24	_	20P4	74LS683	2-456	
8-Bit Magnitude Comparator	M74LS684P	20	200	24	0.4	20P4	74LS684	2-459	
o-bit Wagiittude Comparatoi	M74LS685P	24	200	24	,	20P4	74LS685	2-462	
	M74LS688P	14	200	24	0.4	20P4	74LS688	2-465	
	M74LS689P	22	. 200	24	. —	20P4	74LS689	2-468	

PARITY GENERATOR/CHECKER

9-Bit Odd/Even parity Generator/Checker	M74LS280P	18	80	8	0.4	14P4	74LS280	2-310	ı

ADDER

		Typical	Typical propag	Typical propagation time (ns)		Interchangeable		
Circuit function	Туре	dissipation (mW)	Carry time	Add time	Package Outlines	products	Page	
4-Bit Binary Full Adder with Fast Carry	M74LS83AP	102.5	8	12	16P4	74LS83A	2-83	
4-Bit Binary Full Adder with Fast Carry	M74LS283P	102.5	8	12	16P4	74LS283	2-313	

REGISTER FILES

Circuit function	Tuno	Typical power	Typical propag	gation time (ns)	Package Outlines	Interchangeable	Page	
Circuit function	Type	dissipation (mW)	Write time	Write time Read time		products	age	
4-By-4 Register File with Open Collector Outputs	M74LS170P	125	15	16	16P4	74LS170	2-207	
4-By-4 Register File with 3-State Output	M74LS670P	150	12	13	16P4	74LS670	2-449	
4-Bit D-Type Register with 3-State Output	M74LS173AP	85			16P4	74LS173A	2-210	

Refer to LATCH and REGISTER sections for M74LS173AP specifications.

MITSUBISHI LSTTLS SYMBOLOGY

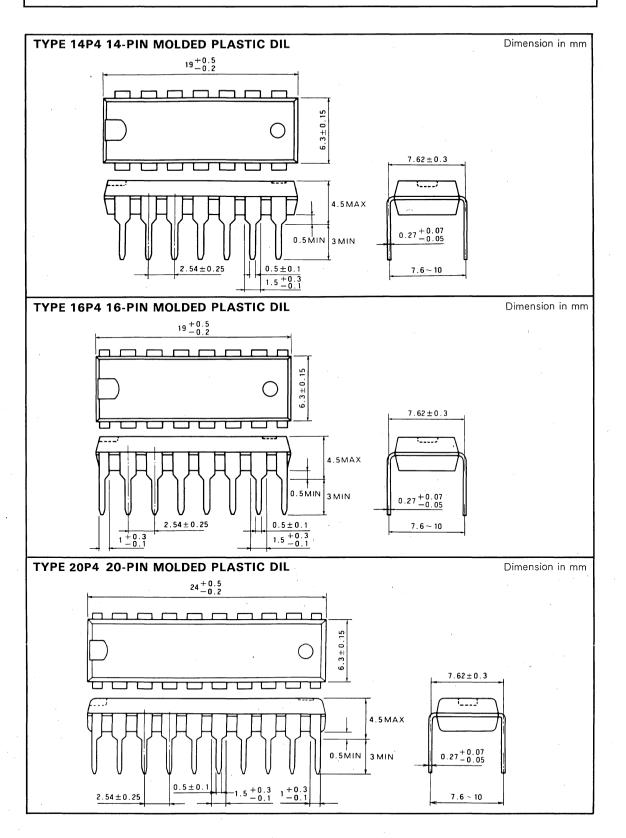
SYMBOLOGY

Symbol		Descriptions
CL	Load capacitance	Extenally connected load capacitance
f _{max}	Maximum clock frequency	Maximum input repetition frequency for normal IC operation.
Fı	Fan-in	Number of similar inputs
Fo	Fan-out	Number of similar ICs which can be driven by an output
н	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level
1	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative
Icc	Supply current	The current flowing into the V _{CC} supply terminal of a circuit
ICCL	Low-level supply current	V _{CC} current when the inputs are such that the output is low.
I _{CCH}	High-level supply current	V _{CC} current when the inputs are such that the output is high.
I _{CCZ}	High-impedance supply current	V _{CC} current when the inputs are such that the output is in the high-impedance state.
l _F	Forward current	Forward diode current
11	Input current	Input current flowing into the IC pin when a voltage is applied.
LiH	High-level input current	The current flowing into an input when a specified high voltage is applied.
I _{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied.
Гон	High-level output current	Current flowing in the load when the output is high or current flowing when a high level is applied
IoL	Low-level output current	The current flowing into an output which is in the low state
los	Short-circuit output current	The current flowing out of an output which is in the high state when that output is short circuit to groun
IozH -	Off-state high-level output current	The current flowing into a disabled 3-state output with a specified high output voltage applied
lozL	Off-state low-level output current	The current flowing out of a disabled 3-state output with a specified low output voltage applied
IT	Threshold current	Current which flows when the threshold voltage is applied to the input
l _{T+}	Positive threshold current	Current which flows when the positive threshold voltage is applied to the input
I _T =	Negative threshold current	Current which flows when the negative threshold voltage is applied to the input
L	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level
0	Indicates output	
Pd .	Power dissipation	Product of the supply voltage and the supply current
PRR	Pulse repetition rate	The rate of repetition of an applied pulse train
Ta	Operating free-air temperature	The temperature of the environment surrounding an IC
t _f .	Falltime	Time required to fall from the high to the low logic level
t _h	Hold time	The required hold time for a specified input after an input has changed
tlatch	Latch time	The time from the latching action of input data until the data appears in the output
Topr	Operating temperature	The ambient temperature range for normal IC operation
tpd	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output,
		expressed as the average propagation time.
t _{PHL}	Propagation delay time, high-to-low-level output	Amount of time required from a change of input signal until the output changes from high to low.
t _{PHZ}	Output disable time from High level	Amount of time required from a change of input signal until the output changes from high to
		high-impedance.
t _{PLH}	Propagation delay time, low-to-high-level output	Amount of time required from a change of input signal until the output changes from low to high.
t _{PLZ}	Output disable time from Low level	Amount of time required from a change of input signal until the output changes from low to high-impedance.
tw	Pulse width	The time required for a pulse to change from one specified level to another.
t _{wo}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator
t _{PZH}	Output enable time to a High level	Amount of time required from a change of input signal until the output changes from high-impedance to high.
t _{PZL}	Output enable time to a Low level	Amount of time required from a change of input signal until the output changes from high-impedance to low.
tr	Risetime	Time required to rise from the low to the high logic level
trec	Recovery time	Time from the point at which the input states are cancelled until the next clock pulse may be applied.
Tstg	Storage temperature	The range of surrounding storage temperature for an IC.
t _{SU}	Setup time	The required hold time for other inputs before a particular input may be changed.
Vcc	Supply voltage	The voltage of power supply voltage over which the device is guaranteed to operate within the
-00		specified limits.



Symbol.		Descriptions
V _{BE}	Base-emitter voltage	
VF	Forward voltage	Forward voltage applied to a diode
VI	Input voltage	Voltage applied to an input
Vic	Input clamp diode voltage	The forward voltage applied to an input clamping diode.
VIE	Input emitter-emitter voltage	The emitter-to-emitter voltage for a multi-emitter transistor input.
VIH	High-level input voltage	The range of input voltages that represents a logic high in the system.
VIL	Low-level input voltage	The range of input voltages that represents a logic low in the system.
V _O	Output voltage	Voltage applied to or appearing at an output
VoH	High-level output voltage	Voltage at an output in the high state
VoL	Low-level output voltage	Voltage at an output in the low state
√P	Pulse amplitude	The difference between the low level and high level of a pulse.
Vт	Threshold voltage	The input voltage beyond at which the output changes
V _{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to hig
V _T _	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from high to lo
Z	Indicates the off-state	Indicates that the output is in the high-impedance state.
Zo	Output impedance	The load impedance which should be connected to such devices as pulse generators.

MITSUBISHI LSTTLS PACKAGE OUTLINES





2

DATA SHEETS

SCHEMATICS OF INPUTS AND OUTPUTS INDIVIDUAL DATA









Schematics of inputs and outputs of the M74LS00P series are shown in I-1 \sim I-11 and in 0-1 \sim 0-17, respectively, for devices whose circuit diagrams are not given in the individ-

ual data. Reference should be made when circuitry is being designed.

SCHEMATICS OF INPUTS AND OUTPUTS

T		Schematics of inpu	ts		Schematics of outputs				
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent	resistance) Ω			
M74LS42P	I -1	17k	All inputs .	0-1	120				
	I -1	25k	DA~DD						
M74LS47P	I -1	20 k	LT, RBI	0-2	_				
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20 k	BI/RBO			
	I -1	25k	DA~DD						
M74LS48P	I -1	20 k	LT, RBI	0-3	2k				
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20 k	BI/RBO			
	I -1	26k	J, K						
M74LS73AP	I -1	9k	Ŧ	0-14	120				
	I -3	9k	RD	1					
	I -3	8k	SD, RD		/				
M74LS74AP	I -4	18k	Т	0-14	120				
	I -5	31k	D	1	,				
N741 0750	I -1	18k	D	0.15	120				
M74LS75P	I -1	4.5k	E	0-15	120				
	I -1	26k	J, K						
M74LS76AP	I -1	9 k	Ŧ	0-14	120				
	I -3	9 k	SD, RD	1					
	I -1	18k	C ₀	0-1	100				
M74LS83AP	I -1	9 k	A ₁ ~A ₄ , B ₁ ~B ₄	0-1	120				
	I -6	17k	I _{A<b< sub="">, I_{A>B}</b<>}		,				
M74LS85P	I -7	R ₁ =15k, R ₂ =8.5k	I _{A=B}	0-1	120				
	I -7	R ₁ =8.5k, R ₂ =17k	A ₀ ~A ₃ , B ₀ ~B ₃						
	I -1	17k	S _{D(9)1} , S _{D(9)2} , R _{D1} , R _{D2}	0-13	R=120, R ₁ =17k	0-			
M74LS90P	I -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8.5k	T ₁	0-13	R ₂ =17k, R ₃ =9k	Qв			
	1 -8	R ₁ =5.8k, R ₂ =5.8k, R ₃ =4.4k	T ₂	0-15	120	QA, QC, QD			
M741 6010	I -1	26k	D _{S1} , D _{S2}	0-15	120				
M74LS91P	I -1	19k [°]	Т	0-13					
	I -1	17k	R _{D1} , R _{D2}	0-13	R=120, R ₁ =17k	Qc			
M74LS92P	1 -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8.5k	T ₁	0.13	R ₂ =17k, R ₃ =9k	40			
	I -8	R ₁ =5.8k, R ₂ =5.8k, R ₃ =4.4k	T ₂	0-15	120	QA, QB, QD			
	I -1	17k .	R _{D1} , R _{D2}	0-15	120	Q _A , Q _D			
	I -8	R ₁ =8.5k, R ₂ =8.5k	T 1		R=120, R ₁ =17k	Qв			
M74LS93P		R ₃ =8.5k	'1	0-13	R ₂ =17k, R ₃ =9k	4 D			
	I -8	R ₁ =13k, R ₂ =13k	T ₂	0-13	R=120, R ₁ =10k	Qc			
	1 -0	R ₃ =9k		}	R ₂ =10k, R ₃ =9k	¥0			
	I -1	17k	T _R , T _L						
M74LS95BP	I -1	9 k	M/C	0-15	120				
	I -1	20 k	D _S , D ₀ ~D ₃						

Note: All resistances given are typical values.



Type designation		Sche	matics of inputs		Schematics of outputs
, ypo dosignation	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω
	I -1	26k	D _S		
M74LS96P	I -1	18k	R _D , T, S _{D0} ~S _{D4}	0-15	120
	I -1	3.4k	LOAD		
	I -1	26k	J, K		
M74LS107AP	I -1	9 k	Ŧ	0-14	120
	I -3	9 k	RD		
-	I -3	8 k	S _D , R _D		
M74LS109AP	I -4	18k	Т	0-14	120
	I -5	31k	J, K		
	I -1	24k	J, K		
M74LS112AP	I -1	9 k	Ŧ	0-14	120 -
	I -3	9 k	$\overline{S_D}, \overline{R_D}$		
	I -1	24k	J, K		
M74LS113AP	I -1	9 k		0-14	120
	I -3	9 k	S _D		
	I -1	24k	J, K		:
	I -1	4.8k	T		
M74LS114AP	I -3 /	9 k	SD	0-14	120
	I -3	4.5k	RD		* * * * *
M74LS122P	I -1	17k	All inputs	0-1	120
M74LS123P	I -1	17k	All inputs	0-1	120
1417 4 2 3 1 2 0 1	I-9	15k	D ₀ ~D ₃		120
M74LS137P	I - 1	20k	E ₁ , E ₂ , E _L	0-5	120
	1-9	10k	D ₀ ~D ₃	0-5	120
M74LS138P	I -1	20k	$E_1, \overline{E_2}, \overline{E_3}$	0-5	120
M74LS139P	I -1	17k	All inputs	0-1	120
M74LS145P	I -1	17k	All inputs	0-6	-
M74LS147P	I -1	17k	All inputs	0-5	120
	I -1	17k	□, Ē		:
M74LS148P	I -1	9 k	$\overline{D_1} \sim \overline{D_7}$	0-5	120
M74LS151P	I -1	17k	All inputs	0-1	120
M74LS153P	I -1	17k	All inputs	0-1	120
M74LS155P	I -1	17k	All inputs	0-1	120
M74LS156P	I -1	17k	All inputs	0-7	_
	I -1	17k	1D ₀ ~4D ₀ , 1D ₁ ~4D ₁		
M74LS157P	I -1	8.5k	S _A , G	0-1	120
	I -1	17k	1D ₀ ~4D ₀ , 1D ₁ ~4D ₁		
M74LS158P	I -1	8.5k	S _A , \overline{G}	0-1	120
	I -1	20 k	$D_A \sim D_D$, T, E _P , $\overline{R_D}$		
M74LS160AP	I -1.	9 k	E _T , LOAD	0-15	120
	I -1	20k	$D_A \sim D_D$, T, E _P , $\overline{R_D}$		-
M74LS161AP	I -1	9 k	E _T , LOAD	0-15	120
	I -1	20k	D _A ~D _D , T, E _P		
M74LS162AP			E _T , R, LOAD	0-15	120
	I -1	9 k			
M74LS163AP	I -1	20 k	DA~DD, T, EP	0-15	120
	I -1	9 k	E _T , R, LOAD	. 1	1



Tuno desi		Schematics of in	puts		Schematics of outputs
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω
M74LS164P	I -1	20 k	All inputs	0-15	120
	I -9	9 k	T, TINH, LOAD		
M74LS165AP	I -1	18k	D ₀ ~D ₇	0-8	120
	I -1	22k	D _S	7	
	I -9	9 k	RD, LOAD, T, TINH		
	I -1	18k	D ₀ ~D ₇	0-8	120
M74LS166AP	I -9	12k	LOAD		400
	I -1	22k	Ds	0-8	120
	I -1	8.5k	E _R , E _W		
M74LS170P	I -1	17k	D ₀ ~D ₃ , R _A , R _B , W _A , W _B	0-2	
M74LS173AP	I -1	19k	All inputs	0-9	100
	I -1	17k	T, RD	T	
M74LS174P	I -1	30 k	D ₀ ~D ₅	0-15	120
	I -1	17k	T, RD	T	
M74LS175P	I -1	30 k	D ₀ ~D ₃	0-15	120
	I -1	5.7k	Ē	2.15	100
M74LS190P	I -1	17k	All inputs except E	0-15	120
	I -1	5.7k	Ē	0.45	100
M74LS191P	I -1	17k	All inputs except E	0-15	120
1474L C100D	I -1	23 k	D _A ~D _D	0.15	100
M74LS192P	I -1	17k	T _U , T _D , R _D , LOAD	0-15	. 120
M741 C100D	I -1	23 k	D _A ~D _D	0-15	120
M74LS193P	I -1	17k	T _U , T _D , R _D , LOAD	0-13	120
M74LS194AP	I -1	25k	D _{SR} , D _{SL} , D ₀ ~D ₃	0-15	120
	I -1	17k	T, RD, M/C1, M/C2	0.13	
M74LS195AP	I -1	20 k	J, K, D ₀ ~D ₃ , M/C	0-15	120
	I -1	17k	T, R _D		120
	I -1	17k	D _A ∼D _D , LOAD	_	
M74LS196P	I -1	8.5k	R _D	0-15	120
	I -8	$R_1 = 5.7k, R_2 = 6.5k, R_3 = 7k$	T ₁		120
	I -8	R ₁ =5.7k, R ₂ =5.7k, R ₃ =5.7k	T ₂		
	I -1	17k	DA~DD, LOAD		
M74LS197P	I -1	8.5k	R _D	0-15	120
	I -8	R ₁ =5.7k, R ₂ =6.5k, R ₃ =7k	<u>T</u> 1		
	I -8	R ₁ =14k, R ₂ =13k, R ₃ =13k	T ₂		
	I -1·	24k	Ā	1	
	I -11	$R_1 = 45k, R_2 = 24k, R_3 = 9.5k$	В		
M74LS221P		R ₄ =14k, R ₅ =1.7k		0-1	120
	I -10	R ₁ =12k, R ₂ =9.5k	R _D		
-	·	R ₃ =14k, R ₄ =1.7k			
	I -1	25k	D _A ~D _D	0-2	_
M74LS247P	I -1	20 k	LT, RBI	ļ	
	I -2	R _{IN} =10k	BI/RBO ,	I-2	R _{OUT} =20k BI/RBO
	I -1	25 k	D _A ~D _D	0-3	2k
M74LS248P	I -1	20 k	LT, RBI		
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20 k BI/RBO



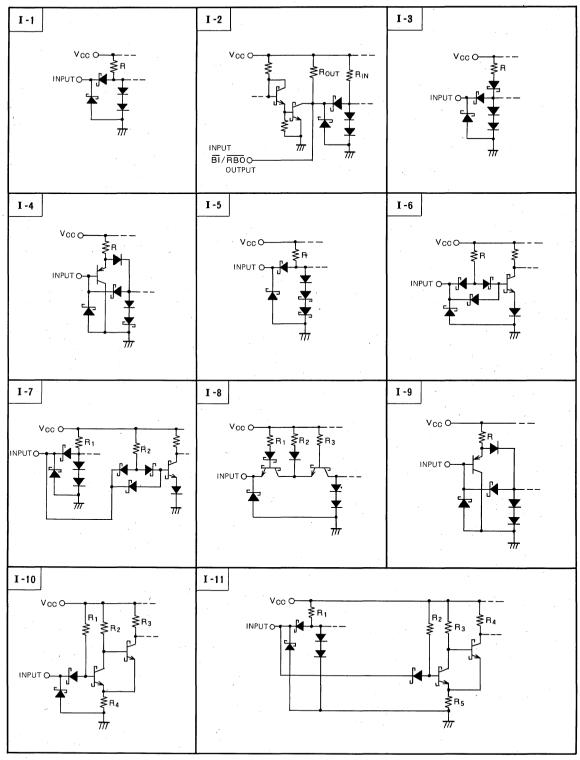
		Schematics of in	nputs		Schematics of ou	tputs	
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent	resistance) Ω	
M74LS251P	I -1	17k	All inputs	0-11	100		
	I -1	19k	S _A , S _B , 100, 200	0-4	100		
M74LS253P	I -1	17k	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃	0-12	100		
	I -1	17k	SA, SB, 1D, 2D, R	0.10			
M74LS256P	I -9	9.5k	M/C	0-16	120		
M74LS257AP	I -1	8.5k	SA	0-9	100		
W174L3237AF	I -1	17k	OC, 1D ₀ ~4D ₀ , 1D ₁ ~4D ₁		100	, , , , , , , , , , , , , , , , , , ,	
M74LS258AP	I -1	8.5k	SA	0-9	100		
WITTESZUGAF	I -1	17k	\overline{OC} , $1D_0 \sim 4D_0$, $1D_1 \sim 4D_1$		100		
M74LS259P	I -1	17k	S _A ∼S _C , D, R	0-16	120		
	I -9	9.5k	M/C		120		
M74LS273P	I -1	17k	T, RD	0-15	120	•	
	I -5	28k	1D~8D	0 10	120		
M74LS280P	I -1	20 k	All inputs	0-1	120		
M74LS283P	I -1	18k	Со	0-1 120			
	I -1	9 k	A ₁ ~A ₄ , B ₁ ~B ₄		120		
	I -1	17k	S _{D(9)1} , S _{D(9)2} R _{D1} , R _{D2}	0-13	$R = 120, R_1 = 17k$	Qв	
M74LS290P	I -8	$R_1 = 8.5 k, R_2 = 8.5 k, R_3 = 8.5 k$	· T ₁		R ₂ =17k, R ₃ =9k		
	I -8	$R_1 = 5.8 k$, $R_2 = 5.8 k$, $R_3 = 4.4 k$	T ₂	0-15	120	QA, QC, QD	
	I -1	17k	R _{D1} , R _{D2}	0-15	120	QA, QD	
	I -8	R ₁ =8.5k, R ₂ =8.5k	T 1		$R = 120, R_1 = 17k$	Qв	
M74LS293P	R ₃ =8.5k		0-13	$R_2 = 17k, R_3 = 9k$,		
	I -8	$R_1 = 13k, R_2 = 13k$	T ₂		R=120, R ₁ =10k	· Qc	
		R ₃ =9k			R ₂ =10k, R ₃ =9k		
,	I -1	18k	下	_	100		
M74LS295BP	I -1	20 k	0C, M/C	0-9			
	. I -5	30k	D _S	-			
	I -5	20k	D ₀ ~D ₃				
M74LS298P	I -1	17k	· ·	0-15	120		
×	I -1	20k	S _A , 1D ₀ ~4D ₀ , 1D ₁ ~4D ₁	 			
	I -1	10k	M/C ₁ , M/C ₂	0-9	100	Q ₀ ~Q ₇	
M74LS299P	I -1	20k	OC ₁ , OC ₂ , R _D , T	-			
	I -5	20 k	D _{SR} , D _{SL} , D ₀ ~D ₇	0-1	120	Q' ₀ , Q' ₇	
	I -1	10k	M/C ₁ , M/C ₂	0-9	100	Q ₀ ~Q ₇	
M74LS323P	I -1	20 k	$\overline{OC_1}$, $\overline{OC_2}$, $\overline{R_D}$, T	-	100	0/ 0/	
	I -5	20k	D _{SR} , D _{SL} , D ₀ ~D ₇	0-1	120	Q'0, Q'7	
M74LS352P	I -1	19k	S _A , S _B , 1 G , 2 G	0-1	120		
	I -1	17k	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃	-			
M74LS353P	I -1	19k	S _A , S _B , 100, 200	0-12	100		
	I -1	178	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃	-			
M74LS373P	I -1	17k	1D~8D	0-9	100	•	
·	I -9	9 k	E, 00	-			
M74LS374P	I -1	30k	1D~8D	0-9	100		
	I -9	9 k	T, OC	·			



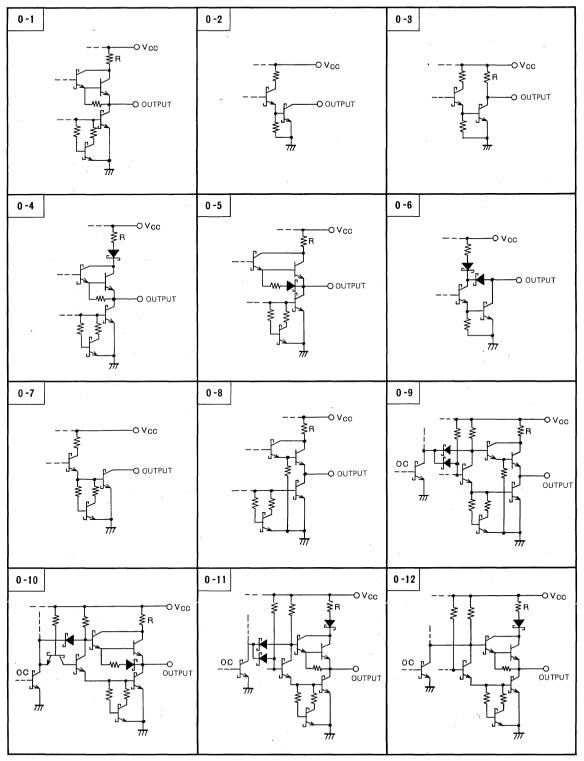
		Schematics of inc	outs	T	Schematics of o	utputs	
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalen	t resistance) Ω	
	I -1	18k	1D~4D	0.45	100		
M74LS375P	I -1	4.5k	1-2E, 3-4E	0-15	120		
	I -1	17k	т, Е	0.45	100		
M74LS377P	I -5	28k	1D~8D	0-15	120		
	I -1	17k	R _D				
M74∟S390	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	T ₁	0-17	120		
	I -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8k	T ₂	7			
14741 00000	I -1	17k	R _D	0.17	100		
M74LS393P	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	Ŧ	0-17	120	,	
	I -1	18k	Ŧ				
	I -1	20k	OC, M/C, RD	0-9	100	Q ₀ -Q ₃	
M74LS395AP	I -5	30 k	Ds				
	I -5	20k	D ₀ ~D ₃	0-17	, 120	Q'3	
M74LS423P	I -1	17k	All inputs	0-1	120		
	I -1	17k	S _{D(9)} , R _D	0-17	120		
M74LS490P	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	T	U-17	120		
M74LS595P	I - 1	19k	Ds	0-9	Q0~Q7		
W174C3393P	I - 9	13k	その他	0-8	Qı'		
M74LS596P	I - 1	19k	Ds	0-2	Q0~Q7	•	
1VI74LS390P	I - 9	13k	その他	0-8	Q7′		
	I -1	8.5k	LOAD	0-15	120	QA,QB Qc,QD	
M74LS668P	I -1	17k	U/D, T, EP, ET] 0-15	120	QA,QB QC,QD	
	I -5	20 k	D _A ~D _D	0-1	120	RCO	
	I -1	8.5k	LOAD	0-15	120	QA,QB,Qc,QD	
M74LS669P	I -1	17k	U/\overline{D} , T , $\overline{E_P}$, $\overline{E_T}$	0-13	120	VA, VB, VC, VD	
	I -5	20 k	D _A ~D _D	0-1	120	RCO	
	I -1	8.5k	Ew ,				
M74LS670P	I -7	R ₁ =8.5k, R ₂ =17k	ōc	0-10	120		
	I -1	17k	R _A , R _B , W _A , W _B , D ₀ ~D ₃				
M74LS682P	I - 9	14k	P0~P7	0-5	100		
100021	I - 12	R ₁ =14k, R ₂ =24k	Q0~Q7	J	100		
M74LS683P	I - 9	14k	P ₀ ~P ₇	0-7			
123000	I - 12	R ₁ = 14k, R ₂ =24k	Qo~Q7	J - ,			
M74LS684P	I -9	14k	全入力	0-5	100		
M74LS685P	I - 9	14k	全入力	0-7	_		
M74LS688P	I -9	14k	全入力	0-5	100		
M74LS689P	I - 9	14k	全入力	0-7			

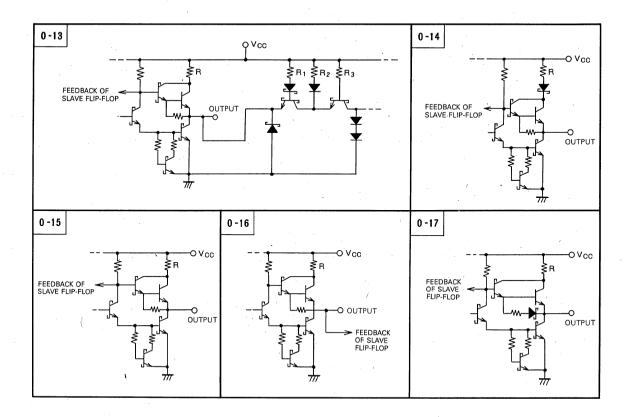


Schematics of inputs



Schematics of outputs





QUADRUPLE 2-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS00P is semiconductor integrated circuit containing four dual-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 8mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATIONS

General purpose, for use in industrial and consumer equipment.

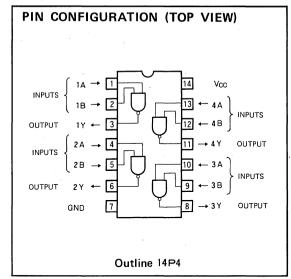
FUNCTIONAL DESCRIPTION

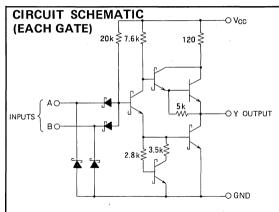
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, and low power consumption as well as high fan-out.

When both A and B inputs are high the output Y is low. When either A or B input is low the output Y is high.

FUNCTION TABLE

Α	В	Y
L	L	Ι
Н	L	Н
L	Н	Н
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply_voltage		-0.5~+7	V
Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter			Limits			
	Parame	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА	
	Low-level output current $ V_{OL} \leq 0.4V $ $V_{OL} \leq 0.5V $		0		4	mA	
lor		0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

	D	Test conditions	Limits			Unit
Symbol	Parameter	lest conditions	Min	Тур*	Max	Onit
ViH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_{I} = 0.8V$, $I_{OH} = -400 \mu A$	2.7	3.4		V
.,	Levilend and advisoring	V _{CC} =4.75V I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V		0.35	0.5	V
	High-level input current	$V_{CC} = 5.25V, V_{I} = 2.7V$			20	μА
Ιιн		$V_{CC} = 5.25V, V_{I} = 10V$			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	$V_{CC} = 5.25V, V_{C} = 0V$	- 20		- 100	mA
I _{CCH}	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		0.8	1.6	mA
I _{CCL}	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5V	-	2.4	4.4	mA

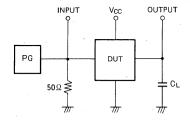
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta =25°C, unless otherwise noted)

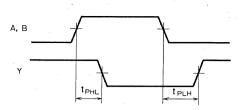
Symbol	Parameter	Test conditions		Limits			Unit
Symbol	i arameter	•.	rest conditions	Min	Тур	Max	Offic
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF			. 6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)			6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



QUADRUPLE 2-INPUT POSITIVE NOR GATES

DESCRIPTION

The M74LS02P is a semiconductor integrated circuit containing 4 dual-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 10mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

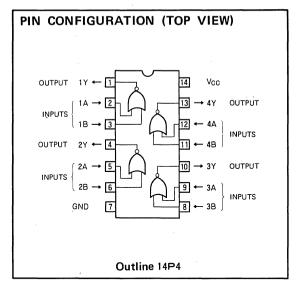
FUNCTIONAL DESCRIPTION

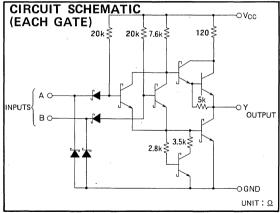
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When at least input A or input B is high, output Y is low, and when both A and B are low, Y is high.

FUNCTION TABLE

Α	В	Y
L	L	Н
Н	L	L
L	н	L
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NOR GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Į.			
			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	.0		4	mA
IoL Low-lev	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

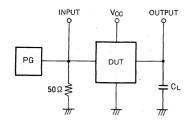
	0	- .	p.r.	Limits			Unit
Symbol	Parameter	lest	conditions	Min	Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA			-1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V ₁ =0.8V, I _{OH} =-400μA		2.7	3.4		٧
	1 1 1 1 1	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 2V$ $I_{0L} = 8mA$	I _{OL} = 8mA		0.35	0.5	V
	High level input ourrors	V _{CC} =5.25V, V _I =	2.7V			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	=0V	- 20		-100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			1.6	3.2	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		2.8	5.4	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

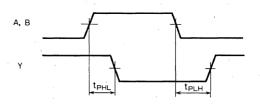
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Syllibol	symbol Parameter Test conditions		Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level output propagation time	C _L = 15pF		6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS03P is a semiconductor integrated circuit containing four dual-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in AND-Tie connection
- High breakdown input voltage $(V_1 \ge 15V)$
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (Pd = 8mW typical)
- High speed (tpd = 10ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

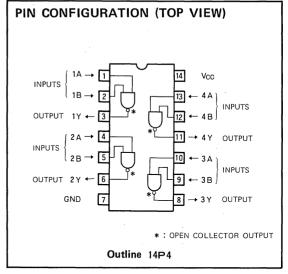
FUNCTIONAL DESCRIPTION

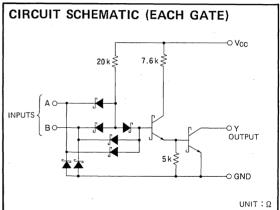
With use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

When inputs A and B are high, output Y is low and when one or both inputs are low, the output Y is high.

FUNCTION TABLE

Α	В	Υ
L	L	Н
н	L	Τ
L	н	Н
Н	н	L





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75°	℃
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	0			Limits			
Symbol	. Paramet	Parameter		Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
ЮН	High-level output current	V ₀ =5.5V	0		100	μА	
		V _{OL} ≤0.4V	. 0		4	mA	
loL	Low-level output current VoL≤0.5V		0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

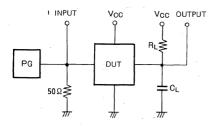
C 1					Limits		
Symbol	Parameter	l est co	nditions	Min	Тур *	Max	Unit
VIH	High-level input voltage						٧.
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18 mA			-1.5	V
1.	IP-b I I	V _{CC} =4.75V, V _I =0	V8.V			100	
Іон	High-level output current	V ₀ =5.5V				100	μА
\/	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =8mA		0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V _I =2	2.7V	1		20	μА
Ιн	riigh-level input current	V _{CC} =5.25V, V _I =1	V _{CC} =5.25V, V _I =10V			0.1	mA
hL	Low-level input current	V _{CC} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Іссн	Supply current, all inputs high	V _{CC} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0V		0.8	1.6	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4	1.5V		2.4	4.4	mA

^{* :} All typical values are at V_{CC}=5V, Ta=25°C

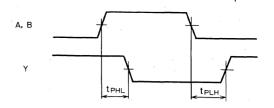
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		t to ta
		rest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level/high-to-low-level	$R_L = 2 k\Omega$		10	32	ns
tenc	output propagation time	C _L = 15 pF (Note 1)		10	28	ns

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) CL includes probe and jig capacitance.



HEX INVERTERS

DESCRIPTION

The M74LS04P is a semiconductor integrated circuit containing 6 inverter circuits.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (Pd = 12mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

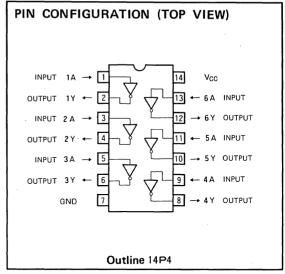
FUNCTIONAL DESCRIPTION

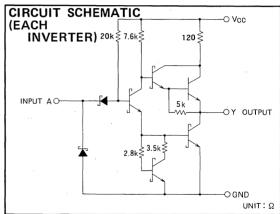
The use of Schottky TTL technology enables the achievement of high input voltage, high speed, low power dissipation and high fan-out.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

A	Y
L	Н
. Н	L





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage .		-0.5~+15	V
Vo ,	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	D					
Symbol Parameter		er .	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	· V
I _{OH}	High-level output current	V _{0H} ≥2.7V	0		-400	μА
1.	Low level output output	V _{OL} ≤0.4V	. 0		4	mA
I _{OL} Low-level output current	V ₀ L≦0.5V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

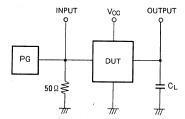
Constant	Postmotor	T	- dist	Limits				
Symbol	Parameter		onditions	Min	Тур*	Max	Unit	
V _{IH}	High-level input voltage			2			V	
VIL	Low-level input voltage					0.8	V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	V	
Voн	High-level output voltage	V _{CC} =4.75V, V _I =0	$V_{CC}=4.75V, V_{I}=0.8V, I_{OH}=-400 \mu A$		3.4		V	
V	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	. V	
VoL		I _{OL} =8mA		0.35	0.5	V		
L	High lovel input average	V _{CC} =5.25V, V _I =2	.7V			20	μА	
lін	High-level input current	V _{CC} =5.25V, V _I =1	0V			0.1	mA	
IIL	Low-level input current	V _{CC} =5.25V, V _I =0	.4V			-0.4	mA	
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0	OV .	- 20		-100	mΑ	
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0	IV		1.2	2.4	. mA	
Iccl	Supply current, all outputs low	V _{CC} =5.25V, V _I =4	.5V		3.6	6.6	mA	

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

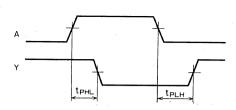
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Faranietei	rest conditions	Min	Тур	Max	Offit
t _{PLH}	High-to-low-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	Low-to-high-level output propagation time	(Note 2)		- 6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , Z_{O} = 50 Ω
- (2) C_L includes probe and jig capacitance.





Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS05P is a semiconductor integrated circuit containing 6 open collector output inverter circuits.

FFATURES

- Usable in AND-Tie connection.
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 12mW typical)
- High speed (tpd = 10ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

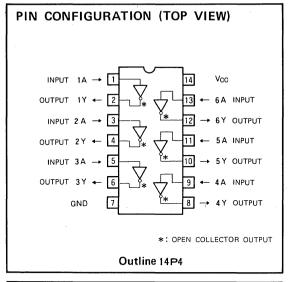
FUNCTIONAL DESCRIPTION

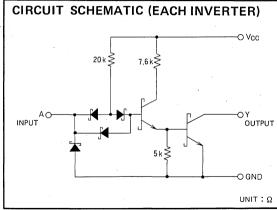
With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

Α	Y
L	Н
Н	L





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃

HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		,		Limits		Unit
Symbol	ymbol Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V ₀ =5.5V	0		100	μА
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V ₀ L≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

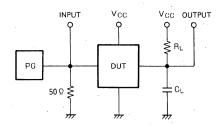
			Test conditions		Limits		11-1-
Symbol	Parameter	lest o			Тур*	Max	Unit
VIH	High-level input voltage			2			V.
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	
Гон	High-level output current	V _{CC} =4.75V, V _I =	$V_{CC}=4.75V, V_1=0.8V, V_0=5.5V$			100	μА
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output vortage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	٧
	High-level input current	V _{CC} =5.25V, V _I =2	2.7V			20	μА
lін	High-level input current	V _{CO} =5.25V, V _I =	10V			0.1	mA
Ι _Ι L	Low-level input current	V _{CO} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			1.2	2.4	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	open		3.6	6.6	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

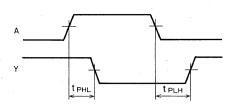
			Limits			11.24
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	R _L = 2 kΩ		10.	32	ns
t _{PHL}	High-to-low-level output propagation time	C _L = 15pF (Note 1)		10	. 28	ns

Note 1: 'Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω

(2) C_L includes probe and jig capacitance.



M74LS08P

QUADRUPLE 2-INPUT POSITIVE AND GATES

DESCRIPTION

The M74LS08P is a semiconductor integrated circuit containing 4 dual input-positive AND and negative OR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 17mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

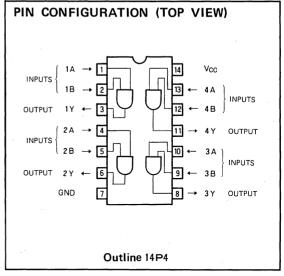
FUNCTIONAL DESCRIPTION

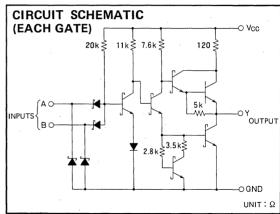
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B are high, output Y is high, and when either or both of the inputs are low, Y is low.

FUNCTION TABLE

Α	В	Y
L	L	L
Н	L	L
L	Н	L
Н	Н	н





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE AND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Symbol Parameter			Limits		Unit
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
I _{OL} Low-level output current	Low-level output current	V ₀ L≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		T	Test conditions		. Limits		
Symbol	Parameter	l'est condi			Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage	·				0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_{I} = 2V$, $I_{OH} = -400 \mu A$		2.7	3.4		V
	Law L	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =0.8V	I _{OL} = 8mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =2.7V	,			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	· mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 20		- 100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =4.5V			2.4	4.8	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =0V			4.4	8.8	mA

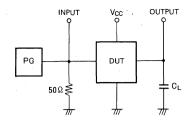
* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

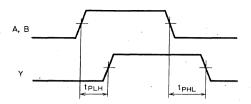
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	r al diffetel	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		9	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$
- (2) C_L includes probe and jig capacitance.



M74LS09P

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS09P is a semiconductor integrated circuit containing 4 dual-input positive AND and negative OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V₁ ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power consumption (Pd = 17mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

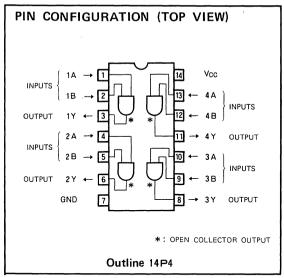
FUNCTIONAL DESCRIPTION

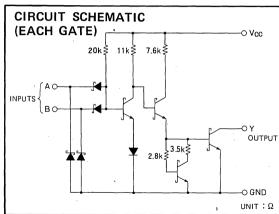
With the use of open collector output, the high-level output impedance can be freely selected by means of an external load resistor. This enables use in wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high, output Y is high and when either or both of them are low, Y is low.

FUNCTION TABLE

Α	. В	Y
L	L	L
H	L	L
L	Н	L
н	Н	Н





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		$-0.5 \sim +7$	V
Vı	Input voltage	·	-0.5~+15	· V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~+150	. ℃

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			11-14			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4 .75	5	5.25	٧	
Іон	High-level output current	V ₀ =5.5V	0		100	μА	
		V _{0L} ≤0.4V	V ₀ L≦0.4V	0		4	mA
l lor	Low-level output current V ₀ L≤0.5V		0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

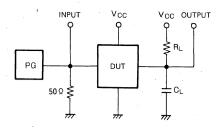
		T			Limits		11.24
Symbol	Parameter	Test conditions		Min	Тур*	Max	Unit
VIH	High-level input voltage			2			·V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧.
Гон	High-level output current	V _{CC} =4.75V, V _I =	$V_{CC} = 4.75V, V_1 = 2V, V_0 = 5.5V$			100	μА
	L	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V _{OL}	Low-level output voltage V ₁ =	V _I =0.8V I _{OL} =8mA	I _{OL} =8mA		0.35	0.5	٧
		V _{CC} =5.25V, V _I =2	2.7V			20	μА
liH.	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
lıL.	Low-level input current	V _{CC} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	V _{CC} =5.25V, V _I =0V		2.4	4.8	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		4.4	8.8	- mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

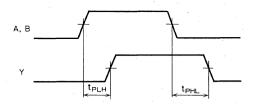
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter Test conditions		Limits			
Syllibol	, r _i arameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	High-to-low-level output propagation time	$R_L = 2 k\Omega$		15	35	' ns
t _{PHL}	Low-to-high-level output propagation time	C _L =15pF (Note 1)		10	35	ns

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.



TRIPLE 3-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS10P is a semiconductor integrated circuit containing three triple-input positive NAND and negative NOR gates.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (Pd = 8mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

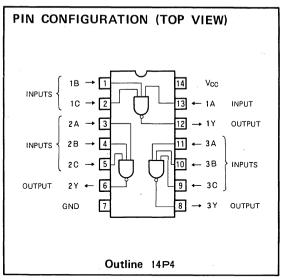
The use Schottky TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation and high fan-out.

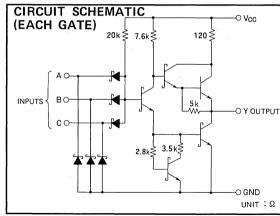
When all inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

Α	N	Υ
L.	L	н
н	L	н
L	Н	Ι
Н	Н	L

 $N = B \cdot C$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

TRIPLE 3-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			
			Min	Тур	Max	Unit	
V _{CC}	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА	
	1	V ₀ L≦0.4V	0		4	mΑ	
loL	Low-level output current V ₀ L≤0.5V		0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	_	T	4'4'	Limits			11-14
Symbol	Parameter	Test of	Test conditions		Тур*	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	-18mA			-1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =	$V_{CC} = 4.75V$, $V_{I} = 0.8V$, $I_{OH} = -400 \mu A$. 3.4		V
	1	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ = 2V	I _{OL} =8mA		0.35	0.5	V
1		V _{CC} =5.25V, V _I =2	2.7V			20	μΑ
Ιн	High-level input current	$V_{CC} = 5.25V, V_I = 1$	0V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0).4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	0V	- 20		- 100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =	ΟŲ		0.6	1.2	mA
Iccl	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		1.8	3.3	mA

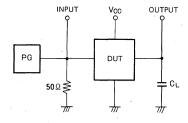
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

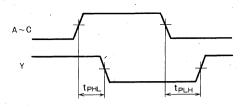
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Symbol Parameter	Test conditions	Limits			Unit
Syllibol		rest conditions	Min	Тур	Max	·
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		9	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.



TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS11P is a semiconductor integrated circuit containing three triple-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (P_d = 13mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

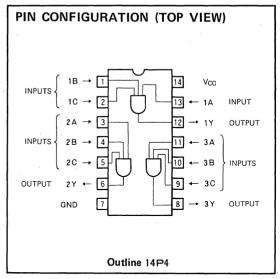
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, lower power dissipation and high fanout.

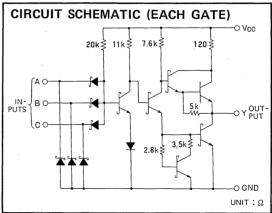
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

Α	N	Υ
L.	L	L
н	L	L
L	Н	L
Н	Н	Н

 $N = B \cdot C$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level state	-0.5~V _{CC}	· V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	. ℃

TRIPLE 3-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Complete	Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА	
		V _{OL} ≤0.4V	0		4	mΑ	
, lo∟	Low-level output current V ₀ L≤0.5V		0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test condit	tions		Limits		Unit
Symbol	i di diffeter	Test condit	rest conditions		Тур *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V, V_{I} = 2V,$	I _{OH} = - 400μA	2.7	3.4		V
	Low-level output voltage	V _{CC} =4.75V	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
VoL	Low-level output voltage	V _I =0.8V	I _{OL} =8mA		0.35	0.5	. V
I	High-level input current	V _{CC} =5.25V, V _I =2.7V	<i>'</i>			- 20	μА
Іін	riigh-lever input current	V _{CC} =5.25V, V _I =10V				0.1	· mA
, I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V	<i>'</i>			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
I _{CCH}	Supply current, all outputs high	V _{CC} =5.25V, V _I =4.5V	/		1.8	3.6	mΑ
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I = 0V			3.3	6.6	mΑ

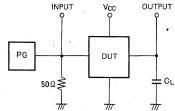
^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

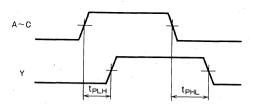
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol Parameter		Test conditions		Limits		l lada
Gymbol	- arameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high output level propagation time	C _L =15pF	`	9	15	ns
t _{PHL}	High-to-low output level propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) CL includes probe and jig capacitance,



TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS12P is a semiconductor integrated circuit containing three triple-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 6mW typical)
- High speed (t_{nd} = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

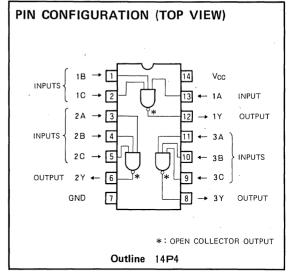
With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

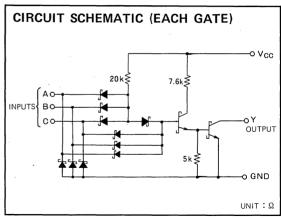
When inputs A, B and C are high, output Y is low and when one or more of the inputs is low, the output Y is high.

FUNCTION TABLE

Α	N	Υ
L	L	н
н	L	Н
L	н	Η
Η	н	L

 $N = B \cdot C$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~ +150	. ℃

TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (Ta=-20~+75°C, unless otherwise noted)

	P			Limits ,			
Symbol	Paramet	er -	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5 . 25	, V	
Іон	High-level output current	V ₀ =5.5V	0		100	μА	
		V ₀ L≦0.4V	0	1	4	mA .	
lor '	Low-level output current V _{OL} ≤0.5V		. 0		8	mA:	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

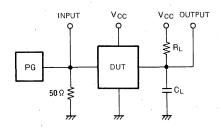
Symbol	Parameter	Toot o	onditions		Limits		
Syllibol .	Farameter	rest d	oriditions	Min	Typ *	Max	Ųnit
VIH	High-level input voltage						V
. VIL	Low-level input voltage		, .			0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
Гон	High-level output current	V _{CC} =4.75V, V _I =	V _{CC} =4.75V, V _I =0.8V, V _O =5.5V			100	μΑ
V		V _{CC} =4.75V	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =8mA		0.35	0.5	· V
ин	High-level input current	V _{CC} =5.25V, V _I =	2.7V			20	μА
	Tight level impat corner.	V _{CC} =5.25V, V _I =	10 V			0.1	mΑ
IIL	Low-level input current	V _{CC} =5.25V, V _I =	0.4V		,	-0.4	mΑ
Госн	Supply current, all inputs high	V _{CC} =5.25V, V _I =	0 V		0.7	1.4	mA
ICCL	Supply current, all inputs low	V _{CC} =5.25V, V _I =	4.5V		1.8	3.3	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

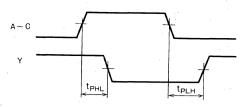
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol Parameter	Parameter		Test conditions		Limits		11.2
Symbol	i arameter		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level/high-to-low level	$R_L = 2 k\Omega$			10	32	ns
t _{PHL}	output propagation time	C _L =15pF	(Note)		15	28	ns

Note: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.



DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS13P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage $(V_1 \ge 15V) \cdot (V_1 \ge 15V, V_0 \ge 7V)$
- Low power dissipation (P_d = 17.5mW typical)
- High speed (tpd = 16ns typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

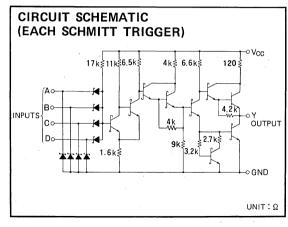
FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

When inputs A, B, C and D are high, output Y is low, and when one or more of the inputs are low, Y is high.

Refer to M74LS14P for the typical characteristics.

PIN CONFIGURATION (TOP VIEW) INPUTS 1B → 2 NC 3 INPUTS 1C → 4 ID → 5 OUTPUT 1Y ← 6 GND 7 Outline 14P4 NC: NO CONNECTION



FUNCTION TABLE

, A	N	Υ
L	L	н
Н	L	Н
L	Н	Н
Н	H	L

 $N = B \cdot C \cdot D$

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٠.٨
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

		Parameter		Limits		
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
	Law lavel autout aurrant	V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C, unless otherwise noted.)

Cumbal	Parameter	Test condit		-	Limits		Unit
Symbol	Farameter	Test condit	ions	Min	Typ *	Max	Onit
V _{T+}	Positive-going threshold voltage	V _{CC} =5V	- 1	1.4	1.6	1.9	V
V _T -	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V		0.4	0.8		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V
.,	V _{OH} High-level output voltage	V _{CC} =4.75V, V _I =0.5V		0.7	2.4		V
У ОН		$I_{OH} = -400 \mu A$		2.7	3.4		. •
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage	V _I =1.9V	I _{OL} =8mA		0.35	0.5	V
l _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-0.14		mA
I _T _	Input current at negative-going threshold	V _{CC} =5V, V _I =V _{T-}			-0.18		mA
	High level in the second	V _{CC} =5.25V, V _I =2.7V	/			20	μА
liH	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V	/			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V ₀ =0V		-20		— 100	· mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			2.9	6	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5V	/		4.1	7	mA

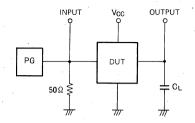
^{* :} All typical values are at V_{CC} = 5.V, T_a = 25°C

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

$\textbf{SWITCHING CHARACTERISTICS} \ (V_{CC} = 5 \text{V. Ta} = 25 ^{\circ} \text{C, unless otherwise noted})$

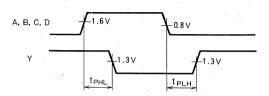
Cumbal	Symbol Parameter	Test conditions		Limits		Unit
Symbol		rest conditions	Min	Тур	Max	Ont
t _{PLH}	Low-to-high-level output propagation time	C ₁ = 15 pF (Note 2)		12	22	ns
tPHL	High-to-low-level output propagation time	OL 19pr (Note 2)		20	27	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM



M74LS14P

HEX SCHMITT TRIGGER INVERTERS

DESCRIPTION

The M74LS14P is a semiconductor integrated circuit containing 6 Schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysterisis width (0.8V typical) and high noise margin
- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 51mW typical)
- High speed (tpd = 12ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

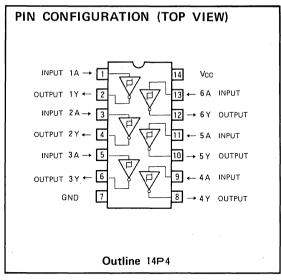
FUNCTIONAL DESCRIPTION

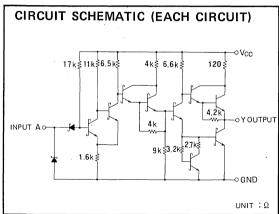
The use Schottly TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysterisis width is 0.8V (typical). Accordingly, noise margin is high. Even slow changing input signals result in a shaped waveform output without casing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

Α	Υ
L	Н
Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V -
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	ol Parameter			Unit		
Symbol			Min	Nom	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
	I _{OL} Low-level output current	V ₀ ∟≦0.4V	0		4	mΑ
OL		V _{0L} ≦0.5V	0		8	mA

HEX SCHMITT TRIGGER INVERTERS

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

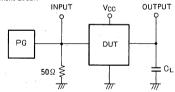
		T	Test conditions		Limits		
Symbol	Parameter	Test cond	irtions	Min	Тур*	Max	Unit
V _{T+}	Positive-going threshold voltage	V _{CC} =5V		1.4	1.6	1.9	· V
V _T _	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	· V
V _{T+} -V _{T-}	Hysteresis	V _{CC} =5V		0.4	0.8		V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V
	V _{OH} High-level output voltage	V _{CC} =4.75V, V _I =0.5	5V _		2.4		V
VOH		$I_{OH} = -400 \mu A$		2.7	3.4		V
.,	<i>i</i> - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage	V _I =1.9V	I _{OL} =8mA		0.35	. 0.5	V
1_+	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-0.14		mA
IT-	Input current at negative-going threshold	V _{CC} =5V, V _I =V _T -			-0.18		mA
	115-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	V _{CC} =5.25V, V _I =2.7	V			20	μА
hн .	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA ⁻
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, 'V ₀ =0V		-20		- 100	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			8.6	16	mA -
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5V	/		12	21	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING: CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

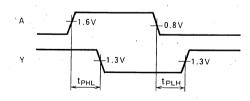
Symbol	Symbol Parameter	Parameter Test conditions	Limits			11.2
Symbol	i ai airietei	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	0 15 5 (No. 10)		12	22	ns
tpHL	High-to-low-level output propagation time	C _L =15pF (Note 2)		12	22	ns

Note 2: Measurement circuit



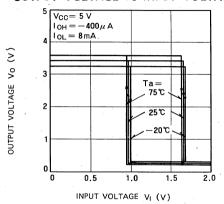
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P , Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

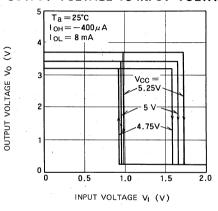


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE



OUTPUT VOLTAGE VS INPUT VOLTAGE



Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS15P is a semiconductor integrated circuit containing 3 triple-input positive AND and negative OR gates with open collector outputs.

FFATURES

- Usable in wire-AND connection
- High breakdown input voltage $(V_1 \ge 15V)$
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (P_d = 13mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

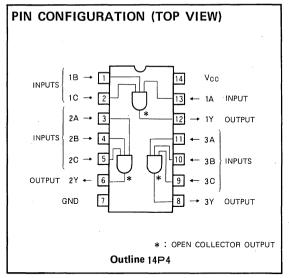
With the use of Schottky TTL Technology and open collector outputs with a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

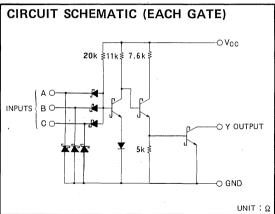
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

Α	N	Y
L	L	L
Н	L	L
L	н	L
н	Н	Н

 $N = B \cdot C$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V _I	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		- 20 ~ + 75	°C
Tstg	Storage temperature range		-65∼+150	°C

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	D			Limits		Unit
Symbol	Parameter -		Min	Тур	Max	1 Office
Voc	Supply voltage	:	4.75	5	5.25	V
Гон	High-level output current	V ₀ =5.5V	0		100	μΑ
Lou	I OL Low-level output current	V _{OL} ≤0.4V	0		4	mA
TOL		V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

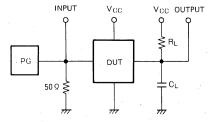
Combal	Devementer	Conditions		Limits			Unit
Symbol	Parameter			Min	Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Гон	High-level output current	V _{CC} =4.75V, V _I =2V, V _O =5.5V				100	μΑ
\/a.	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	٧.
V _O L	Low-level output voltage	V _I =0.8V	I _{OL} = 8mA		0.35	0.5	>
he	High-level input current	V _{CC} =5.25V,V _I =2.	7 V			20	μΑ
чн	Thigh-lever input current	V _{CC} =5.25V,V _I =10V				0.1	mΑ
liL	Low-level input current	V _{CC} =5.25V,V _I =0.4	4 V			-0.4	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V,V ₁ =4.	5V		1.8	3.6	mA ·
Iccl	Supply current, all outputs low	V _{CC} =5.25V,V _I = 0	•		3.3	6.6	mA

^{*:} All typical values are at V_{CC}=5V, T_a=25°C.

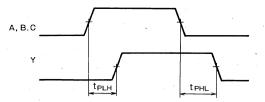
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зуптвог	i dianietei	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level output propagation time	R _L =2KΩ		15	35	ns
t _{PHL}	High-to-low-level output propagation time	CL=I5pF (Note)		10	35	ns

Note: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) CL includes probe and jig capacitance.



DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS18P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 22mW typical)
- High speed (t_{nd} = 24ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

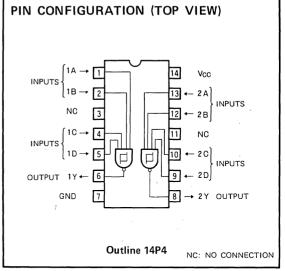
FUNCTIONAL DESCRIPTION

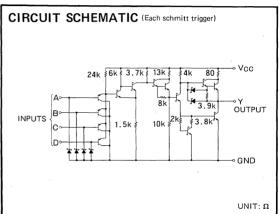
It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A, B, C and D inputs are high, output Y is low, and when more than one is low, Y is high.

M74LS13P can be replaced with M74LS18P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.





FUNCTION TABLE

Α	Z	Y
L	L	Н
Н	L	Н
L	н	н
Н	. н	L

 $N = B \cdot C \cdot D$

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~+150	°C



DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter			Limits				
			Min	Тур	Max	Unit		
V _{CC}	Supply voltage		4.75	5	5.25	ν		
Гон	High-level output current	V _{0H} ≧2.7V	0		-400	μА		
I _{OL} Low-		V _{OL} ≦0.4V	0		4	mA		
	Low-level output current VoL≤0.5V		0		8	mA -		

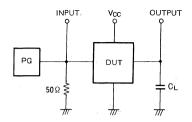
ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Completed.	Parameter	T	allal		Limits	.	Unit
Symbol	Parameter	Test con	ditions	Min	Typ *	Max	
V _T +	Positive-going threshold voltage	V _{CC} =5V		1.65	1.9	2.15	V
V _T -	Negative-going threshold voltage	V _{CC} =5V		0.75	1.0	1.25	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V		0.4	0.9		· V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	· V
V _{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.5V$ $I_{OH} = -400 \mu A$		2.7	3.4		·V
.,		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =1.9V	I _{OL} =8mA		0.35	0.5	٧
I _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-2		μΑ
I _T _	Input current at negative-going threshold	V _{CC} =5V, V _I =V _T -			-5		μΑ
	High total total	V _{CC} =5.25V', V _I =2.	7 V			20	μA
ин	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.05	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 20		-100	, mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			3.3	6	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.	5V		5.7	10	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

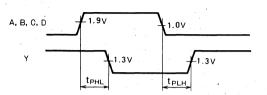
Symbol	Parameter	Test conditions C _L =15 pF (Note 2)	Limits			
- Cyllibor	ymbol Farameter Test conditions	Min	Тур	Max	Unit	
tpLH	Low-to-high-level output propagation time	0 45 5 (1) 0)		12	20	ns
tpHL	High-to-low-level output propagation time	CL= 15 pF (Note 2)		37	55	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, Vp = 3Vp.p, $Z_0 = 50\Omega$ (2) CL includes probe and jig capacitance.

TIMING DIAGRAM





^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

HEX SCHMITT TRIGGER INVERTER

DESCRIPTION

The M74LS19P is a semiconductor integrated circuit containing 6 schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage (V₁ ≥15V)
- Low power dissipation (Pd = 67mW typical)
- High speed (t_{nd} = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

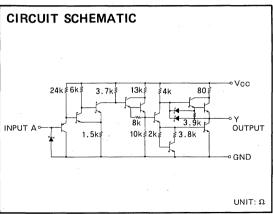
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

M74LS14P can be replaced with M74LS19P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.



FUNCTION TABLE

Α	Υ
L	Н
Н	L

ABSOLUTE MAXIMUM RATINGS

($Ta = -20 \sim +75 \, ^{\circ}\!\!\! \mathrm{C}$, unless otherwise noted)

			· ·	
Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	ν.
Topr	Operating free-air ambient temperature range		-20~+75	,C
Tstg	Storage temperature range		-65~+150	,C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Unit		
	. raramet	Min	Тур	Max	Onit	
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	1 1 1	. V _{OL} ≦ 0.4V	0		4	mA
I _{OL} Low-level of	Low-level output current	V ₀ L≦0.5V	0		8	mA

HEX SCHMITT TRIGGER INVERTER

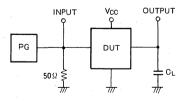
ELECTRICAL CHARACTERISTICS (Ta=-20~+75℃, unless otherwise noted)

				.	Limits		
Symbol	Parameter	Test condi	tions	Min	Typ *	Max	Unit
V _{T,+}	Positive-going threshold voltage	V _{CC} =5V	V _{CC} =5V		1.9	2.15	. V .
V _T	Negative-going threshold voltage	V _{CC} =5V	V _{CC} =5V		1.0	1.25	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V	V _{CC} =5V		0.9		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	٧
		V _{CC} =4.75V, V _I =0.5V	/				.,
V _{OH}	High-level output voltage	$I_{OH} = -400 \mu A$		2.7	3.4		V
.,		V _{CC} =4.75V	I _{OL} =4mA	1	0.25	0.4	V
V _{OL}	Low-level output voltage	V ₁ =1.9V	I _{OL} =8mA		0.35	0.5	V
I _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-2		μΑ
I _T _	Input current at negative-going threshold	V _{CC} =5V, V _I =V _{T-}			-5		μΑ
		V _{CC} =5.25V, V _I =2.7V	/			20	μА
ήн	High-level input current	V _{CC} =5.25V, V _I =10V	V _{CC} =5.25V, V _I =10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V	V _{CC} =5.25V, V _I =0.4V			-0.05	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V ₀ =0V	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	-20		— 100	mΑ
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			9.9	18	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5V	/	-	17	30	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

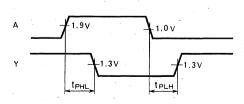
Symbol	Parameter Test conditions		Limits			Unit
	, diamoto	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	0 -15-5 (N-+-2)		11	20	ns
tpHL	High-to-low-level output propagation time	C _L =15pF (Note 2)		15	30	ns

Note 2: Measurement circuit



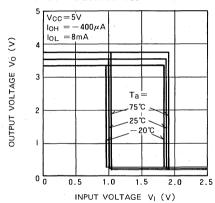
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , $Z_0 = 50\Omega$
- (2) CL includes probe and jig capacitance.

TIMING DIAGRAM

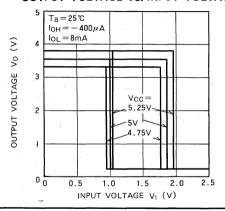


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS. INPUT VOLTAGE



OUTPUT VOLTAGE VS. INPUT VOLTAGE



^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS20P is a semiconductor integrated circuit containing two 4-input positive NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (P_d = 4mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

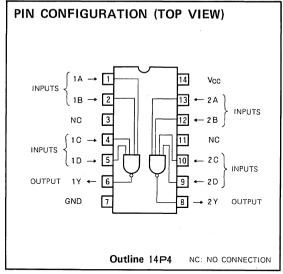
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

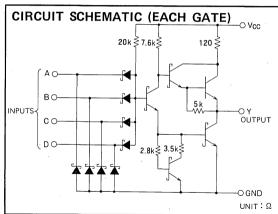
When inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Y
L	L	Н
Н	L	Н
L	H·	Н
Н	Н	L

 $N = B \cdot C \cdot D$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀ .	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		·-65~+150	°C

DUAL 4-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Course board				Limits		
Symbol	Paramet	er	Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
OL	IoL Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Control	D	T	Test conditions		Limits		Unit
Symbol	Parameter	l est con	aitions	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					8.0	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	. V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =0	.8V, I _{OH} = -400 μA	2.7	3.4		. V
	Low lovel autout valtage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٠V
Vol	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High Investment of	V _{CC} =5.25V, V _I =2	.7V			20	μА
Чн	High-level input current	$V_{CC} = 5.25V, V_I = 10$	٠ ٧			0.1	mA
- I _I L	Low-level input current	V _{CC} =5.25V, V _I =0	.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0)V	- 20		-100	mA
I _{CCH}	Supply current, all inputs high	V _{CC} =5.25V, V _I =0	V -		0.4	0.8	mA
Iccl	Supply current, all inputs low	V _{CC} =5.25V, V _I =4	.5V		1.2	2.2	mA

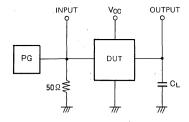
^{* :} All typical values are at V_{CC}=5V, Ta=25℃

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

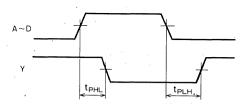
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Danasasas	Test conditions		Limits		
Symbol	Parameter	rest conditions	Min .	Тур	Max	Unit
t _{PLH}	Low-to-high-level/high-to-low-level	C _L =15pF		6	15	ns
t _{PHL}	output propagation time	(Note 2)		13	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.



DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS21P is a semiconductor integrated circuit containing two 4-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 8.5mW typical)
- High speed (tpd = 9ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

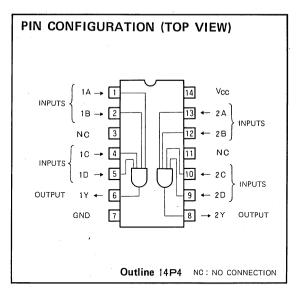
FUNCTIONAL DESCRIPTION

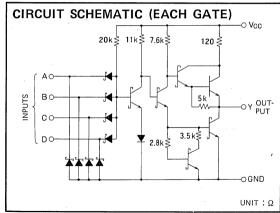
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

When inputs A, B, C and D are high, output Y is high, and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

Α	N	Y
L	L	L
Н	L	L
L	Н	L
Н	Н	I





Symbol	Parameter	Conditions	Limits	· Unit
Vcc	Supply voltage		-0.5∼+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range	-	-65~+150	℃

DUAL 4-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

C	Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
		V _{OL} ≦0.4V	0		4	mA	
lor	Low-level output current VoL≤0.5V		0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D	T	Test conditions		Limits		Unit
Symbol	Parameter Parameter	Test cond			Typ *	Max	Unit
VIH .	High-level input voltage						٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧
VoH	High-level output voltage	V _{CC} =4.75V, V ₁ =2V,	I _{OH} = -400 μA	2.7	3.4		٧
.,		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VoL	Low-level output voltage	V ₁ =0.8V	I _{OL} = 8 mA		0.35	0.5	V
liн	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μΑ
чн	riginever input current	V _{CC} =5.25V, V _I =10V				0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V .			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =4.5	V		1.2	2.4	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =0V			2.2	4.4	mΑ

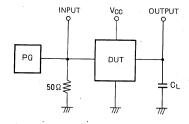
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

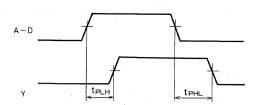
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter Test conditions		Limits			Unit
Cymbol	l alametei .	l est conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-output level propagation time	C _L =15pF		9	15	ns
, t _{PHL}	High-to-low-output level propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) CL includes probe and jig capacitance.



DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS22P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_1 \ge 15V$)
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (P_d = 4mW typical)
- High speed (tnd = 18ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

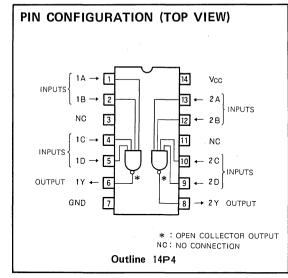
With the use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

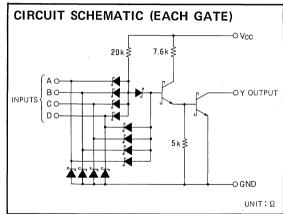
When inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Y
L	L	Н
H	L	Н
L	н	Н
Н	Н	L

 $N = B \cdot C \cdot D$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING OCNDITIONS (Ta = -20~+75°C, unless otherwise noted)

	Parameter			Unit		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V ₀ =5.5V	0		100	μА
	Low-level output current	V ₀ L≦0.4V	0		4	mΑ
lor		V ₀ L≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = -20~+75°C, unless otherwise noted)

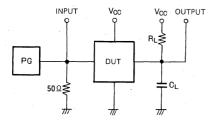
C	Parameter	-	Test conditions		Limits		Unit
Symbol		l est c			Typ *	Max	Unit
ViH	High-level input voltage			- 2			V
V _{IL}	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
Іон	High-level output current	V _{CC} =4.75V. V _I =0.8V V _O =5.5V				100	μА
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
1	High level in the second	V _{CC} =5.25V, V _I =	2.7V			20	μА
Ιιн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
1 ссн	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.4	0.8	mA
ICCL	Supply current, all inputs low	V _{CC} =5.25V, V _I =	4.5V		1.2	2.2	mΑ

^{* :} All typical values are at V_{CC}=5V, T_a=25°C

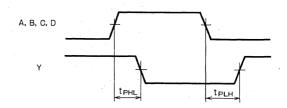
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	raianietei	Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level/high-to-low-level	R _L = 2 kΩ		10	3 2	ns
tpHL	output propagation time	C _L =15pF (Note 1)		25	28	ns

Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns; V_P = $3V_{P,P}$, Z_Q = 50Ω



⁽²⁾ C_L includes probe and jig capacitance.

OUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS24P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 44mW typical)
- High speed (t_{rod} = 18ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

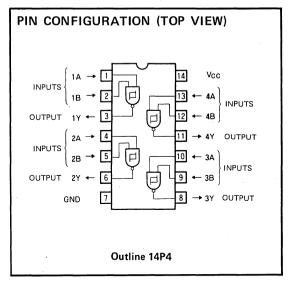
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A and B inputs are high, output Y is low, and when more than one is low, output Y is high.

M74LS132P can be replaced with M74LS24P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level

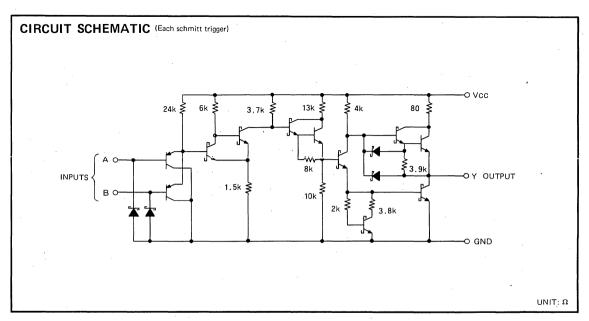


of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.

FUNCTION TABLE

ĺ	,A	В	Υ
	L	L	н
	н	L	Н
	L	Н	н
	Н	н	L



QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	ర
Tstg	Storage temperature range		-65~+150	τ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol				Unit		
	Parameter		Min Typ Max			Oiiit
Vcc	Supply voltage		4.75	5	5.25	V
IoH	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ
loL	Low-level output current	V ₀ L≦0.4V	0		4	mA
	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Crossels al	Daysmator	Tout on	Test conditions		Limits		
Symbol	Parameter	Test co	onditions	Min	Тур *	Max	Unit
V _{T+}	Positive-going threshold voltage	V _{CC} =5V		1.65	1.9	2.15	V
V _T -	Negative-going threshold voltage	V _{CC} =5V	,	0.75	1.0	1.25	٧
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V		0.4	0.9		٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18mA			- 1.5	V
Voн	High-level output voltage	$V_{CC}=4.75V, V_{I}=0$ $I_{OH}=-400\mu A$.5V	2.7	3.4		V
	I am land and a sales	V _{CC} =4.75V	I _{OL} =4mA 0.25 0.4	0.4	V		
VoL	Low-level output voltage	V _I = 1.9V	I _{OL} =8mA		0.35	0.5	V
IT+	Input current at positive-going threshold	V _{CC} =5V, V _I =V _T -	$V_{CC}=5V$, $V_{I}=V_{T+}$		-2		μΑ
IT-	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_T$	_		-5		μΑ
		V _{CC} =5.25V	,			20	V V V V V μΑ μΑ μΑ
liн	High-level input current	V _I =2.7V					
''''	riigii level iiipat callent	V _{CC} =5.25V				0.1	
		V _I = 10 V					
lı∟	Low-level input current	$V_{CC} = 5.25V, V_{I} =$	0. 4 V			-0.05	mA .
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _C =	:0V	. — 20		— 100	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	0V		6.6	12	mA
Iccl	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		11	20	mA

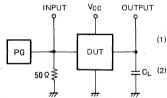
^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

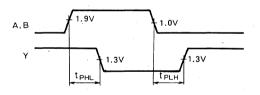
Symbol	Parameter	Test conditions		Limits		11-1-
Symbol	i arametei	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C ₁ = 15pF (Note 2)		13	. 20	· ns
t _{PHL}	High-to-low-level output propagation time	CL= 15pF (Note 2)		24	40	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P.P, Z_O = 50Ω
 C_L (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM





TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74LS27P is a semiconductor integrated circuit containing three triple-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 13.5mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

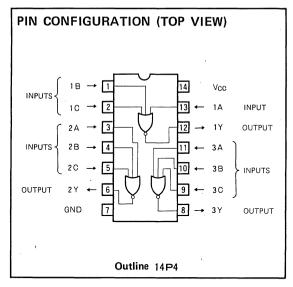
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

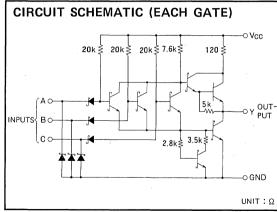
When one or more of the A, B and C inputs are high, output Y is low and when all inputs are low, Y is high.

FUNCTION TABLE

Α	2	Υ
L	L	Н
н	L	L
L	н	L ·
Н	Н	L

$$N = B + C$$





Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150 ·	°C

TRIPLE 3-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D			Limits		Unit	
Symbol	Paramet	Parameter		Min Typ Max		Omit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
:		V _{OL} ≤0.4V	0		4	mA	
IOL	IoL Low-level output current	V _{0L} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumbal	Resembles	Toot	Test conditions		Limits		Unit
Symbol	Parameter	rest	conditions	Min	Typ*	Max	Unit
ViH	High-level input voltage						V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA			-1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =	$V_{CC}=4.75V$, $V_{I}=0.8V$, $I_{OH}=-400\mu A$		3.4		V
.,	Low lovel output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =	2.7V			20	μΑ
lтн	nigh-lever input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
. los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	V _{CC} =5.25V, V _O =0V			-100	mA
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	V _{CC} =5.25V, V _I =0V		2	4	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		3.4	6.8	mΑ

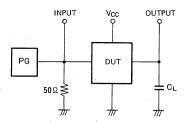
^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

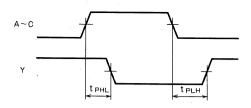
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	i alametei	lest conditions	Min	Тур	Max	oʻnit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)	-	6	ـ15	ns ·

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) CL includes probe and jig capacitance,



M74LS30P

SINGLE 8-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS30P is a semiconductor integrated circuit containing one 8-input positive-logic NAND gate, usable as a negative-logic NOR gate.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 2.4mW typical)
- High speed (tpd = 11ns typical)
- Low output impedance
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

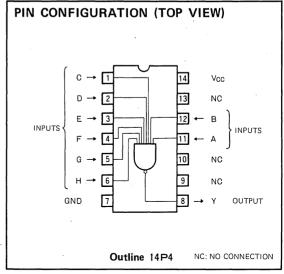
FUNCTIONAL DESCRIPTION

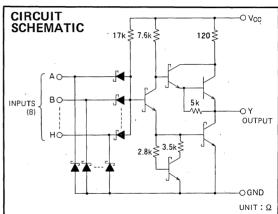
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

When inputs A, B, C, D, E, F and G are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Y
L	L	Н
Н	L	н
L	Н	Ξ
Н	Н	L





ABSOLUTE MAXIMUM RATINGS (Ta = $-20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5-+V _{CC}	V
Topr	Operating free-air ambinet temperature range		· -20~+75	°C
Tstg	-Storage temperature range	4	-65~+150	°C



SINGLE 8-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Constant			-	Limits		Unit
Symbol	Paramet	er ·	Min Typ Max			
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА.
		V _{OL} ≦0.4V	0		4	mA
I _{OL} Low-level ou	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

0	Parameter	Total and dis			Limits		Unit
Symbol	rarameter	Parameter Test conditions		Min	Typ *	Max	Onit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0.8	$V_{CC}=4.75V$, $V_1=0.8V$, $I_{OH}=-400\mu A$		3.4		V
.,,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μA
Іін	right-level input current	V _{CC} =5.25V, V _I =10\	/			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output circuit (Note 1)	V _{CC} =5.25V, V _O =0V	V _{CC} =5.25V, V _O =0V			-100	· mA
Гссн	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.35	0.5	. mA
IccL	Supply current, all inputs low	V _{CC} =5.25V, V _I =4.	5V		0.6	1.1	mA

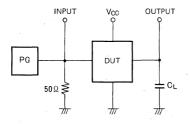
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 1: All measurements should be done quickly.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

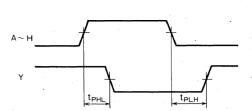
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	· · · · · · · · · · · · · · · · · · ·	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level/high-to-low-level	C _L =15pF		6	15	. ns
t _{PHL}	output propagation time	(Note 2)		16	20	กร

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characterisites: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns; V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the $V_{\mbox{\footnotesize CC}}$ supply voltage.

M74LS32P

QUADRUPLE 2-INPUT POSITIVE OR GATES

DESCRIPTION

The M74LS32P is a semiconductor integrated circuit containing 4 dual-input positive OR and negative AND gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 20mW typical)
- High speed (tpd = 7ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

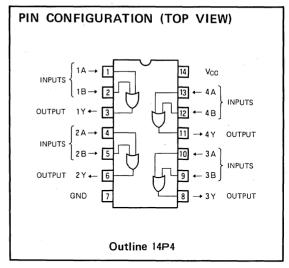
FUNCTIONAL DESCRIPTION

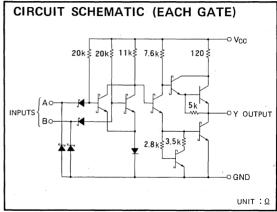
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When either or both of the inputs A and B is/are high, output Y is high, and when both A and B are low, Y is low.

FUNCTION TABLE

Α	В	Υ
L	L	L
н	L	H
L	н	н
Η	Н	Н





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo .	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range	;	−65~+150	℃

QUADRUPLE 2-INPUT POSITIVE OR GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits	*.	Unit
Symbol .	Symbol Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
. 1		V _{OL} ≤0.4V	0		- 4	mA
OL	I _{OL} Low-level output current	V ₀ L≦0.5V	0.		. 8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T	- utat		Limits		11-14
Symbol	Parameter	l est co	Test conditions		Тур*	Max	Unit
.V _{IH}	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧.
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	—18mA			-1.5	٧
VoH	High-level output voltage	$V_{CC}=4.75V$, $V_{I}=2V$ $I_{OH}=-400\mu A$		2.7	3.4		V
.,	Law law Law at water	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	٠٧
V _{OL}	Low-level output voltage	V _I =0.8V	I _{OL} =8mA		0.35	0.5	٧
1	High level innut overent	V _{CC} =5.25V, V _I =2	.7V			20	μА
Iн	High-level input current	V _{CC} =5.25V, V _I =1	0V			0.1	mA
l _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I = 4.5V			·3.1	6.2	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V . V _I =0	V		4.9	9.8	mA

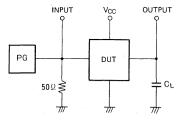
^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

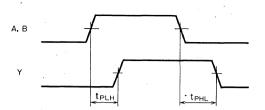
$\textbf{SWITCHING} \ \ \textbf{CHARACTERISTICS} \ \ (\lor_{CC} = 5 \lor , \ Ta = 25 °C, \ \ unless \ otherwise \ noted)$

Symbol	Parameter	Test conditions		Limits		Unit
Symbol l'arameter	rest conditions	Min	Тур	Max	Onit	
tpLH	Low-to-high-level output propagation time	O - 15 p 5 (No. 10)		7 ·	22	ns
t _{PHL}	High-to-low-level output propagation time	C _L =15pF (Note 2)		7	22	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characterstics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS37P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan-out ($I_{OL} = 24mA$, $I_{OH} = -1.2mA$)
- High breakdown input voltabe $(V_1 \ge 15V)$
- Low power dissipation (P_d = 17.5mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

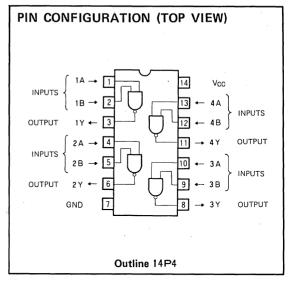
FUNCTIONAL DESCRIPTION

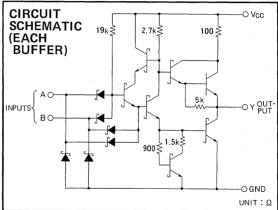
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When inputs A and B are high, output Y is low, and when one or both inputs are low, Y is high.

FUNCTION TABLE

Α	В	Υ
L	L	Н
н	L	Н
L	Т	Н
Н	Н	L





MAXIMUM ABSOLUTE RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	· V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~+150	°C



QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C	Symbol Parameter		Limits			Unit	
Symbol			Min	Тур	Max	Omit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≥2.7V	0		-1.2	mA	
	Low-level output current	V _{0L} ≤0.4V	0		12	mA	
loL	Low-level output current	V ₀ L≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

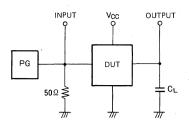
			Total and disions		Limits		
Symbol	Parameter	Test conditions		Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} :	= - 18mA			-1.5	V
Voн	High-level output voltage	$V_{CC} = 4.75V, V_1 = 0.8V, I_{OH} = -1.2 \text{mA}$		2.7	3.4		V
		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =24 mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =	2.7V			20	μА
Іін	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V ₀ =0V		- 30		-130	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			0.9	2	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	= 4.5V		6	12	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

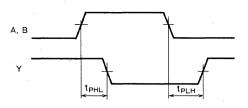
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	r al affeter	rest conditions	Min	Тур	Max	Oilit
t _{PLH}	Low-to-high-level output propagation time	C _L =45pF		7	24	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		12	24	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_0 = 50Ω .
- (2) C₁ includes probe and jig capacitance.



Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS38P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High fan-out (I_O₁ = 24mA max)
- High breakdown input voltage (V_I ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (P_d = 17.5mW typical)
- High speed (tpd = 14ns typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

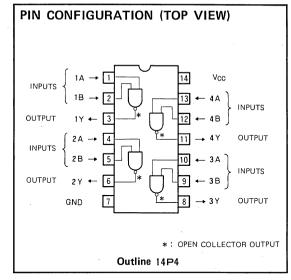
General purpose, for use in industrial and consumer equipment.

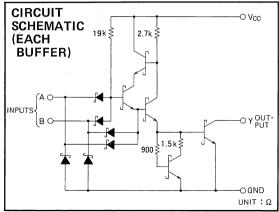
FUNCTIONAL DESCRIPTION

With the use of open collector outputs and SBD inputs having a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates. The maximum low-level output current (I_{OL}) of 24mA makes this device suitable as a buffer gate. When inputs A and B are high, output Y is low and when one or both inputs are low. Y is high.

FUNCTION TABLE

Α	В	Y
L	L	Н
Τ	L	Н
L	I	н
H	Ι	L,





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5∼+15	V-
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

6			Limits			
Symbol	Parame	eter	Min	Тур	Max	Unit
Vcc	Supply voltage	1	4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		250 ⁻	μА
	1 1	V _{OL} ≦0.4V	0		12	mA
IOL Low-level output of	Low-level output current	V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

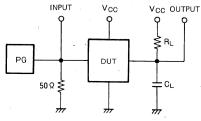
Symbol	Parameter	Tool oon	Test conditions		Limits		Unit
Symbol	Parameter	rest con	artions	Min	Тур.*	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage		•			0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
Гон	High-level output current	V _{CC} =4.75V, V _I =0.	$V_{CC}=4.75V, V_1=0.8V, V_0=5.5V$			250	μΑ
\/-·	Low-level output voltage	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =24mA		0.35	0.5	· V
1	High-level input current	V _{CC} =5.25V, V _I =2.	7 V			20	μА
ин	riigirioverinput current	V _{CC} =5.25V, V _I =10	V			0.1	. mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA ·
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V	V _{CC} =5.25V, V _I =0V		0.9	2	mA
lock	Supply current, all outputs low	V _{CC} =5.25V, V _I =Op	en .		6	12	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

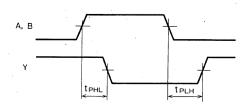
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	i alanietei	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	R _L =667Ω		13	32	ns
t _{PHL}	High-to-low-level output propagation time	C _L =45pF (Note 1)		14	28	ns

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- (2) CL includes probe and jig capacitance.



DUAL 4-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS40P is a semiconductor integrated circuit containing 2 built-in quadruple-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan out ($I_{OL} = 24mA$, $I_{OH} = -1.2mA$)
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d =9mW typical)
- High speed (tpd = 14ns typical)
- Low output impedance
- Wide operating temperature range (Ta = $-20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

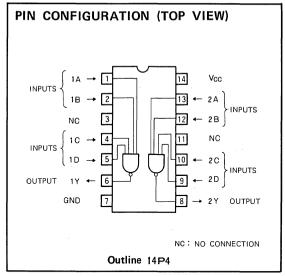
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

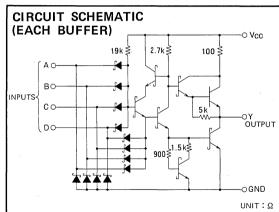
When all inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

Α	N	Υ
L	L	Η
• н	L	н
L	н	Н
Н	н	L

N=B·C·D





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
VI	Input voltage		−0.5∼+15	· V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

DUAL 4-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

				Limits					
Symbol	Para	meter	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	V			
Іон	High-level output current	V _{OH} ≥2.7V	0	-	-1.2	mA			
		V _{OL} ≦0.4V	0		12	mA			
lor	Low-level output current	V ₀ L≦0.5V	0		24	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0		_			Limits		Unit
Symbol	Parameter	Test cor	nditions	Min	Typ*	Max	Unit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	٧
VoH	High-level output voltage	V _{CC} =4.75V, V ₁ =0	.8V, I _{OH} =-1.2mA	2.7	3.4		٧
		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =24mA		0.35	0.5	٧
1		V _{CC} =5.25V, V _I =2.	7V			20	μΑ
Іін	High-level input current	$V_{CC}=5.25V$, $V_{I}=10$	V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
los .	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0	V	-30		- 130	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =0	v .		0.45	1	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =0	pen		3	6	mA

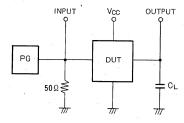
^{* :} All typical values are at V_{CC}=5V, T_a=25°C

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

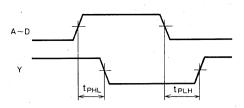
SWITCHING CHARACTERISTICS (V_{CC}=.5V, T_a=25°C, unless otherwise noted)

Symbol	Poromotor	Test conditions		Limits		Unit
0,	Parameter		Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level output propagation time	C _L =45pF		7	24	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		20	24	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P,P}, Z_O = 50\Omega.$
- (2) Ct includes probe and jig capacitance.



BCD-TO-DECIMAL DECODER

DESCRIPTION

The M74LS42P is a semiconductor integrated circuit provided with a BCD-to-decimal decoder function.

FEATURES

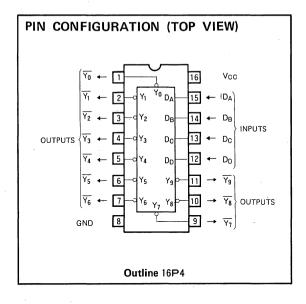
- All outputs set high with reactive input
- Usable as a 3-bit binary/octal decoder
- Wide operating temperature range (T_a=-20~+75°C)

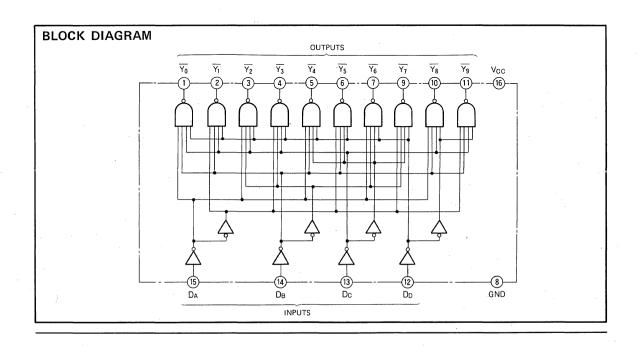
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When inputs D_A , D_B , D_C and D_D are specified in BCD code, the output corresponding to the number among $\overline{Y_0} \sim \overline{Y_9}$ is set low and all the other 9 outputs are set high. When a binary number of 10 or more is applied to $D_A \sim D_D$, all the outputs are set high.







BCD-TO-DECIMAL DECODER

FUNCTION TABLE

Decimal number	D _D	Dc	DB	DA	$\overline{Y_0}$	· <u>Y</u> 1	Y ₂	<u>Y</u> 3	<u>Y</u> 4	<u>Y</u> 5	<u>Y</u> 6	<u>\</u>	Y ₈	Y ₉
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	, L	Н	Н	Н	Н	Н	Н	Н	Н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	н	Н	Н	Н
- 3	L	L	Н	н	Н	H.	н	L	Н	Н	н	Н	Н	Н
4	L	Н.	L	Ļ	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	· L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	н	L	Н	Н	Н
7	L	Н	Н	. н	Н	Н	Н	Ή	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	. н	Н	Н	Н	Н	Н	н	Н	Н	L
10	н	· L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
11	Н	·L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
12	H-	Н	L	L	н	н	н	Н	Н	Н	Н	Н	Н	Н
13	н	н	L	Н	Н	Н	. н	н	H	Н	Н	н	Н	H.
14	н	н	Н	L	Н	н	. н	Н	Н	Н	Н	н	Н.	Н
15	н	I	Ι	Н	I	н	н	Н	Н	Н	Н	Н	Н	Η

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
′VI	Input voltage		-0.5~+15	· V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

				. Limits .					
Symbol	Parame	rter	Min	Тур	Max	Unit			
Vcc	Supply voltage	1	4.75	5	5.25	٧			
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ			
	Loude of sure at a sure	V _{OL} ≦0.4V	0		4	mΑ			
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Task and dis	!		Limits		
Symbol	Farameter	Test condit	ions	Min	Typ *	0.8 -1.5 -0.4 -0.5 -20 -0.1 -0.4	Unit
ViH	High-level input voltage			- 2			V
VIL	Low-level input voltage					0.8	· V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	I8mA			-1.5	٧
V _{ОН}	High-level output voltage	$V_{CC} = 4.75 \text{ V}, V_1 = 0.8$ $V_1 = 2 \text{ V}, I_{OH} = -400$		2.7	3.4		V
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4 mA		0.25	0.4	V
, VOL	Low-level output voltage	$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} =8mA	-	0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V _I =2.7	7 V			20	μΑ
Iн	righ-level input current	V _{CC} =5.25V, V ₁ =10V	V .			0.1	mA
- I _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4	IV			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0	/	-20		-100	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 2)			7	13	mΑ

 $[\]boldsymbol{*}$: All typical values are at VCC $=\!5\,\text{V}$, $T_{a}\!=\!25^{\circ}\text{C}$

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

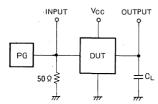
Note 2: I_{CC} is measured with all inputs at 0V.



SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

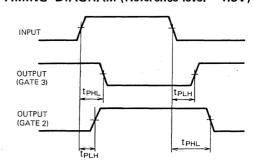
Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output			8	25	ns
t _{PHL}	propagation time, gate 2	C _L =15pF (Note 3)		14	25	ns
tpLH	Low-to-high-level, high-to-low-level output	CL=15pF (Note 3)		12	30	ns
tphL	propagation time, gate 3			12	30	ns

Note 3: Measurement circuit



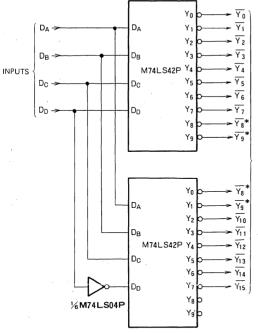
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_O =50 Ω
- (2) C₁ includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



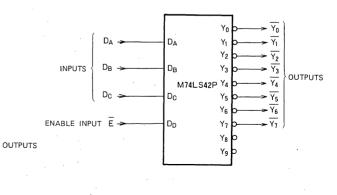
APPLICATION EXAMPLES

(1) 4-bit binary/hexadecimal decoder



Outputs marked with * are provided from both decoders.

(2) 3-bit binary/octal decoder with enable input



M74LS47P

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

DESCRIPTION

The M74LS47P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO outputs for zero suppression.
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

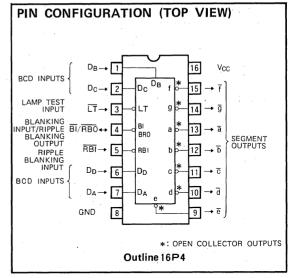
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is designed in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs $\overline{a} \sim \overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a} \sim \overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, thereby making it possible to directly drive a 7-segment LED for the display of anode-common numbers.

Suppression of the high-order unnecessary zeroes is possible by setting the highest order \overline{RBI} ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-order \overline{RBI} for each of the digits. (Refer to the application example.)

By setting blanking input $\overline{\text{BI}}/\overline{\text{RBO}}$ low, outputs $\overline{a}\sim\overline{g}$ are set high and the display element is extinguished irrespective

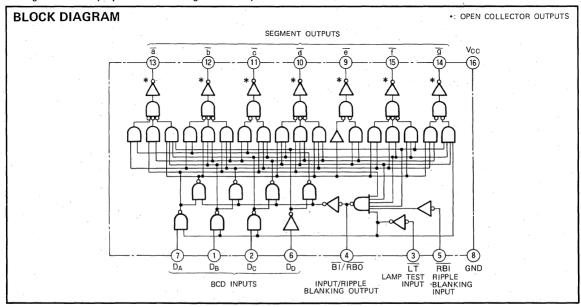


of the status of the other inputs. The luminous intensity can be controlled by applying pulses.

Since $\overline{\text{BI/RBO}}$ serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input \overline{LT} low, $\overline{a} \sim \overline{g}$ are set low irrespective of the status of $\overline{BI/RBO}$, D_A , D_B , D_C and D_D , all the segments in the display element are lighted and each segment can be tested.

Except for that pins 6 and 9 differ in character from the M74LS47P has exactly the same functions, pin connections and characteristics as the M75LS247P.



BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	D _D	Dc	DB	DA	BI/	RBO	a	<u>b</u> .	C	d	ē	f	g	Note
0	Н	Н	L	L	L	L		Н	L	L	L	L	L	L	Н	
1	Н	Х	L.	L	L	Н		Н	Н	L	L	Н	Н	Н	Н.]
2	Н	X	L	L	Н	L		Н	L	L	Н	L	L	Н	L	1
3	Н	Х	L	L	Н	Н		Н	L	L	L	L	Н	Н	L	
4	Н	X	L	Н	L	L		Н	Н	L	L	Н	Н	L	L	
5	Н	Х	L	Н	L	Н		Н	L	Н	L.	L	Н	L	L	
. 6	Н	Х	L	Н	Н	L		Н	Н	H	L	L	L	L	L	
7	Н	Х	L	Н	Н	Н		Н	L	L	L	Н	Н	Н	Н	(1)
8	Η,	Х	Н	L	L	L		Н	L	L	L	L	L	L	L	
9	Н	Х	Н	L	L	Н		Н	L	L	L	Н	Н	L	L	
10	Н	Х	Н	L	Н	L		Н	Н	Н	Н	L	L	Н	L	
11	Н	X	Н	L	Н	Н		Н	Н	Н	L	L	Н	Н	L	
12	Н	Х	Н	Н	L	L		Н	Н	L	Н	Н	Н	L.	L	
13	Н	Х	Н	Н	L	Н		Н	L	Н	Н	L	Н	L	L	
14	Н	Х	Н	Н	Н	L		Н	Н	Н	Н	L	L	L	L]
15	Н	Х	Н	Н	Н	Н		Н	Н	Н	Н	Н	Н	Н	Н	1
Blanking	X	X	Х	Χ.	Х	X	L		Н	Н	Н	Н.	Н	Н	Н	(2)
Ripple blanking	Н	L	L.	L	L	L.		L	Н	Н	Н	Н	Н	Н	Н	(3)
Lamp test	·L	X	Х	X	Х	Х		Н	L	L	L	L	L	L	L	(4)

Note 1. (1) LT is normally kept in high

RBI is kept open or in high with a decimal 0 output.

(2) When BI/RBO is low, all the segment outputs are high irrespective of the status of the other inputs.

(3) All the segment outputs are set high and $\overline{BI/RBO}$ is set low when \overline{LT} is high and \overline{RBI} , D_A , D_B , D_C and D_D are low.

(4) When LT is low, all the segment outputs are low.

X: Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	_6	7	8	9	10	11	12	13	14	15
Character	CD	!	3	3	-:-	5	5		00	٠.	ט		U		는	

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol		Parameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vi	Input voltage	Input BI/RB0		-0.5~V∞	\ \ \
· VI	Input voltage	Other inputs		-0.5~+15	V
Vo	Output voltage	Output BI/RBO	High-level state	-0.5~ V _C C	V
	Output vortage	Other outputs	rign-ievel state	-0.5~+15	V
lo(peak)	Output current		tw≤1ms, dutycycle≤10%	200	mA
10	Output current		High-level state	1	mΑ
Topr	Operating free-air amb	ient temperature range		-20~+75	°C
Tstg	Storage temperature range			−65~ + 150	°C

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

6	D			Limits		Unit
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage	,	4.75	5	5.25	٧
Іон .	High-level output current, outputs ā ~ g	V _{OH} = 15 V	0		250	μА
Юн	High-level output current, output BI/RBO	V _{OH} ≥ 2.4 V	0		-50	μА
	Low-level output current,	V _{OL} ≤0.4V	0		12	mA
loù	outputs $\overline{a} \sim \overline{g}$	V _{OL} ≦0.5V	0		24	mA-
	Low-level output current,	V _{OL} ≤0.4V	0		1.6	mA
lor	output BI/RBO	V _{OL} ≦0.5V	0		3.2	mA _.

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

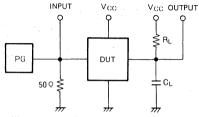
Symbol	Parameter		Test condit	ione		Limits		Unit
Symbol	Farameter		Test conditions		Min	Typ *	Max	OIIIL
ViH	High-level input voltage	-			2			V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage	-	V _{CC} =4.75V, I _{IC} =-18	BmA			- 1.5	٧
Voн	High-level output voltage, output	BT/RBO	V _{CC} =4.75V	$I_{OH} = -50\mu A$	2.4	4.2	5.50	V
ј Іон	High-level output current, outputs	ā∼g	$V_1 = 0.8 V$, $V_1 = 2 V$	V _O = 15 V			250	μΑ
1.	·	Outputs a ~ q		I _{OL} = 12 mA		0.25	0.4	1
1/	Low-level output voltage	Outputs a ~ y	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	· v
VoL	Low-level output voltage	Outputs BI/RBO	$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} = 1.6mA		0.25	0.4	. •
		Outputs B1/ NBO		I _{OL} =3.2mA		0.35	0.5	
1	High-level input voltage, except in	out DI / DBO	$V_{CC}=5.25V, V_{I}=2.7V$	<i>i</i> .			20	μΑ
ΙΗ	riigii-lever iriput vortage, except irip	DUL BI/ NBO	$V_{CC} = 5.25 \text{V}, V_I = 10 \text{V}$				0.1	mA
1	Low-level input current	Input BI/RBO	V	,			— 1. 2 .	mA
lı∟ .	Low-level input current	Other inputs	$V_{CC}=5.25V, V_1=0.4V$,			-0.4	mA
los	Short-circuit output current, output	rt BI/RBO	V _{CC} =5.25V, V _O =0V		-0.3		-2	, mA
lcc-	Supply current		V _{CC} =5.25V (Note 2)			7	13	mΑ

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C. Note 2: I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Taraneter	rest conditions	Min	Тур	Max	, one
tpLH	Low-to-high-level, high-to-low-level output propagation	B 0050		35	100	ns
t _{PHL}	time, from input D_A to outputs $\overline{a} \sim \overline{g}$	R _L =665Ω		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF		50	100	ns .
t _{PHL}	time, from input \overline{RBI} to outputs $\overline{a} \sim \overline{f}$	(Note 3)		45	100 .	ns

Note 3: Measurement circuit

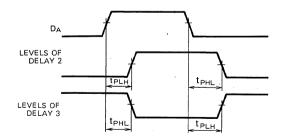


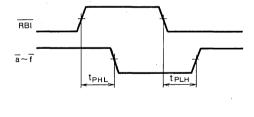
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.



BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

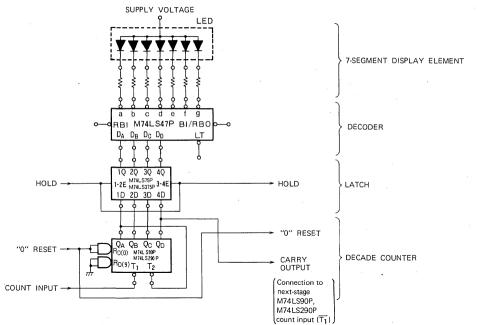
TIMING DIAGRAM (Reference level = 1.3V)



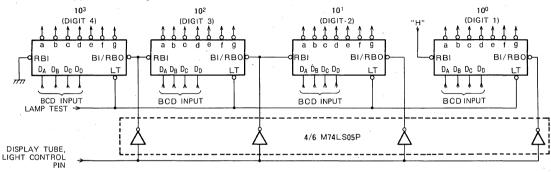


APPLICATION EXAMPLES

(1) Counter using M74LS47P



(2) Zero suppression and light control



M74LS48P

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

DESCRIPTION

The M74LS48P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO output for zero suppression
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- NPN transistor can be externally mounted for Highcurrent drive.
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

This device resembles the M74LS47P without the output transistors and when a number is specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs a~g are set high in accordance with that number. Outputs a~g contain 2Ω pull-up resistors which are suitable for driving common-cathode LEDs. By connecting an NPN transistor to these outputs, it is possible to drive high current display elements.

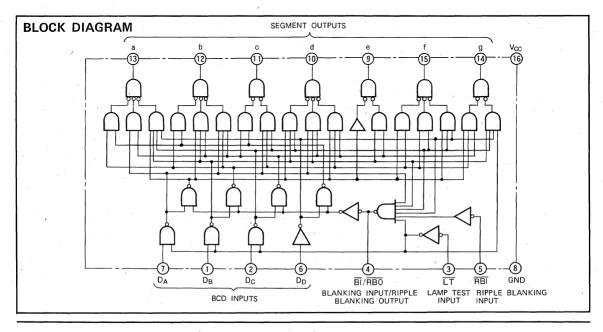
The ripple blanking, blanking and lamp test functions are the same as those for the M74LS47P.

Refer to the M74LS47P for the application example.

Except for that pins 6 and 9 differ in character form the M74LS48P has exactly the same functions, pin connections

PIN CONFIGURATION (TOP VIEW) De. Vcc BCD INPUTS Dc LAMP TEST ĪĪ→ LT BLANKING INPUT/RIPPLE BLANKING BI/RBO↔ OLITPLIT RIPPLE OUTPUTS RRI → RRI DI ANKING Dη 6 BCD INPUTS DΔ DΔ 10 GND Outline 16P4

and characteristics as the M74LS248P.



BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	D _D	Dc	DB	DA	BI/F	BO	a	b	С	d	е	f	g	Note
0	Н	Н	L	L	Ļ	L		Н	Н	Н	Н	Н	Н	Н	L	
1	Н	Х	L	·L	L	Н		Н	L	Н	Н	L	L	L	L]
2	Н	Х	L	L	Н	L		Н	Н	Н	L	Н	Н	L	Н]
3	Н	. X	L	L	н	Н		Н	Н	Н	Н	Н	L	L	Н]
4	Н	Х	L	Н	L.	L		Н	L	Н	Н	L	L	Н	Н	
5	Н	Х	L	Н	L	Н		Н	Н	L	Н	H	L	Н	Н	1
6	Н	Х	L	Н	Н	L		Η	L	L	Н	Н	Н	Н	Н]
7	Н	Х	L	Н	Н	Н		Н	Ĥ	Н	Н	L	L	L	L	(1)
8	Н	X	Н	L	Ŀ	L		Н	Н	Н	Н	Н	Н	Н	Н	
9	.Н	Х	Н	L	L	Н		Н	Н	Н	Н	L	L	Н	Н	
10	Н	Х	Н	L	Н	L		Н	L.	L	L	Н	Н	L	Н	
11	Н	Х	Н	L	Н	Н		Н	L	L	Н	Н	L	L	Н	1
12 '	Н	Х	Н	Н	L	L		Н	L	Н	L.	L	L	Н	Н	1
. 13	Н	Х	Н	Н	L	Н		Н	Н	L	L	Н	L	Н	Н]
14	Н	Х	Н	Н	Н	L		Н	L	L	L	Н	Н	Н	Н	
15	Н	Х	Н	Н	Н	Н		Н	L	L	L	L	L	L	L	1
Blanking	Х	Х	Х	Х	Х	Х	L		L	L	L	L	L	L	L	(2)
Ripple blanking	Н	L	L	L	L	L		L	L	L	L	L	L	L	L	(3)
Lamp test	L	Х	Х	Х	Х	X		Н	Н	Н	Н	Н	Н	Н	Н	(4)

Note 1. (1) LT is normally kept in high.

RBI is kept open or in high with a decimal 0 output.

DEFINITION OF SEGMENTS

- (2) When BI/RBO is low, all the segment outputs are low irrespective of the status of the other inputs.
 (3) All the segment outputs are set high and BI/RBO is set low when LT is high and RBI, DA, DB, DC and DD are low.
- (4) When LT is low, all the segment outputs are high.
- X: Irrelevant



CHARACTERS DISPLAYED

01.7 11.7 10																
Decimal number	0	1	2	3	4	5	6	7	8	9	10	11 .	12	13	14	15
Character		!	2	3	4	5	Ь	٦-	8	or	С	n	U	<u>_</u>	Ł	

ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Para	ameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
.,	Input voltage	Input BI/RBO		-0.5~V _{CC}	V
VI .	input voltage	Other inputs		-0.5∼+15	V
.,	Output valtage	Output BI/RBO	High-level state	-0.5~V _{CC}	V
Vo	Output voltage	Qther outputs	riigii-ievei state	-0.5~Vcc	V
Topr	Operating free-air ambier	nt temperature range		-20~+75	°C
Tstg	Storage temperature rang	je		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

0	D			Limits		Unit
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current, outputs a~ g	V _{OH} ≧2.4V	0		- 100	μА
Іон	High-level output current, output BI/RBO	V _{0H} ≥2.4V	0		-50	μΑ
la.	Low-level output current,	V ₀ L≤0.4V	0		2	mA
loL	outputs a ~ g	V _{OL} ≦0.5V	0		6	mA
	Low-level output current,	V _{OL} ≦0.4V	0		1.6	mA
loL	output BI/RBO	V _{OL} ≤0.5V	. 0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70^{\circ}C$, unless otherwise noted)

0			T-14	***		Limits		11
Symbol	Paramete	ir	rest cond	Test conditions		Тур *	Max	Unit
ViH	High-level input voltage	-		,	2			V
VIL	Low-level input voltage						0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	-18mA			-1.5	V
	High-level output voltage	Outputs a ~ g	V _{CC} =4.75V	I _{OH} = -100 μA	2.4	4.2		V
Voн	r rigit-level output voltage	Output BI/RBO	$V_1 = 0.8V, V_1 = 2V$	$I_{OH} = -50 \mu A$	2.4	4.2		V
Іон	High-level output current	Outputs a ~ g	Vcc=4.75V, V _I =0.8V	$V_1 = 2V_1 V_0 = 0.85V_1$	-1.3	-2		mA
		0		I _{OL} =2mA		0.25	0.4	V
.,		Outputs a ~ g	$V_{CC}=4.75V$	I _{OL} =6mA		0.35	0.5	V
VoL	Low-level output voltage	Output BI/RBO	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =1.6mA		0.25	0.4	V
		Output BI/ NBO		I _{OL} =3.2mA		0.35	0.5	V
	Little Love Control	Inputs BI/RBO	V _{CC} =5.25V, V _I =2.7	7V			20	μА
lіН	High-level input current	other than BI/RBU	V _{CC} =5.25V, V _I =10\	/			0.1	mA ·
1	Lew level input current	Input BI/RBO		11/			-1.2	mA
lıL.	Low-level input current	Other inputs	$V_{CC}=5.25V, V_{I}=0.4$	+ v			-0.4	mA
los	Short-circuit output current	' Output BI/RBO	V _{CC} =5.25V, V _O =0\	/	-0.3		-2	.mA
loc	Supply current		V _{CC} =5.25V (Note 2)			25	38	mA

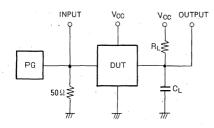
^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

Note 2: I_{CC} is measured with all inputs at 4.5V.

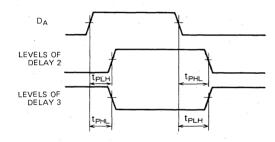
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

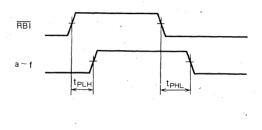
Symbol	D	Total and distance		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Offit .
tpLH	Low-to-high-level, high-to-low-level output propagation	R _L =4kΩ		30	100	ns
tphL	time, from input D_A to outputs a \sim g	C _L =15pF (Note 3)		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =6kΩ		40	100	ns
tphL	time, from input RBI to outputs a ~ f	C _L =15pF (Note3)		45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P.P.}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

DESCRIPTION

The M74LS51P is a semiconductor integrated circuit containing dual 2-wide 2-input/3-input AND-OR-INVERT gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d=5.5mW typical)
- High speed (tpd=7ns typical)
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Schottky TTL technology enables input high breakdown voltage, high speed, low power dissipation and high fan-out.

This device consists of a NOR gate with two 2-input AND gates as the inputs and a NOR gate with two 3-input AND gates as the inputs, and the following logical expressions are yielded:

$$1Y = \overline{1A \cdot 1B \cdot 1C + 1D \cdot 1E \cdot 1F}$$
$$2Y = \overline{2A \cdot 2B + 2C \cdot 2D}$$

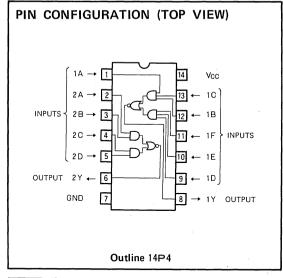
FUNCTION TABLE

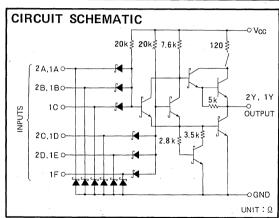
М	N	Υ
L	L	Н
н	L	L
L	Н	L
Н	Н	L

M = 1A • 1B • 1C N = 1D • 1E • 1F AND • OR

M=2A+2B

N = 2C • 2D





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	٧.
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range-		-65~+150	°C

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

	D			Limits					
Symbol	Parame	Min	Тур	Max	Unit				
Voc	Supply voltage	V	4.75	5	5.25	٧			
Іон	High-level output current	V _{0H} ≧2.7V	0.		-400	μА			
	Low-level output current	V ₀ L≦0.4V	0		4	mA			
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

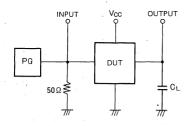
0	Parameter	T	- 124		Limits		
Symbol	Farameter	lest co	Test conditions		Typ *	Max	Unit
ViH	High-level input voltage					-	V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_1 = 0.8V$ $I_{OH} = -400 \mu A$		2.7	3.4		V
1/-	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =2V	I _{OL} =8mA		0.35	0.5	V
L	High-level input current	V _{CC} =5.25V, V _I =2	V _{CC} =5.25V, V _I =2.7V			20	μА
lін	riigirievei input current	V _{CC} =5.25V, V _I =1	0V		,	. 0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0	.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	V _{CC} =5.25V, V _O =0V			— 100	mA .
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0V		0.8	1.6	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4	1.5V		1.4	2.8	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C).

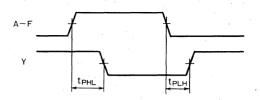
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
6,111661	i di dilietei	rest conditions	Min	Тур	Max] """ .[
tpLH	Low-to-high-level output propagation time	C _L =15pF		6	20	ns
tpHL	High-to-low-level output propagation time	(Note 2)		8	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_r =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance.



Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

M74LS73AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

DESCRIPTION

The M74LS73AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , inputs J and K and direct reset input $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct reset input
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ} C$)

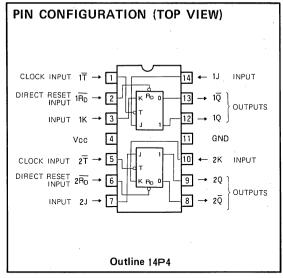
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By setting $\overline{R}_{\overline{D}}$ low, Q and \overline{Q} are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{R}_{\overline{D}}$ must be kept high.

Also available is M74LS107AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 14 and GND at pin 7.



FUNCTIONAL TABLE (Note 1)

Ŧ	R _D	J	К	Q	Q
Х	L	Х	- X	L	П
1	Н	Н	I	Tog	ggle
1	Н	L	Н	L	Н
1	. н	Н	L	н	L
1	H.	L	L	Q ⁰	Q ⁰
Н	Н	×	X	Q^0	Q ⁰

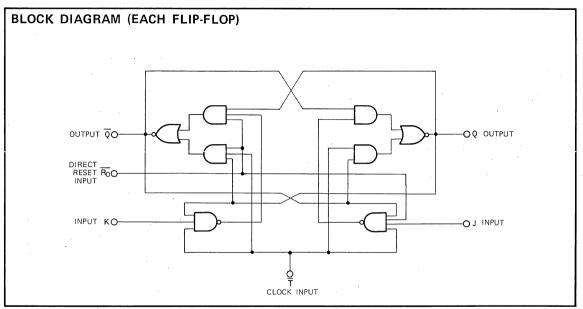
Note 1 \$\displaystyle : Transition from high to low-level (negative edge trigger)

X : Irrelevant

Q0: level of Q before the indicated steady-state input conditions were established.

 $\overline{Q\,0}$: level of \overline{Q} before the indicated steady-state input conditions were established.

Toggle: complement of previous state with \downarrow transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	٧٠
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C ,
Tstg	Storage temperature range		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75℃, unless otherwise noted)

Complete at 1				Limits				
Symbol	Paramete	Min	Тур	Max	Unit			
Vcc	Supply voltage	4.75	5	5.25	٧			
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ		
1	Low-level output current	V _{OL} ≦0.4V	0		4	mA		
OL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		T - 1			Limits		
Symbol	Parameter		Test condit	tions	Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage	nput voltage					0.8	· V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	l8mA			— 1.5	٧
Voн	High-level output voltage	High-level output voltage $ \begin{array}{c} V_{CC} = 4.75 \text{V}, \ \text{V} = 0.8 \text{V} \\ \text{V}_{ =2} \text{V} I_{OH} = -400 \mu \text{A} \end{array} $		2.7	3.4		٧	
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧	
VoL	Low-level output voltage		$V_{i} = 0.8V, V_{i} = 2V$	I _{OL} =8mA		0.35	0.5	٧
	J, K	\\ . F 05\\				20	μА	
	;	R _D	V _{CC} =5.25V V _I =2.7V				. 60	μΑ
	()		7 1-2.70				80	μА
hн	High-level input current	J, K					0.1	mA
		R _D	V _{CC} =5.25V	•			0.3	mA
		T	V _I = 10 ∨				0.4	mA
		J, K	V _{CC} =5.25V				-0.4	mA
h L	Low-level input current	R _D T	V _I =0.4V				-0.8	mΑ
los	Short-circuit output current (Not	e 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
lcc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mΑ

 $[\]boldsymbol{*}$: All typical values are at $V_{CC}\!=\!5\,\text{V},\,T_{a}\!=\!25^{\circ}\!\text{C}$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

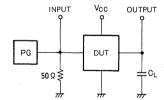
Note 3: Supply current measurements should be done with Q and \overline{Q} set alternately high and \overline{T} should be set low during actual measurement.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Constrat	Parameter	Test conditions	Limits			Unit
Symbol	rai arrietei	lest conditions	Min	Тур	Max	""
fmax	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	,		8	20	ns .
t _{PHL}	time, from T to Q, Q	C _L = 15 pF (Note 4)		6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	20	ns
t _{PHL}	time, from RD to Q, Q			7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

Note 4: Measurement circuit

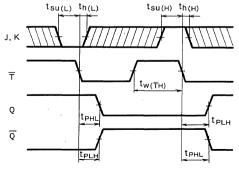


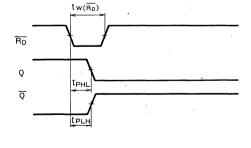
- (1) The pulse generator (PG) has the following characteristics: PRR = $\dot{1}$ MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_o = 50Ω .
- (2) C₁ includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, junless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Зуппьог	. Farameter	rest conditions	Min	Тур	Max	Ont
t _W (₸н)	Clock input \overline{T} high pulse width		20	12		ns
tw(RD)	Direct reset input pulse width		25	4		ns
tr	Clock rise time			650	100	ns
t _f	Clock fall time			900	100	ns
t _{su(H)}	Setup time high T to J, K		20	9		ns
t _{su(L)}	Setup time low T to J, K		20	10		ns
t _{h(H)}	Hold time high Tto J, K		0	– 8		ns
t _{h(L)}	Hold time low T to J, K	1	0	– 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

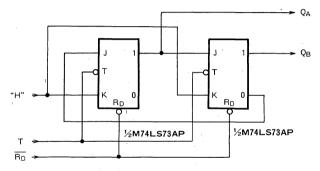


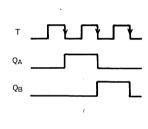


Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

High-speed 1/3 divider





DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS74AP is a semiconductor intergrated circuit containing 2 D-type positive edge-triggered flip-flop circuits with discrete terminals for clock input T, data input D and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Each flip-flop can be used independently.
- Direct set and reset inputs
- Positive edge-triggering
- Q and Q outputs
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and \overline{Q} in accordance with the function table. By using \overline{S}_D and \overline{R}_D , this IC can be made into a direct R-S flip-flop. When both S_D and R_D are low, $Q=\overline{Q}=$ high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a D-type filip-flop, \overline{S}_D and \overline{R}_D must be kept in high.

FUNCTION TABLE

SD	RD	Т.	D.	Q	Q
L	н	X	X	Н	L
Н	L	x.	X	L	Н
L	L	X	Х	н *	н *
Н	Н	L	Х	Q ₀	\underline{Q}_0
Н	Н	t	. н	Н	L
н	H ·	· †	L	L	Н

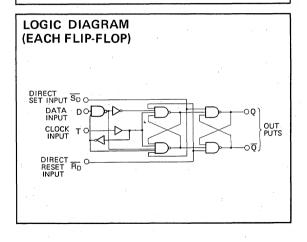


 Q^0 : level of Q before the indicated steady-state input conditions were established.

 $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.

X : Irrelevant

 Nonstable; it will not persist when RD, RD inputs return to their inactive (high) level.



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+5.5	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	. v -
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		· -65~+150	°C .

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Complete				Limits				
Symbol	Paramet	Min	Тур	Max	Unit			
Vcc	Supply voltage	age 4.75	5	5.25	V			
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА		
1		V _{OL} ≤0.4V	0		4	mΑ		
loL	Low-level output current V _{OL} ≤0.5V		0		8	mA		

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75 ℃, unless otherwise noted)

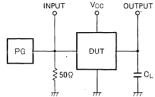
Symbol	Parameter		Tost condi	tions		Limits		Unit
Зуппоот	rarameter		rest condi	Test conditions		Typ*	Max	Oilit
V _{IH} ·	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	BmA			-1.5	V
Vон	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $I_{OH} = -400\mu A$	/, V _I =2V	2.7	3.4		V
VoL	Low-level output voltage		V _{CC} =4.75V I _{OL} =4mA			0.25	0.4	V
• OL	Lew level catput tottage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		D, T					20	
	High-level input current	SD, RD	$V_{CC} = 5.25V, V_I = 2.7V$				40	μΑ
Ιн	riigii-levei input current	D, T	V 5 05V V -40V				0.1	
		SD, RD	V _{CC} =5.25V, V _I =10V	V _{CC} =5.25V, V _I =10V			0.2	mΑ
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	D, T	V	,			-0.4	
l _{IL}	Low-level input current	SD, RD	V _{CC} =5.25V, V _I =0.4V				-0.8	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mΑ
lcc	Supply current		V _{CC} =5.25V, (Note 3)			4	8	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Combal	Symbol Parameter	Test conditions	Limits			Unit
Symbol		rest conditions	Min	Тур	Max	Offic
f _{max}	Maximum clock frequency		25	50		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation			11	25	ns
t _{PHL}	time, from T to Q, Q	C _L =15pF		11	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 4)		8	25	ns
t _{PHL}	time, from $\overline{S_D}$, $\overline{R_D}$ to Q , \overline{Q}			11	40	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

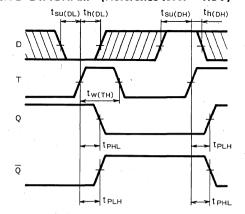
Note 3: Measurement circuit

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

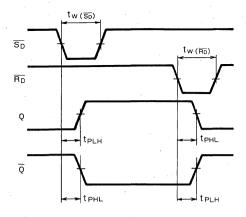
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	D	Test conditions		Limits		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		25	4		ns
tw (SD, RD)	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
t _{su(DH)}	Setup time high D to T		20	10		ns
t _{su(ĎL)}	Setup time low D to T		20	8		ns
th(DH)	Hold time high D to T		5	_ 5		ns
th(DL)	Hold time low D to T		5 .	– 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

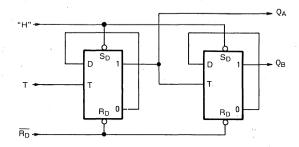


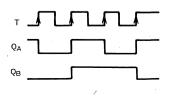
Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.



APPLICATION EXAMPLE

%divider





4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS75P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Ω and $\overline{\Omega}$

FEATURES

- Enable inputs common to two circuits each
- Q and Q outputs
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{\mathbf{Q}}$. When the D signal changes, the signal that appears in outputs Q and $\overline{\mathbf{Q}}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{\mathbf{Q}}$ does not change even if D is changed.

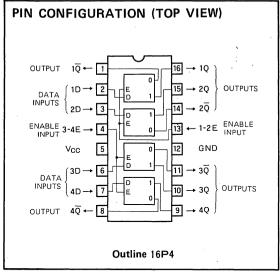
Also provided is the M74LS375P with the same functions and electrical characteristics. With the V_{CC} positioned at pin 16 and GND at pin 8, this device makes for easy mounting.

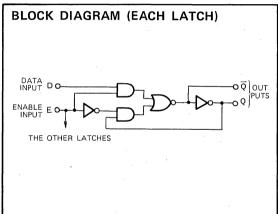
FUNCTION TABLE (Note 1)

E	D .	Q	Q
Н	н	H ·	٦
н	L	L	Н
L	Х	Q ⁰	$\overline{Q^0}$

Note 1 $Q^0,\overline{Q^0}$: Level of Q and \overline{Q} before the indicated steady-state input conditions were established.

X : Irrelevant





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		-65~+150	°C

4-BIT BISTABLE LATCH

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted)

Symbol	Davana			Limits		Unit	
Symbol	Parame	ter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
I _{OH}	High-level output current	V _{OH} ≧ 2.7V	0		- 400	μA	
loL	Low-level output current	V _{OL} ≤0.4∨	. 0		4	mA	
	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75 °C, unless otherwise noted)

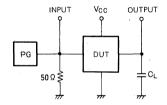
Symbol	Parameter		Test conditions			Limits		Unit	
Зутьог	Taranieter		rest conditions		Min	Typ ★	Max	Unit	
ViH	High-level input voltage	High-level input voltage			2			V	
VIL	Low-level input voltage					1.0	0.8	V.	
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} = - 18m/	Δ .			- 1.5	V	
	High-level output voltage		V _{CC} =4.75V, V _I = 0.8V		2.7	3.5		V V V V V V V A μΑ	
Voн	ringri-rever output vortage		$V_1 = 2V$, $I_{OH} = -400 \mu A$		2.7	3.5		V	
\/-·	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	4 V	
VoL	Low-level output voltage		$V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =8mA	-	0.35	0.5	. V	
		D	V _{CC} = 5.25V	-			. 20		
	High-level input current	E	V _I = 2.7V				80	μΑ	
I _I н	migri-level input current	D	V _{CC} =5.25V				0.1		
	'	E	V _I = 10 V				0.4	mA	
	Low lovel input current	. D	V _{CC} =5.25V				-0.4		
l _{IL}	Low-level input current	E	V _I = 0.4V				-1.6 mA		
108	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O = 0 V		-20		- 100	mA	
· Icc	Supply current	Supply current				6.3	12	mA -	

^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

SWITCHING CHARACTERISTICS (VCC=5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
Symbol	i alametei	rest conditions	Min	Тур	Max	Onit I	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	27	ns	
t _{PHL}	time, from input D to output Q			8	17	ns	
tplH	Low-to-high-level, high-to-low-level output propagation			.10	20	ns	
t _{PHL}	time, from input D to output Q	C _I = 15pF (Note 4)		6	15	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL= 13pr (Note 4)	-	13	27	ns	
t _{PHL}	time, from input E to output Q	•		12	25	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	30	ns	
t _{PHL}	time, from input E to output Q	· · · · · · · · · · · · · · · · · · ·		6	15	ns	

Note 4: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_t = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at OV.

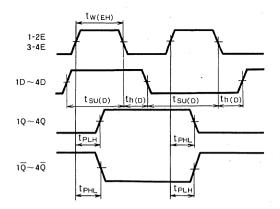
⁽²⁾ C_L includes probe and jig capacitance.

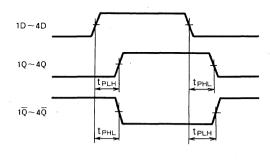
4-BIT BISTABLE LATCH

TIMING REQUIREMENTS (VCC=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Symbol Farameter	rest conditions	Min	Тур	Max	Unit
tw(EH)	Enable input E high pulse width		20	7		ns
tsu(D)	Setup time 1D ~ 4D to E		20	12		ns
th(D)	Hold time 1D ~ 4D to E		8	5		ns

TIMING DIAGRAM (Reference level = 1,3V)





High-level 3-4E, 1-2E

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS76AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , inputs J and K and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each fli-flop can be used independently
- Direct set and reset inputs
- Q and \overline{Q} outputs
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

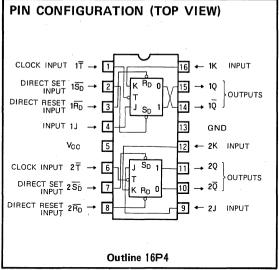
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immmediately before the change emerge in outputs Ω and $\overline{\Omega}$ in accordance with the function table. By using $\overline{S}_{\overline{D}}$ and $\overline{R}_{\overline{D}}$ this IC can be made into a direct R-S flip-flop. When both $\overline{S}_{\overline{D}}$ and $\overline{R}_{\overline{D}}$ are low, $\Omega = \overline{\Omega} = \text{high}$. However, when both of them change to high at the same time, the status of Ω and $\overline{\Omega}$ cannot be anticipated. For use as a J-K flip-flop, $\overline{S}_{\overline{D}}$ and $\overline{R}_{\overline{D}}$ must be kept in high.

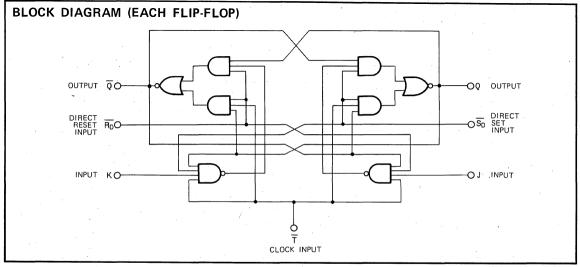
Also available is M74LS112AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 16 and GND at pin 8.



FUNCTION TABLE (Note 1)

Ŧ	SD	R _D	J	K	Q	Q	
X	· L	Н	×	×	н	٦	
Х	н	L	×	×	L	н	
Х	L.	L	X	х	Н*	H*	
↓	Н	H	Н	Н	Toggle		
↓	Н	Η	L	Н	L	Н	
1	Н	Н	н	L	Н	L	
1	Н	I	L	Ŀ	Q ₀	<u>Q</u> 0	
Н -	Н	Ŧ	X .	X	Q ⁰	$\overline{Q^0}$	

- Note 1 \$\preceq\$: Transition from high to low-level (negative edge trigger)
 - X : Irrelevant
 - *: $Q = \overline{Q}$ = high when $\overline{S_D} = \overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and \overline{Q} cannot be anticipated.
 - Q0: level of Q before the indicated steady-state input conditions were established.
 - $\overline{Q0}$: level of \overline{Q} before the indicated steady-state input conditions were established.
 - Toggle : Complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		$-0.5 \sim +7$	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	င
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

				Limits	Max 5.25 — 400	Unit
Symbol	Parame	eter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	. V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
OL	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condit	ions		Limits		Unit
Symbol	raidileter		. rest condit	10/15	Min	Typ *	. Max	Unit
ViH	High-level input voltage		2			٧		
VIL	Low-level input voltage						0.8	٠٧
V _{IC}	Input clamp voltage	Input clamp voltage		BmA			-1.5	. V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		٧
	High-level input current		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	mign-level input current		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		J, K					20	
		$\overline{S_D}, \overline{R_D}$	V _{CC} =5.25V				60	μΑ
		Ŧ	- V _I =2.7V	N			80	
Ιιн	Low-level input current	J, K	V -5 05V				0.1	
		$\overline{S_D}, \overline{R_D}$	V _{CC} =5.25V				0.3	mΑ
		Ŧ	V _I =10V				0.4	
		J, K	V _{CC} =5.25V				-0.4	
I _{IL}	Low-level output voltage	$\overline{S}_D, \overline{R}_D, \overline{T}$	V _I =0.4V (Note 2)				-0.8	mA
los	Short-circuit output current (no	ote 3)	V _{CC} =5.25V, V _O =0V		-20		-100	mΑ
lcc	Supply current		V _{CC} =5.25V (Note 4)			4	6	mA

^{* :} All typical values are at V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	OIII
fmax	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	20	ns
t _{PHL}	time, from \overline{T} to Q , \overline{Q}	C _L = 15pF (Note 5)		7	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	20	ns
t _{PHL}	time, from $\overline{S_D}$, $\overline{R_D}$ to \overline{Q} , \overline{Q}			7	20	ns

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

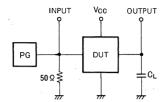
Note 4: Supply current measurements should be done with \overline{Q} and $\overline{\overline{Q}}$ set alternately high and $\overline{\overline{T}}$ should be set low during actual measurement.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

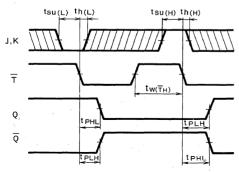
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

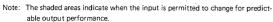
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		20	12		ns
tw(SD, RD)	Direct set, reset pulse width		25	4		ns
tr	Clock rise time			650	100	ns
t f	Clock fall time			900	100	ns
t _{su(H)}	Setup time high J, K to T		20	12		ns
t _{su(L)}	Setup time low J, K to T		20	12		ns
t _{h(H)}	Hold time high J, K to \overline{T}		0	— 10		ns
t _{h(L)}	Hold time low J, K to T	·	0	- 6		ns

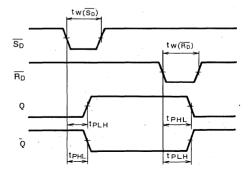
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.







M74LS83AP

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS83AP is a semiconductor integrated circuit containing a 4-bit binary look ahead carry type full adder.

FEATURES

- High speed with look-ahead carry addition
- Possible configuration of systems with partial look-ahead carry
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

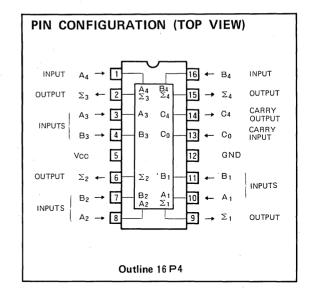
General purpose, for use in industrial and consumer equipment.

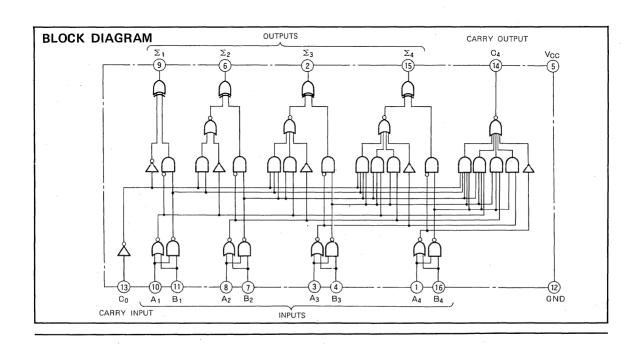
FUNCTIONAL DESCRIPTION

This device performs the addition of two 4-bit binary numbers. When a 4-bit binary number is applied to inputs $A_1 \sim A_4$ and $B_1 \sim B_4$ and the carry signal from the previous digit is applied to input C_0 , the respective bit sum output and carry outputs for the next upper digit appear in outputs $\Sigma_1 \sim \Sigma_4$ and C_4 .

This adder features full internal look ahead across all four bits generating the carry term in 8ns typically. Therefor, the carry output can be obtained in a delay time of 8Nns when N-stages are connected and a 4N-bit parallel adder is configured. (Refer to application example.)

Also available is the M74LS283P with the same functions and electrical characteristics and with a pin 16 V_{CC} and 8 GND configuration.





4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

C _{k-1}	Ak	Bk	Σ_{k}	Ck
L	L	L	L	L
L	Н	Ĺ	н	L
L	L	Н	Н	, L
L	Н	Н	L	Н
Н	L	L	Н	L
ŀН	Н	L	. L	Н
Н	L	Н	L	Н
Н	Н	Ĥ.	Н	Н

Note 1 C_k and Σ_k are the carry output and sum output obtained by adding A_k , B_k and C_{k-1} (carry input), and they are expressed in the following logical expression.

in the following togical expression:
$$\sum_{k} = A_k \oplus B_k \oplus C_{k-1}$$

$$C_k = A_k \cdot B_k + (A_k + B_k) \cdot C_{k-1}$$
Where $k = 1 - 4$

$$\oplus = \text{Exclusive OR}$$
 $+ = \text{OR}$
 $+ = \text{AND}$

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions		Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vı	Input voltage			-0.5∼+15	V
Vo	Output voltage	High-level state		-0.5~ V _{CC}	. V
Topr	Operating free-air ambient temperature range			−20~+75	°C
Tstg	Storage temperature range			- 65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Complete	Devenden			Unit		
Symbol	Paramete		Min	Тур	Max	Oilit
Vcc	Supply voltage		4.75	5	5.25	√V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0	1	8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramet	or	Test condi	tions		Limits		11-1
Symbol	T diditiet	si .	i est condi	itions	Min	Тур*	Max	Unit
V _{IH}	High-level input voltage				2			٧
VIL	Low-level input voltage						0.8	٧
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	٧
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-400µ		2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4,75V	I _{OL} =4mA		0.25	0.4	٧
VOL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		Co	V 5 05V V 0 5V				20	
	High-level input current	A1~A4, B1~B4	V _{CC} =5.25V, V _I =2.7V			40	μΑ	
Ιн	riigirievei iliput current	Co					0.1	
		A1~A4, B1~B4	$V_{CC} = 5.25V, V_{I} = 10V$,			0.2	mA
,	1	Co					-0.4	
IIL .	Low-level input current	A1~A4, B1~B4	$V_{CC} = 5.25V, V_{I} = 0.4$	IV .			-0.8	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _C =0V	/	-20		- 100	mA
		`	V _{CC} =5.25V, V _I =0V	1	,	22	39	mΑ
Icc	Supply current		V _{CC} =5.25V, V _I =0V	, V _I =4.5V (Note 3)		19	34	mA
			V _{CC} =5.25V, V _I =4.	5V		19	34	mA

^{* :} All typical values are at V_{CC}=5V, T_a= 25°C.



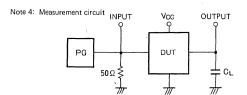
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Measurement should be conducted with inputs $B_1 - B_4$ at 0V and the other inputs at 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

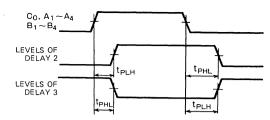
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зупівої	rarameter	rest conditions	Min	Тур	Typ Max 12 24 13 24 9 24 11 24 8 17 8 22	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	24	ns
t _{PHL}	time, from input C_0 to outputs $\Sigma_1 \sim \Sigma_4$			13	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to outputs			9	24	ns
t _{PHL}	$\Sigma_1 \sim \Sigma_4$	C _L =15pF (Note 4)		11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL 1301 (Note 4)		8	17	ns
t _{PHL}	time, from input C ₀ to output C ₄	,		8	22	ns .
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			. 8	17	ns
t _{PHL}	time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to output C_4			8	17	ns



- The pulse generator (PG) has the following characteristics:
 PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_P.P, Z_Q=50Ω.
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

Shown on the right is a 4N-bit binary parallel adder using N number of M74LS83AP devices. The typical delay times of the carry output in this circuit are:

N = 1 (4 bits)

10.5ns

N = 2 (8 bits)

21ns

N = 3 (12 bits)

31.5ns

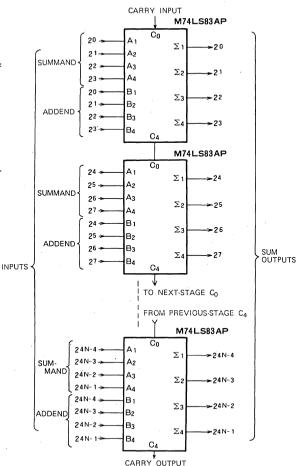
N = 4 (16 bits)

42ns

N = 8 (32 bits)

84ns

This allows a high-speed ripple carry adder to be configured.



DESCRIPTION

The M74LS85P is a semiconductor integrated circuit containing a 4-bit digital comparator.

FFATURES

- Easy expansion of number of bits
- Binary or BCD comparison
- Wide operating temperature range (T_a=-20~+75°C)

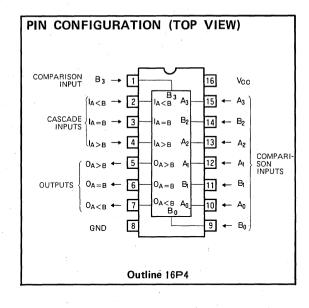
APPLICATION

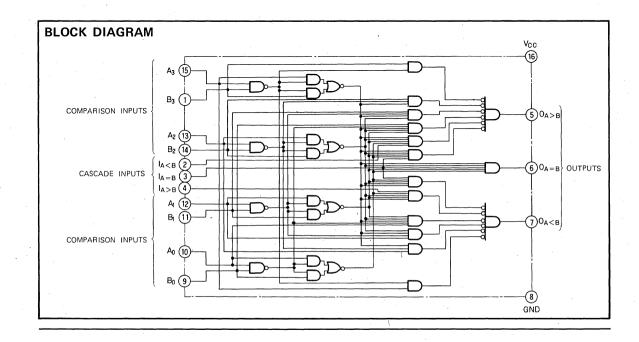
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

By applying two sets of 4-bit binary numbers A and B to be compared to comparison inputs A₀~A₃ and B₀~B₃ and by setting cascade input IA=B high, high appears in outputs $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ in accordance with the magnitude. This is used for connecting cascade inputs $I_{A>B}$, $I_{A < B}$ and $I_{A = B}$ and increasing the number of bits.

(Refer to application example)





FUNCTION TABLE (Note 1)

A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A>B}	I _A <b< th=""><th>I_{A=B}</th><th>O_{A>B}</th><th>O_{A<b< sub=""></b<>}</th><th>O_{A=B}</th></b<>	I _{A=B}	O _{A>B}	O _{A<b< sub=""></b<>}	O _{A=B}
A 3>B 3	Х	Х	Х	Х	×	X	Н	L	٦
A 3 <b 3<="" td=""><td>Х</td><td>Х</td><td>X</td><td>Х</td><td>×</td><td>Х</td><td>L</td><td>Н</td><td>L</td>	Х	Х	X	Х	×	Х	L	Н	L
A 3=B 3	A ₂ >B ₂	Х	Х	Х	×	Х	Н	L	L
A 3=B 3	A 2 <b 2<="" td=""><td>. X</td><td>, X</td><td>Х</td><td>×</td><td>Х</td><td>L</td><td>Н</td><td>L</td>	. X	, X	Х	×	Х	L	Н	L
A 3=B 3	A 2=B 2	A ₁ >B ₁	Х	Х	Х	Х	Н	L	L
A 3=B 3	A 2=B 2	A1 <b1< td=""><td>х</td><td>Х</td><td>×</td><td>Х</td><td>L</td><td>Н</td><td>L</td></b1<>	х	Х	×	Х	L	Н	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A ₀ >B ₀	Х	х	Х	Н	L	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A ₀ <b<sub>0</b<sub>	Х	×	· X	L	Н	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A ₀ =B ₀	Н	L	L	Н	L	L
A ₃ =B ₃	A 2=B 2	A ₁ =B ₁	A ₀ =B ₀	L	Н	L	L	Н	Ļ
A 3=B 3	A 2=B 2	A ₁ =B ₁	A 0=B 0	Х	Х	Н	L	L	Н
A 3=B 3	A 2=B 2	A ₁ =B ₁	A 0=B 0	Н	Н	L	L	L	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A 0=B 0	L	L	L	Н	Н	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		- 65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

	D			Limits				
Symbol	Parame	ter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
	I OL Low-level output current	V _{OL} ≦0.4V	0		4	mA		
1 OL		V _{0L} ≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0 1 1	Danasas		Tost sandi	*:		Limits		Unit
Symbol	Paramet	er	Test conditions .		Min	Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	I8mA			— 1.5	V
Voн	High-level output voltage	1	$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-400 \mu A$		2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} =4mA		0.25	0.4	V
	High level input average	I _A <b, i<sub="">A>B A₀~A₃,B₀~B₃,I_{A=B}</b,>	V _{CC} =5.25V V _I =2.7V				20 60	μΑ
ЧΗ	IIH High-level input current	I _A <b, i<sub="">A>B A₀~A₃,B₀~B₃,I_{A=B}</b,>	V _{CC} =5.25V V _I = 10 V				0.1	mA
liL	Low-level input current	I _A < _B , I _A > _B A ₀ ~A ₃ ,B ₀ ~B ₃ ,I _{A=B}	V _{CC} =5.25V V _I =0.4V				-0.4 -1.2	mA
los	Short-circuit output current (I	Note 2)	V _{CC} =5.25V, V _O = 0 V	/	-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			11	20	mA

* : All typical values are at V_{CC}= 5V, T_a= 25°C.

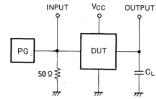
Note 2: All measurements must be done quickly and not more than output should be shorted at a time.

Note 3: I_{CC} is measured with $I_{A=B}$ at 0V and with all other inputs at 4.5V.

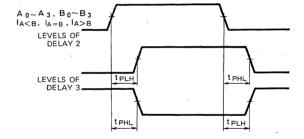
SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C, unless otherwise noted)

	Parameter		Test conditions		Limits		Unit
Symbol	Parameter		, rest conditions	Min	Тур	Max	Oint _
tpLH		Number of delay			6		ns
tpHL	Low-to-high-level, high-to-low-level output propagation time, from	gate steps 1			11		ns
tpLH		Number of delay	7		10		, ns
t _{PHL}	inputs, $A_0 \sim A_3$, $B_0 \sim B_3$ to	gate steps 2			18		ns
t _{PLH}	outputs OA <b, oa="">B</b,>	Number of delay	·		12.	36	ns
t _{PHL}		gate steps 3.	<u>_</u>		20	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level o time, from inputs An A3.Bn B3		C _L = 15pF (Note 4)		16	45	ns
t _{PHL}	OA <b, <math="">O_A = B, $O_A > B$</b,>	to outputs	•		20 '	45	ns
, t _{PLH}	Low-to-high-level, high-to-low-level o				6	22	ns
t _{PHL}	time, from input IA=B to outputs C	0 _{A<b< sub="">, O_{A>B}</b<>}			12	17	ns
.tpLH	Low-to-high-level, high-to-low-level or	utput propagation			7.	20	ns
t PHL	time, from input $I_{A=B}$ to output $O_{A=B}$. 13	26	ns
t _{PLH}	Low-to-high-level, high-to-low-level or	utput propagation			9	22	ns
t PHL	time, from inputs $I_A < B$, $I_A > B$ to o $O_A < B$, $O_A = B$, $O_A > B$	utputs			15	17	ns

Note 4: Measurement circuit

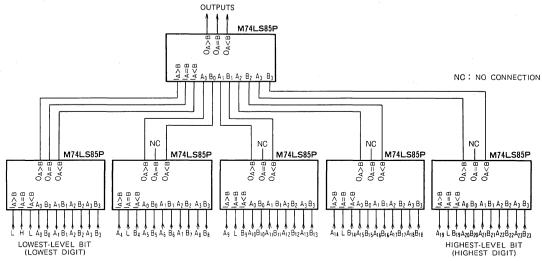


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P =3 V_P -P, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.



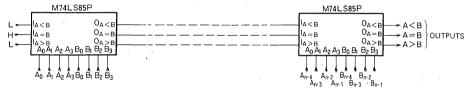
APPLICATION EXAMPLES

(1) Shown below is a 24-bit (digital) comparator using the M74LS85P. Expansion is possible up to n bits using this type of cascade connection.



NC: NO CONNECTION

(2) Shown below is an n-bit comparator using the M74LS85P. The speed is decreases as the number of bits in the configuration below increases. configuration below.



M74LS86P

OUADRUPLE 2-INPUT EXCLUSIVE OR GATES

DESCRIPTION

The M74LS86P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 30.5mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

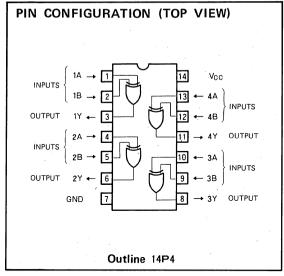
FUNCTIONAL DESCRIPTION

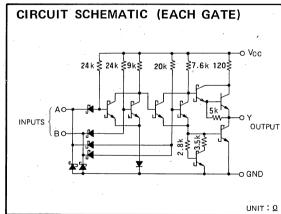
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Y
L	L	L
Н	L	Н
L	H	Н
. н	Н	L





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5 ∼+15	V
V _O	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \,^{\circ}C$, unless otherwise noted)

Cb1	Parameter			Limits				
Symbol	Paramet	ter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
I _{OH} .	High-level output current	V _{OH} ≧2.7V	. 0		-400	μА		
la.	Low-level output current	V _{OL} ≤0.4V	0		4	mA		
OL	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter		T		Limits		
Symbol	Parameter	Test condi	tions	Min	Typ*	Max	Unit
ViH	High-level input voltage						V
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18 mA			- 1.5	V
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.8	IV.				V
VoH	High-level output voltage	$V_1 = 2V$, $I_{OH} = -400 \mu$	Α .	2.7	3.4		V
``	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0 .4	V
VoL	Low-level output voltage	$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} =8mA		0.35	0.5	٧
	High total input accepts	V _{CC} =5.25V, V _I =2.7	V			40	μА
Ιιн	High-level input current	V _{CC} =5.25V, V _I =10	V			0.2	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.8	mΑ
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V	V _{CC} =5.25V, V _O =0V			-100	mA
lcc	Supply current	V _{CC} =5.25V (Note 2).			6.1	10	mA

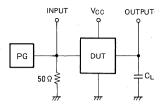
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time. Note 2: Icc is measured with all inputs grounded.

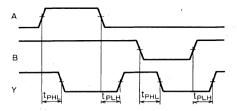
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unia		
Symbol	OI Farameter Test conditions		Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15p F, Other input low (Note 3)		8	23	ns
t _{PHL}	time	GL = 15pF, Other input low (Note 3)		12	17	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O - 15 a F Oahar in the late (Near 2)		8	30	ns
t _{PHL}	time	C _L = 15pF, Other input high (Note 3)		10	22	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



DECADE COUNTER

DESCRIPTION

The M74LS90P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset inputs and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9 set inputs provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (f_{max}=75MHz typical)
- Wide operating temperature range (T_a=-20~+75°C)

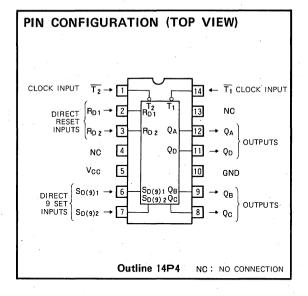
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

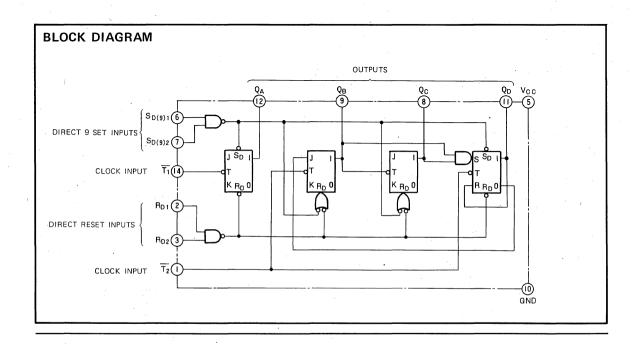
This device consists of independent binary and divide-by-five counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-five counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-five counters can be reset or



set to 9 simultaneously by setting direct reset inputs R_{D1} and R_{D2} high or direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, R_{D1} and/or R_{D2} , and $S_{D(9)1}$ and/or $S_{D(9)2}$, are set low.

Also provided is the M74LS290P with the same functions and electrical characteristics. Its GND positioning at pin 7 and V_{CC} at pin 14 makes for easy mounting.



DECADE COUNTER

FUNCTION TABLE (Note 1)

							,	
Ŧ	R _{D1}	R _{D 2}	S _{D(9)1}	S _{D(9)2}	QΑ	Qв	Qc	QD
Х	Н	Н	L	. X	L	L	L	L
Х	Н	Н	×	L	L	L	L	L
Х	Х	Х	Н	Н	Н	L	L	Н
1	L	Х	L	Х		Co	unt	
1	Х	L	Х	L	Count			
ļ	L	×	Х	L	Count			
Į.	X	L	L	×	Count			

Note 1	- 1	Transition	from	high t	o low

X: Irrelevant

Count	QΑ	Qв	Qc	QD
0	L	L	L	L
1	н	L	L	L
2	L	н	L	L
3	н	н	L	L
4	L	L	Ι	L
5	н	L	Н	L
6	L	. н	н	L
7	Н	н	н	L
8	L	L	L	н
9	н	L	L	Н

⁽¹⁾ Output QA is connected to input B for BCD count.

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	rameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	V
N. Januaritan		Inputs $\overline{T_1}$, $\overline{T_2}$		1
VI	Input voltage	Inputs R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	-0.5~+15	7 °
Vo	Output voltage	High level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \,^{\circ}$), unless otherwise noted)

	Parameter			Limits				
Symbol	rarameter :		Min	Тур	Max	Unit		
Vcc	Supply voltage .		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА		
1)	V _{OL} ≦0.4V	0		4	mA		
lor	· Low-level output current	V _{OL} ≤0.5V	0		- 8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D	arameter	Test con	disi		Limits		Unit
Symbol		arameter	rest con	artions	Min	Typ *	Max	
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	· V
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8$ $V_{I}=2V, I_{OH}=-400 \mu$		2.7	3.4		V
V _{OL} Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA (Note 2)		0.25	0.4	V	
	Low-level output voltage	ver output vortage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA (Note 3)		0.35	0.5	V
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	5 05.1/				20	
		T ₁ .	V _{CC} =5.25V				40	μΑ
	Uinh lough input guarant	T ₂	V _I =2.7V				80	
Ιн	High-level input current	T ₁	V _{CC} =5.25V		_		0.2	A
	·	T ₂	$V_1 = 5.5 V$				0.4	. mA
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V _{CC} =5.25V, V _I =10\	/			0.1	mA
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	\/E 25\/				-0.4	
IIL Low-level inp	Low-level input current	-level input current T ₁	V _{CC} =5.25V				-2.4	mA
		T ₂	V _I =0.4V				-3.2	
los	Short-circuit output curr	ent (Note 3)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

f x: All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 4: I_{CC} is measured with R_{D1} , R_{D2} inputs grounded following momentary connection to 4.5V, and T_1 , T_2 , $S_{D(9)1}$ and $S_{D(9)2}$ inputs grounded



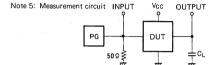
Note 2: Testing of output QA should be conducted with input T2 connected to output QA.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

DECADE COUNTER

SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C, unless otherwise noted)

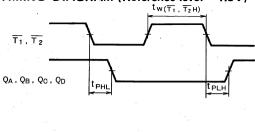
Symbol	Parameter	Test conditions			Unit	
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	75	,	MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B	•	16	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input T ₁ to output Q _A	`.		8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	48	ns
t _{PHL}	time, from input $\overline{T_1}$ to output Q_D			16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input T ₂ to output QB			8	21	ns
t _{PLH}	Low-to-high-output, high-to-low-level output propagation	C _L = 15pF (Note 5)		15	32	ns
t _{PHL}	time, from input $\overline{T_2}$ to output QC	CL - 15 pr (Note 5)		15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		7	32	ns
t _{PHL}	time, from input \overline{T}_2 to output Q_D			8	35	ns
t _{PHL}	High-to-low-level output propagation time, from inputs R_{D1} , R_{D2} to outputs Q_A , Q_B , Q_C , Q_D			17	40	ns
t _{PLH}	Low-to-high-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QA, QD		-	10	30	ns
t _{PHL}	High-to-low-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QB, QC			14	40	ns

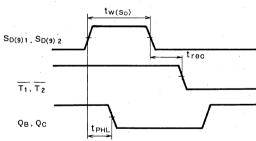


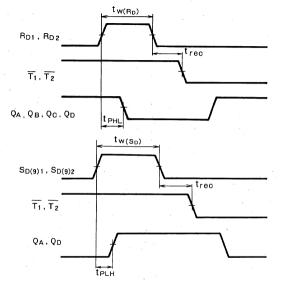
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (Vcc=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Cymbol	1 di diffetei	Test conditions	Min	Тур	Max	Unit
$t_{W(\overline{T_1}H)}$	Clock input T ₁ high pulse width		15	- 6		ns
tw(T2H)	Clock input T ₂ high pulse width	e e	30	17		ns
tw(RD)	Direct reset RD1, RD2 pulse width	:	15	6		ns
tw(SD)	Direct 9 set S _{D(9)1} , S _{D(9)2} pulse width		15	. 8		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(Rp)	Recovery time RD1, RD2 to T1, T2		25	8		ns
t _{rec(s_D)}	Recovery time SD(9)1, SD(9)2 to T1, T2	,	25	8		·ns









DESCRIPTION

The M74LS91P is a semiconductor integrated circuit containing an 8-bit serial input-serial output shift register function

FEATURES

- Synchronous serial input-serial ouptut
- Positive edge-triggering
- Q_7 and \overline{Q}_7 outputs provided
- Wide operating temperature range (T_a=-20~75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

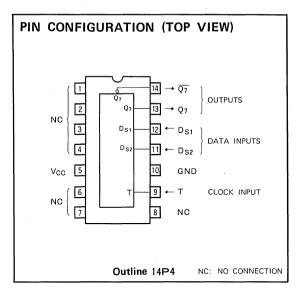
FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered R-S-T flip-flops and the serial data input D_{S1} , D_{S2} and D_{S1} D_{S2} represents the first-stage flip-flop data input.

When D_{S1} and D_{S2} are both high and eight clock pulses are applied to clock input T, the high signal appears in Q_7 and the low signal in $\overline{Q_7}$. When one or more of the inputs is low and the eight clock pulses are applied to T, the low signal appears in $\overline{Q_7}$ and the high signal in $\overline{Q_7}$.

Data reading and shifting operations are performed when T changes from low to high.

Either D_{S1} and D_{S2} should be set low and eight or more clock pulses should be applied to T in order for all the 8 flip-flops to be set low.

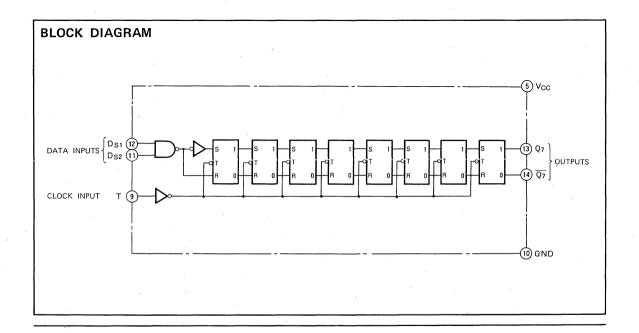


FUNCTION TABLE (Note 1)

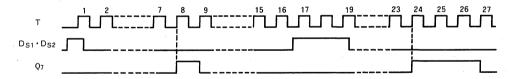
t	n	tn+8	3
D _{S1}	D _{S2}	Q7	Q ₇
L	L	L	. н
L	Н	L	Н
Н	L	. L	Н
Н	Н	Н	L

Note 1 In : Bit time before clock

tn+8: Bit time after 8 clock pulses have been applied



OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	. V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	Parameter		Limits			
Symbol	, Totalice		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА	
		V ₀ L≦0.4V	0		4	mA	
loL	Low-level output current	V ₀ L≦0.5V	0		- 8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T		Limits			Unit
Symbol	Parameter	Test condit	ions	Min	Typ*	Max	Onit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	·V
VoH	High-level output voltage	V _{CC} =4.75V, V ₁ =0.8V V ₁ =2V, I _{OH} =-400μA		2.7	3.5		V
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
*OL	25W 15W 5W pat 15Mags	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
lıн	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μΑ
чн	rigit-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA.
los	Short-circuit output current	V _{CC} =5.25V . V _O =0V (Note 2)		- 20		- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			12	20	mA

 $[\]star$: All typical values are at V_{CC} = 5V, T_a = 25°C



Note 2: All measurements should be done quickly.

Note 3: I_{CC} is measured with D_{S1} and D_{S2} at 0V after 8 clock pulses have been applied to T

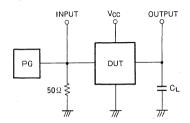
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Cumbal	Symbol Parameter	Test conditions	Limits			11-14
Symbol		rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		10	60.		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15 pF (Note 4)		12	40	ns
t _{PHL}	time, from input T to outputs Q_7 , $\overline{Q_7}$			15	40	ns

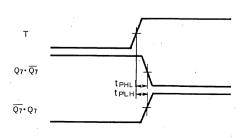
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

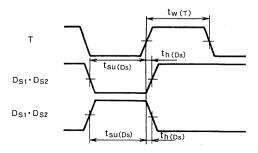
Symbol	Parameter	Test conditions	st conditions Limits			11.3
Зуппьог	raiametei	rest conditions	Min	Тур	Max	Unit
tw(T)	Clock input pulse width		25	6		ns
tsu(Ds)	Setup time D _{S1} , D _{S2} to T		25	7		ns
th(Ds)	Hold time Ds1, Ds2 to T		6	- 0		ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





DIVIDE-BY-TWELVE COUNTER

DESCRIPTION

The M74LS92P is a semiconductor integrated circuit containing an asynchronous divide-by-twelve counter function with direct reset inputs.

FEATURES

- Direct reset input provided
- Usable independently as binary and divide-by-six counter
- High-speed counting (f_{max} = 80MHz typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

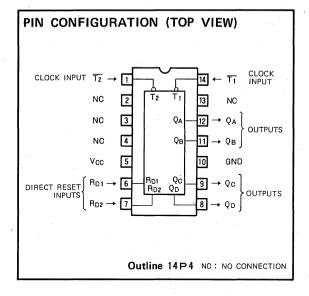
APPLICATION

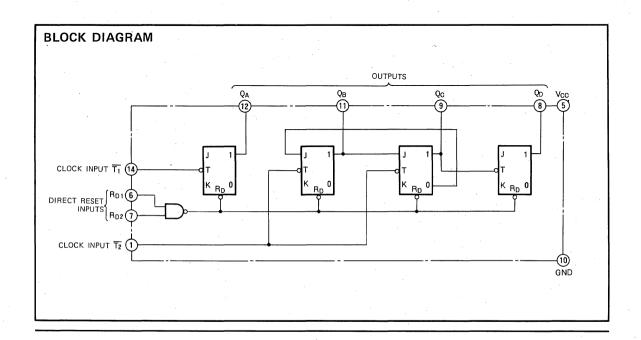
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-6 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-6 counter. When employed as a divide-by-12 counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the output appears in outputs Q_A , Q_B , Q_C and Q_D in accordance with the function table. The code appearing in the output is not pure binary code. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-6 counters can be reset simultaneously by setting direct reset inputs $R_{D\,1}$ and $R_{D\,2}$ high. For use as a counter, either $R_{D\,1}$ or $R_{D\,2}$ or both set low.





DIVIDE-BY-TWELVE COUNTER

FUNCTION TABLE (Note 1)

₹	R _{D1}	R _{D2}	QA	QD				
X	Н	Н	L L L I					
1	L	Н		Co	unt			
1	Н	L	Count					
1	L	L	Count					

Note 1 ↓ : Transition from high to low

X : Irrelevant

Count number	$Q_{\mathbf{A}}$	Qв	Q _C	Q _D
0	L	L	L	L
1	Н	١	L	L
2	L	I	L	L
3	Н	Ι	L	L
4	L	L	н	L
5	Н	L	Н	L
6	L	L	L	н
7	Η	L	L	Н
8	L	Н	L	Н
9	Ξ	Ι	L	Н
10	L	L	Н	Н
1:1	I	, L	I	I

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS

 $(T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage	•	-0.5~+7	V
\/.	V _I Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5	V
VI		Inputs R _{D1} , R _{D2}	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDTIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter			Unit		
Symbol			Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
loH	High-level output current	V _{0H} ≥2.7V	0		-400	μА
		V ₀ L≦0.4V	0		4	mA
loL	Low-level output current VoL≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parame	tor	Test cor	dia:		Limits		Unit
Symbol	Faranie	iter	lest cor	attions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	V
VoH	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
	Low-level output voltage		V _{CC} =4.75V I _{OL} =4mA (Note 2)			0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V, V _I =2V I _{OL} =8mA (Note 2)			0.35	0.5	V
		R _{D1} , R _{D2}					20	
		T ₁	V _{CC} =5.25V, V _I =2.7V				40	μA
	High-level input current	T ₂		ĺ			80	
LIH	riigii-level iliput current	T ₁	Vcc=5.25V, Vi=5.	EV			0.2	
		T ₂	VCC-5.25V, VI-5.	5 V .			0.4	mA
		R _{D1} , R _{D2}	V _{CC} =5.25V, V _I =10	V			0.1	mA
		R _{D1} , R _{D2}					-0.4	
I₁∟	Low-level input current	T ₁	V _{CC} =5.25V, V _I =0.4	4 V.			-2.4	mA
		T ₂					-3.2	
los	Short-circuit output current (Note 3)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC}= 5V, Ta = 25°C.

Note 2: Testing of output Q_A should be conducted with input $\overline{T_2}$ connected to output Q_A ,

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5V.

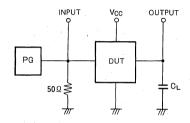


DIVIDE-BY-TWELVE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Oh.ad	Parameter	Test conditions		Limits	-	Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Oint
f _{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	. 80		MHz
f _{max}	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
tpHL	propagation fime, from input $\overline{T_1}$ to output Q_A			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			25	48	ns
tpHL	propagation time, from input $\overline{T_1}$ to output Q_D			25	50	ns
tpLH	Low-to-high-level, high-to-low-level output			7	16	ns
tpHL	propagation time, from input $\overline{T_2}$ to output Q_B			8	21	ns
tpLH	Low-to-high-level, high-to-low-level output	C _L =15pF (Note 4)		8	16	ns
t _{PHL}	propagation fime, from input $\overline{T_2}$ to output Q_C	'		10	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			15	32	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			15	35	ns
t _{PHL}	High-to-low-level output propagation time, from inputs R _{D1} , R _{D2} to outputs Q _A , Q _B , Q _C , Q _D			17	40	ns

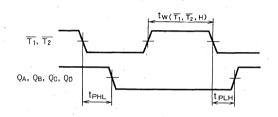
Note 4: Measurement circuit

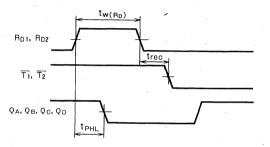


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MNz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P , V_P = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	raiameter	, rest conditions	Min	Тур	Max	Unit
t _W (T₁H)	Clock input T ₁ high pulse width		15	6		ns
t _W (T ₂H)	Clock input T ₂ high pulse width		30	17		ns
tw(RD)	Direct reset R _{D1} , R _{D2} pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(R _D)	Recovery time R _{D1} , R _{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns







DESCRIPTION

The M74LS93P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexadecimal) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max} = 60MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

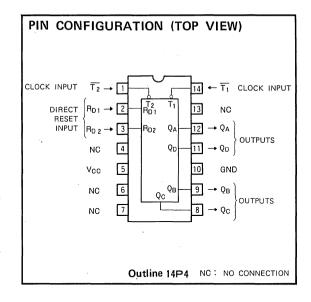
General purpose, for use in industrial and consumer equipment.

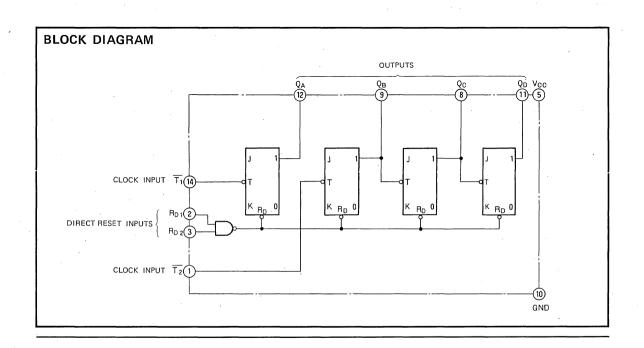
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} or R_{D2} , high. For use as a counter, either R_{D1} or R_{D2} , or both, is set low.

Also provided is the M74LS293P with the same functions and electrical characteristics. Its GND positioning at pin 7 enables easy mounting.





FUNCTION TABLE (Note 1)

T	R _{D1}	. R _{D2}	QΑ	QD				
×	Н	Н	L	. L	L	L		
Ţ	L	Н	Count					
↓	Н	L	Count					
1	L	L	Count					

Note 1 ↓: Transition from high to low

X : Irrelevant

Count number	QΑ	Qв	Qc	QD
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	. L
4 .	L	L	Н	. L
- 5	Н	Ļ	н	L
. 6	L.	H	Н	L
7	Н	Н	Н	. L
8	L.	Ļ	L	н
9	Н	L	L	Н
10	L	н	L	Н
11	Н	Н	L	Н
12	L	L	Н	Н
13	Н	L	Ι	Н
14	L	Н	Н	Н
15	Н	I	Ξ	Ι

Valid when $Q_{\mbox{\scriptsize A}}$ and $\overline{T_{\mbox{\scriptsize 2}}}$ are connected and $\overline{T_{\mbox{\scriptsize 1}}}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
	Vi Input voltage	Inputs T ₁ , T ₂	-0.5~+5.5	.,	
Vı	Input voltage	Inputs RD1, RD2	-0.5~+15	7 °	
Vo	Output voltage	High-level state	-0.5~ Vcc	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75℃, unless otherwise noted)

Complete	P			Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
Vcc	Supply voltage			5	5.25	٧		
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА		
	Low-level output current	V _{OL} ≤0.4V	0		4	mA		
IOL	Low-level output current	V _{OL} ≦0.5V	0		. 8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condit	tions		Limits		Unit
Symbol	rarameter	•	rest condi	LIONS	Min	Typ ∗	Max	Oiiit
VIH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
	High-level output voltage		V _{CC} =4.75V, V _I =0.8	3V	2.7			.,
Voн			$V_1 = 2V$, $I_{OH} = -400 \mu$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V
1/-	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4 mA (Note 2)		0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA(Note 2)		0.35	0.5	V
		R _{D1} , R _{D2}	V _{CC} =5.25V				20	
	High-level input current	T ₁ , T ₂	V ₁ =2.7V	7V			40	μΑ
lіН	High-level input current	T ₁ , T ₂	V _{CC} =5.25V, V _I =5.5	SV.			0.2	mA
		R _{D1} , R _{D2}	V _{CC} =5.25V, V _I =10	V .			0.1	mA
		R _{D1} , R _{D2}	V _{CC} =5.25V				-0.4	
I _{IL}	Low-level input current	T1,	V _{CC} =5.25V V _I =0.4V				-2.4	mA
	T ₂		7 17-0.44				-1.6	
los	Short-circuit output current (N	lote 3)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
loc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

^{* :} All typical values are at V_{CC} = 5V, Ta=25°C.

Note 2: Testing of output Q_A should be conducted with input T_2 connected to output Q_A

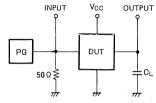
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{I_1}$ and $\overline{I_2}$ at OV after R_{D1} and R_{D2} have been set to OV from 4.5 V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	lest conditions	Min	typ	Max	Onn
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	60		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
t _{PHL}	propagation time, from input $\overline{\Gamma_1}$ to output Q_A			8	. 18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			28	70	ns
t _{PHL}	propagation time, from input T2 to output QB	C∟= 15pF (Note 5)		28	70	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_C			. 8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			15	32	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			22	51	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_D			22	51	ns
t _{PHL}	High-to-low-level output propagation time, from inputs RD1, RD2 to outputs QA, QB, QC, QD			17	40	ns

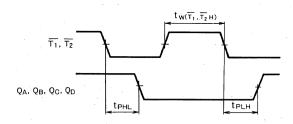
Note 5: Measurement circuit

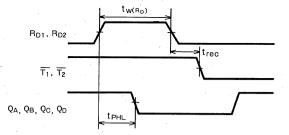


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MNz, t_T = 6ns, t_W = 500ns, V_P = 3 $V_{P\cdot P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0 1 1	D	T		Unit		
Symbol	Parameter	Test conditions	Min ·	Тур	Max	Oùit
t _{W(T1H)}	Clock input T ₁ high pulse width		15	6		ns
t _{W(T₂H)}	Clock input T ₂ high pulse width		30	15		ns
t _{W(RD)}	Direct reset RD1, RD 2 Pulse width		15	- 5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(RD)	Recovery time R _{D1} , R _{D2} to $\overline{T_1}$, $\overline{T_2}$,	25	8		ns





M74LS95BP

4-BIT PARALLEL-ACCESS SHIFT REGISTER

DESCRIPTION

The M74LS95BP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

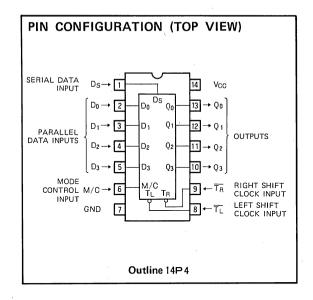
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection.
- Mode control input provided
- Special right and left shift inputs provided
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

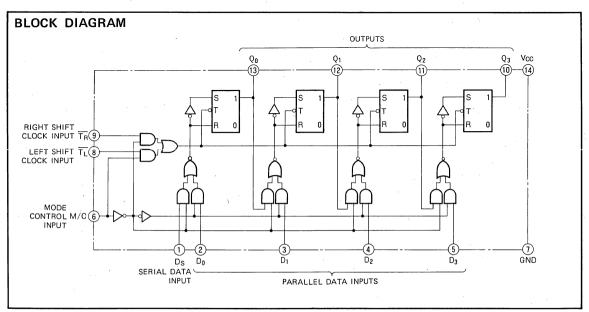
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept at low, the serial data are applied to serial data input Ds and the clock pulse is applied to right shift clock input $\overline{T_R}$, the serial data are shifted sequentially into outputs $Q_0 \sim Q_3$ in synchronization with the clock pulse. When M/C is kept at high, the parallel data are applied to parallel data inputs D₀~D₃ and the 1-bit clock pulse is applied to left shift clock input $\overline{T_L}$, the signals $D_0 \sim D_3$ appear in outputs $Q_0 \sim Q_3$ respectively. When $\overline{T_R}$ and $\overline{T_L}$ change from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high, Q3 is connected to D_2 , Q_2 to D_1 and Q_1 and D_0 , the serial data are applied to D_3 and the clock pulse is applied to $\overline{T_L}$, the device functions as a left shift register. Care should be taken when



switching the M/C signal since the output changes in accordance with the status of $\overline{T_R}$ and $\overline{T_L}$. Refer to the function table.



4-BIT PARALLEL-ACCESS SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operational mode	M/C-	TR	TL	Ds	$D_0 \sim D_3$	Q_0	Q ₁	Q ₂	Q ₃
Right shift	L	1	Х	L	X	L	Q ₀ 0	Q ₁ 0	Q ₂ 0
right shift	L	1	Х	Н	X	Н	Q ₀ 0	Q ₁ 0	Q20
Parallel reading	Н	X	1	X	D ₀ ~D ₃	D ₀	D ₁	D ₂	D ₃
*	1	L	L	X,	X	Q ₀ 0	Q10	Q ₂ 0	Q3 ⁰
	1	L	L	Х	X	Q ₀ 0	Q10	Q ₂ 0	Q30
	1	Н	L	, X	×	Q ₀ 0	Q ₁ 0	Q ₂ 0	. Q ₃ 0
M/C switching	* 1	. н	L	X	X	*	*	*	*
	1	L	Н	X	X	*	*	*	*
	1	L	Н	Х	X	Q ₀ 0	Q10	Q ₂ 0	Q ₃ 0
	1	Н	Н	Х	X	*	*	*	*
	1	Н	Н	X	X	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q ₃ 0

Note 1. ↓: Transition from high to low (negative edge trigger)

 $\ensuremath{\uparrow}$: Transition from low to high (positive edge trigger)

Q0: Level of Q before the indicated steady-state input conditions were established

* : Cannot be predicted

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	, V
VI	Input voltage		-0.5∼+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combat	December			Limits			
Symbol	Parameter	i arameter			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	. 0		-400	μА	
		V _{OL} ≦0.4V	0		4	mA	
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

C	B		T4 dist			Limits		Umia
Symbol	Parame	ter	Test conditi	ons	Min	Typ*	Max	Unit
ViH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V 1
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_1=0.8$ $V_1=2V, I_{OH}=-400\mu A$		2.7	3.4		V
V _{OL}	Low-level output voltage		$V_{CC} = 4.75V$ $I_{OL} = 4mA$ $V_{I} = 0.8V, V_{I} = 2V$ $I_{OL} = 8mA$			0.25	0.4	V
		M/C	V 5 05V V 0 7V				20	
	Uliab lauri in mus aucum	M/C	V _{CC} =5.25V, V _I =2.7V	,			40	μΑ
ин	High-level input current	M/C	V				0.1	
		M/C	$V_{CC} = 5.25V, V_I = 10V$				0.2	mA
1	Low lovel input average	M/C	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
'IL	I _{IL} Low-level input current	M/C	VCC-5.25V, VI=0.4V				-0.8	ıIIA
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mΑ
Icc	Supply current		V _{CC} =5.25V (Note 3)			13	21	mΑ

 $\boldsymbol{*}~:~$ All typical values are at VCC=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with $D_0 \sim D_3$ at 0V, D_S open and M/C at 4.5V after $\overline{T_R}$ and $\overline{T_L}$ have been set from 3V to 0V.

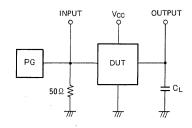


4-BIT PARALLEL-ACCESS SHIFT REGISTER

SWITCHING CHARACTERISTICS (V_{CC}=5V; T_a=25°C, unless otherwise noted)

		T		Unit		
Symbol	Parameter	Test conditions		Тур	Max	Unit
fmax	Maximum clock frequency		. 25	50		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		14	27	ns
tpHL	time, from inputs $\overline{T_R}$, $\overline{T_L}$ to outputs $Q_0 \sim Q_3$			14	32	ns

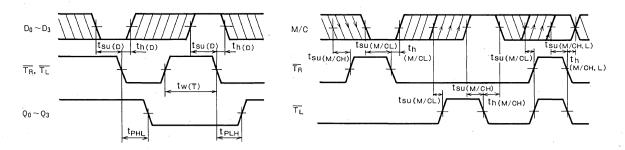
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Constant	D	Test conditions	Limits			Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
t _{W(T)}	Clock input Thigh pulse width		25	8		ns
tf	Clock input T falltime			350	100	ns
t _{SU(D)}	Setup time D to T		20	0		ns
t _{SU(M/CL)}	Setup time M/C low to T		20	14		ns
t _{SU(M/CH)}	Setup time M/C high to \overline{T}		. 20	0		ns
t _h (D)	D hold time to T		10	2		ns
th (M/CL)	Hold time M/C low to T		10	2		ns
th(M/CH)	Hold time M/C high to T].	10	-13		ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

The arrows on the shaded areas indicate the direction for when the input is permitted to change.

DESCRIPTION

The M74LS96P is a semiconductor integrated circuit containing a 5-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

- Positive edge-triggering
- Right shift function
- Asynchronous parallel input provided
- Direct reset input provided
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

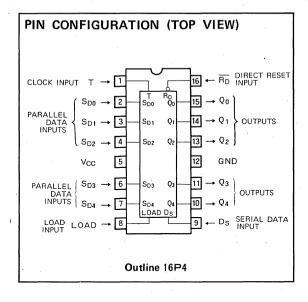
FUNCTIONAL DESCRIPTION

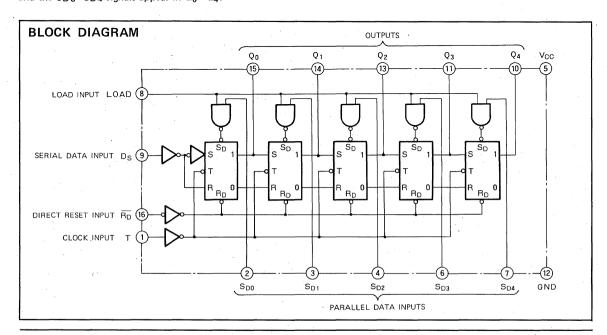
This 5-bit shift register is composed with 4 R-S-T flip-flops and it functions as a serial/parallel inpput-serial/parallel output shift register.

For use as a serial input-serial/parallel output shift register, the load input LOAD or parallel data inputs $S_{D0} \sim S_{D4}$ are kept in high and the data are applied to the serial data input D_S . When a clock pulse is applied to clock input T with D_S in high, the high signal is shifted sequentially to Q_0 , Q_1 ... Q_4 . Shifting is performed when T changes from low to high. When the serial data are applied to $D_{S0} \sim S_{D4}$ and LOAD is set high, the $S_{D0} \sim S_{D4}$ signals appear in $Q_0 \sim Q_4$ respectively irrespective of T.

When direct reset input \overline{R}_D is set low, $Q_0 \sim Q_4$ are set low if LOAD is low irrespective of the other input signals.

When LOAD is high, parallel reading takes precedence, and the $S_{D,0} \sim S_{D,4}$ signals appear in $O_0 \sim O_4$.





FUNCTION TABLE (Note 1) SERIAL INPUT-PARALLEL OUTPUT

	tn	t _{n+1}	tn+2	tn + 3	tn + 4	tn + 5	· tn +6
Ds	L	н.	L	Н	L	H	L
Q ₀	*	L	Н	L	Н	L	Н
Q ₁	*	*	L	Н	L	Н	L
Q ₂	*	*	*	L	Н	L	Н
Q ₃	*	*	*	*	L	Н	L
Q ₄	*	*	*	*	*	L	Н

Note 1: For use as a serial input-parallel output, LOAD, S_{D0}, S_{D1}, S_{D2}, S_{D3} and

 S_{D4} are all kept at low and \overline{RD} is kept at high.

tn: Bit time prior to clock

tn+1: Bit time after application of 1 clock pulse tn+6: Bit time after application of 6 clock pulses

* : Cannot be predicted

PARALLEL INPUT-PARALLEL OUTPUT

LOAD	S _{D(N)}	RD	Q(N)
L	L	L	L
L	L	Н	Q٥
L	Н	L	L
L	Н	Н	Q ⁰
Н	L	· L	L
Н	L	Н	Q ⁰
Н	Н	L	Н
Н	. н	Н	Н

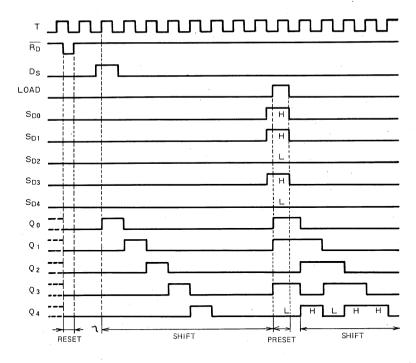
Note 2: For use as a parallel input-parallel output, $\overline{R_D}$ is first set low and kept at high. The parallel input data are input into $S_{DO} \sim S_{D4}$.

The data are read when LOAD is high and they simultaneously appear in the outputs. $\overline{R_D}$ is usually kept at high and LOAD at low.

The "N" in S_{D(N)} refers to 0, 1, 2, 3, 4.

Q⁰ is the level of Q before the indicated steady-state input conditions were established.

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Uniț
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level output	-0.5~V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature		−65∼ + 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parame	•••			Unit	
Зушьы	rarame	ter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0	•	-400	μА
I OL Low-level output curren	Low level output current	V _{OL} ≤0.4V	0		4	mA
	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

C	Parameter		Test and die			Limits		Unit V V V V V V A A
Symbol	rarameter		Test condit	ions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	3mA			-1.5	V
VoH	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	. 3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		LOAD	V _{CC} =5.25V				100	
	High-level input current	Other inputs	$V_1 = 2.7V$				20	μΑ
Ιн	riigirieveriiiput current	LOAD	V _{CC} =5.25V				0.5	
		Other inputs	V _I = 10V				0.1	mA
L	Low-level input current	LOAD	V _{CC} =5.25V				-2.0	
IIL	Low-level input current	Other inputs	V _I = 0.4V			-	-0.4	mA
los	Short-circuit output current (Note 3)		V _{CC} =5.25V, V _O = 0 V		-20		- 100	mΑ
loc	Supply current		V _{CC} =5.25V (Note 4)			12	20	mΑ

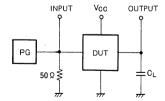
^{* :} All typical values are at V_{CC}=5V, Ta=25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Faranteter	rest conditions	Min	Тур	Max	
fmax	Maximum clock frequency		25	45		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation			12	40	ns
t _{PHL}	time, from input T to outputs $Q_0 \sim Q_4$	C L = 15pF (Note 5)		12	40	ns
tpLH	Low-to-high-level output propagation time, from input SD, LOAD to outputs Q0 \sim Q4			11	35	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs $Q_0 \sim Q_4$			11	35	ns

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time. Note 4: I_{CC} is measured with $\overline{R_D}$ at OV and all the other inputs at 4.5V.

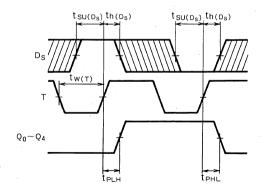
Note 5: Measurement circuit



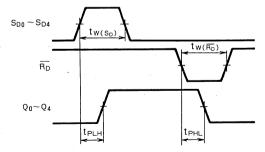
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input T pulse width		20	5		ns
tw(sD)	Parallel data input pulse width		30	5		ns
tw(RD)	Direct reset pulse width		30	5		ns
tsu(Ds)	Setup time D _S to T		30	3		ns
th(Ds)	Hold time D _S to T		5	1		ns







DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS107AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , J and K inputs and direct reset input R_D .

FEATURES

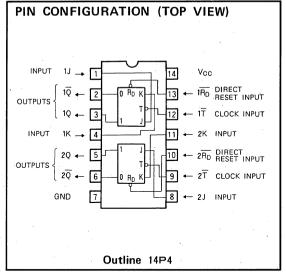
- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct reset input
- Q and Q outputs
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals are read when \overline{T} is "H". When \overline{T} changes from "H" to "L", Q and \overline{Q} transit with the J and K signals to the states described in the function table. By setting \overline{R}_D in "L" state, Q and \overline{Q} become "L" and "H", respectively, irrespective of the states of the other input signals. For use as a J-K flio-flop, keep \overline{R}_D in the "H" state. M74LS107AP is the same as M74LS73AP except for pin configuration.



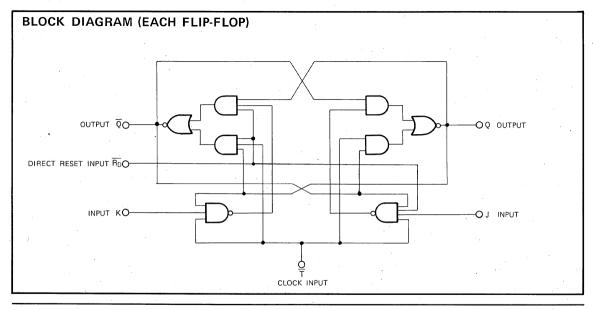
FUNCTION TABLE (Note 1)

T	RD	, J	К	· Q	Q	
X	L	X	, X	L	. н	
. ↓	Н	Н	н.	Toggle		
1	Н	,L	Н	L	Н	
+	Н	Н	L	Н	L	
1	H ·	L	L'	Q0	Q0	
Н	Н	X	Х	Q ⁰	Q ⁰	

Note 1: 1: transition from high to low-level

- X: irrelevant
- Q⁰: level of Q before the indicated steady-state input conditions were established.
- $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.

Toggle: complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		- 65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 ^{\circ}$), unless otherwise noted)

Combat	D			Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≧ 2.7V	0		- 400	μΑ		
IOL Low	Low-level output current	V _{OL} ≦0.4V	0		4	mA		
	Low-level output current	V _{OL} ≦0.5V	. 0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	8		T			Limits		Unit
Symbol	Parameter		Test condi	itions	Min	Тур*	Max	Onit .
VIH	High-level input voltage							V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
VoH	High-level output voltage $ \begin{array}{c} V_{CC}\!=\!4.75 V, V_{I}\!=\!0.8 V \\ V_{I}\!=\!2 V , I_{OH}\!=\!-400 \mu \text{A} \end{array} $		2.7	3.4		V		
\/	Low-level output current		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VoL	Low-level output current		$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} = 8 mA		0.35	0.5	V
-		J, K					20	μΑ
		RD	V _{CC} =5.25V				60	
	High-level input current	Ť	V₁=2.7V				80	
hH,	High-lever input current	J, K					0.1	
		RD	V _{CC} =5.25V				0.3	mA
		Ŧ .	V₁= 10 V				0.4	
		J, K	V _{CC} =5.25V				-0.4	
lıL.	Low-level input current	R _D T	V ₁ =0.4V				-0.8	mA
los	Short-circuit output current (N	ote 2)	V _{CC} =5.25V, V _O =0	I	-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mA

^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25° C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

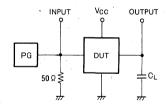
Note 2: I_{CC} is measured with Q and \overline{Q} outputs high in turn. At the time of measurement, \overline{T} input is grounded.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

	T	Limits			Unit
Parameter	lest conditions	Min	Тур	Max	Oiiit I
Maximum clock frequency		30	45		MHz
Low-to-high-level, high-to-low-level output propagation			8	20	ns
time, from input T to output Q, Q	$C_L = 15pF$ (Note 4)		6	20	ns
Low-to-high-level, high-to-low-level output propagation			10	20	ns
time, from input $\overline{R_D}$ to output Q, \overline{Q}			7	20	ns
Company of the Compan	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T} to output Q,\overline{Q} Low-to-high-level, high-to-low-level output propagation	$\label{eq:low-to-high-level} \begin{tabular}{lll} Maximum clock frequency \\ Low-to-high-level, high-to-low-level output propagation \\ time, from input \overline{T} to output Q, \overline{Q} \\ \\ Low-to-high-level, high-to-low-level output propagation \\ \end{tabular}$	Maximum clock frequency Low-to-high-level, high-to-low-level output propagation time, from input T to output Q, Q Low-to-high-level, high-to-low-level output propagation	Parameter Test conditions Min Typ Maximum clock frequency 30 45 Low-to-high-level, high-to-low-level output propagation time, from input \overline{T} to output Q, \overline{Q} CL = 15 pF (Note 4) 8 Low-to-high-level, high-to-low-level output propagation 6	Parameter Test conditions Min Typ Max

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

Note 4: Measurement circuit

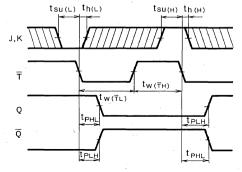


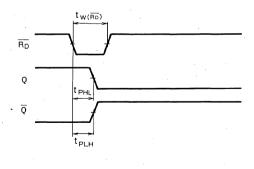
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) C₁ includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5 V, T_a=25°C, unless otherwise noted)

Symbol	Personates	Test conditions	Limits			Unit
Зушьог	Parameter	l est conditions	Min	Тур	Max	Offic
t _{w(TH)}	Clock input T high pulse width		20	12		ns
tw(RD)	Direct reset input $\overline{R_D}$ pulse width	• •	25	4		ns
tr	Clock rise time			650	100	ns
tf	Clock pulse fall time]		900	100	ns
t _{su(H)}	Setup time high J, K to T		20	9		ns
t _{su(L)}	Setup time low J, K to T		20	10		ns
t _{h(H)}	Hold time high J, K to T		0	- 8	·	ns
t _{h(L)}	Hold time low J, K to T] '	0	- 5		ns.

TIMING DIAGRAM (Reference level = 1.3V)

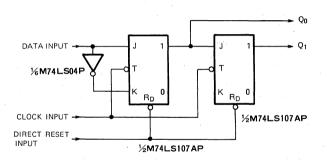


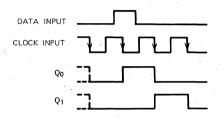


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

2bit shift register





Note 6: Output switching characteristics may not satisfy the ratings if the clock signal is applied without observing the set-up time.



M74LS109AP

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS109AP is a semiconductor integrated circuit containing 2 J \overline{K} positive edge-triggered flip-flop circuits with discrete terminals for clock input T, inputs J and \overline{K} , and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Positive edge-triggering
- Each flip-flop can be used independently
- Direct set and reset inputs
- J and K inputs
- Q and Q outputs
- Wide operating temperature range $(T_a = -20 \sim +75 \circ C)$

APPLICATION

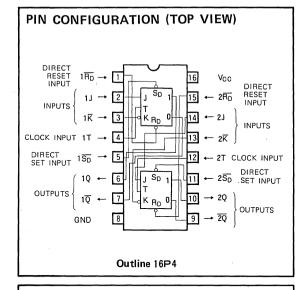
General purpose, for use in industrial and consumer equipment.

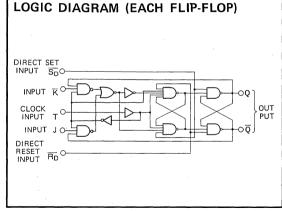
FUNCTIONAL DESCRIPTION

When T changes from low to high, the J and \overline{K} signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, $Q=\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high. By connecting J and \overline{K} , this IC can be used as a D-type flip-flop.

FUNCTION TABLE (Note 1)

S _D	R _D	Т	J	ĸ	Q	Q
L	н	X	×	Х	н	L
Н	L	Х	X	Х	L	Н
L	· L	Х	X	×	н*	, H*
Н	Н	L	Х	Х	Q ⁰	Q ⁰
Н	Н	1	L	L	L	Н
.н	Н	1	Н	L	Tog	ggle
н	Н	↑ ·	L	Н	Q ⁰	Q ⁰
Н	Н	1	Н	Н	Н	L





- Note 1 \uparrow): Transition from low to high-level (positive edge trigger)
 - Q^0 : Level of Q before the indicated steady-state input conditions were established.
 - $\overline{Q^0}$: Level of \overline{Q} before the indicated steady-state input conditions were established. Toggle: complement of previous state with 1 transition of output
 - X : Irrelevant
 - *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D} \text{ are set high, the status of } Q \text{ and } \overline{Q} \text{ cannot be anticipated.}$

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 \, ^{\circ} \! \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+5.5	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature range		-65~+150	°C

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

	Symbol Parameter -			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{0H} ≧2.7V	0		- 400	μΑ		
		V _{OL} ≦0.4V	0		4	mA		
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ		

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

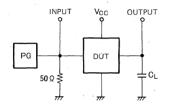
Symbol	Parameter		Test conditi			Limits		Unit
Зушьог	rarameter		rest conditions		Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage		1				0.8	٧
V _{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -1$	I8mA			-1.5	>
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		V
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
			$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} = 8 mA		0.35	0.5	V
		J, K, T	V _{CC} =5.25V, V _I =2.7\				20	μА
Лн	High-level input current	SD, RD	V ₀₀ = 3.23 V, V ₁ = 2.7 V	·			. 40	μд.
чн	riigii level iiiba e caireire	J, K, T	Vcc=5.25V, Vi =10V				0.1	
		SD, RD	VCC=5.25V, VI = 1UV				0.2	mA
I	Low-level input current	J, R, T	V	,			-0.4	^
lı_	Low-level input current	S _D , R _D	$V_{CC} = 5.25 \text{V}, \text{ V}_{I} = 0.4 \text{V}$				-0.8	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O = 0 V	•	- 20		— 100 [°]	· mA
Icc	Supply current		V _{CC} =5.25V, (Note 3)			4	8	mΑ

^{* :} All typical values are at V_{CC}= 5 V, Ta = 25 ℃

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Oilit
fmax	Maximum clock frequency		25	45		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		10	25	ns
t PHL	time, from T to Q, Q			12	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			-11	25	ns
t _{PHL}	time, from $\overline{S_D}$, $\overline{R_D}$ to \overline{Q}			10	40	. ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- $V_p = SV_p P$, $Z_0 = SU_2 Z$. (2) C_1 includes probe and jig capacitance.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

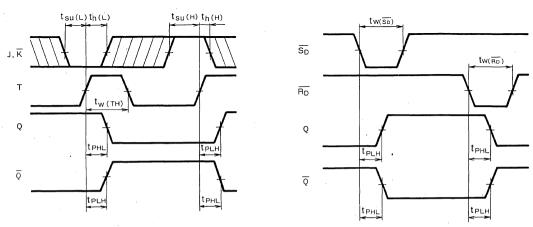
Note 3: The supply current should be measured with Q and \overline{Q} alternately set high and with T set low during actual measurement.

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

TIMING REQUIREMENTS ($V_{CC}=5$ V, $T_a=25$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Faranietei	rest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		25	11		ns
tw(SD.RD)	Direct set, reset pulse width		25	4		ns
t _{su(H)}	Setup time high to T		20	19		ns
t _{su(L)}	Setup time low to T		20	7		ns
t _{h(H)}	Hold time high to T		5	- 2		ns
t _{h(∟)}	Hold time low to T		5	-16		ns

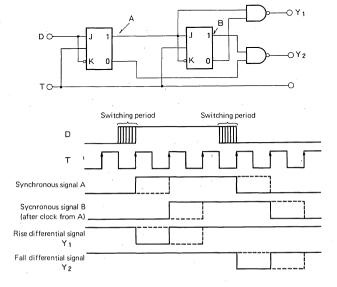
TIMING DIAGRAM (Reference level = 1.3V)



Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Typical circuit for converting asynchronous signal into synchronous signal and rise/fall differential circuit



Note 5: The waveforms indicated by the dotted lines apply when reading with the next clock without observing the set-up time to T.

M74LS112AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS112AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , J and K inputs and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FFATURES

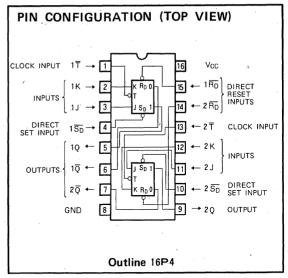
- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals of are read, while \overline{T} is high. When \overline{T} changes from high to low, the signals of J and K immediately before the change appear in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into an direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, $Q=\overline{Q}$ = high. However, when both of them changed to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, keep $\overline{S_D}$ and $\overline{R_D}$ high. M74LS112AP is the same as M74LS76AP except for pin configuration.

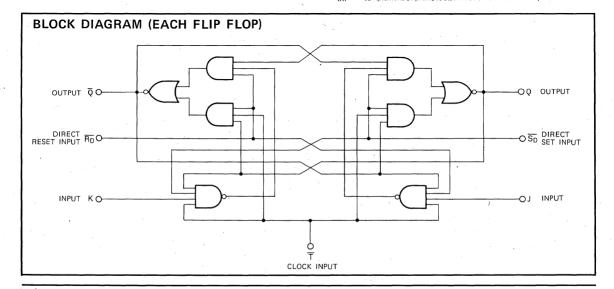


FUNCTION TABLE (Note 1)

Ŧ	SD	\overline{R}_D	J	К	Q	Ō
Х	L.	н	X	Х	Н	L
Х	Н	L	X	. X	L	н
Х	L	L	X	X	H*	Н*
1	н	Н	Н	H	Toggle	
J	. н	. н	L	н	L	Н
1	н.	Н	Н	L	Н	L
1	Н	Н	L	L	Q ₀	Q̄0
Н	Н	Н	Х	х	Q ⁰	Q ⁰

Note 1: \downarrow : transition from high to low-level

- X : irrele vant
- *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D}$ are set high, the status of Q and \overline{Q} cannot be anticipated.
- Q^0 : level of Q before the indicated steady-state input conditions were established. $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established. Toggle: complement of previous state with \downarrow transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits				
Symbol ratameter		:1	Min	Min Typ		Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
		V _{OL} ≦0.4V	0		4	mΑ		
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol			T			Limits		Unit
Symbol	Paramete	Г	Test condi	itions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage				. 2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			1.5	V
.,			V _{CC} =4.75V, V _I =0.8	V	2.7			
V _{OH} .	High-level output voltage		$V_1 = 2V$, $I_{OH} = -400 \mu$	V _I =2V, I _{OH} = - 400 μ A		3.4		V
.,	1 11		V _{CC} =4.75V			0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.8V$, $V_1 = 2V$ $I_{OL} = 8 \text{ mA}$		0.35	0.5	V	
		J,K		1.1.			20	
		SD, RD	V _{CC} =5.25V, V _I =2.7	V			60	μΑ
		Ŧ					80	
Ιн	High-level input current	J,K					0.1	
		SD, RD	V _{CC} =5.25V, V _I =10V				0.3	mA
		Ŧ					0.4	
		J,K					-0.4	
IIL	Low-level input current	SD, RD T	V _{CC} =5.25V, V _I =0.4	V			-0.8	mA
los	Short-circuit output current	(Note 3)	V _{CC} =5.25V, V _O =0V		- 20		100	mA
lcc	Supply current		V _{CC} =5.25V (Note 4)			4	6	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	0,,,,
fmax	Maximum clock frequency	C _L =15pF (Note 5)	30	. 45		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation time from input \overline{T} to output \mathbb{Q} , $\overline{\mathbb{Q}}$			6	20	ns
t _{PHL}				7	20	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{S_D}$, $\overline{\overline{R_D}}$ to output Q , $\overline{\overline{Q}}$			7	20	ns
tphL				7	20	ns

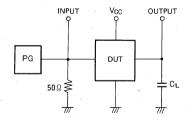
Note 2: S_D and R_D should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, \overline{T} input is grounded.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

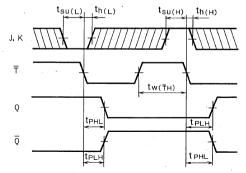
Note 4: Measurement circuit



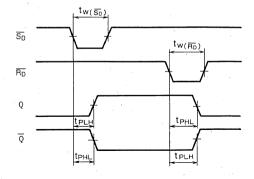
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P =3 V_P -P, Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Syllibol	raidilletei	lest conditions	Min	Тур	Max	Unit
t _W (⊤H)	Clock input Thigh pulse width		20	12		ns
$t_{W(\overline{S_D},\overline{R_D})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
t _r ,	Clock rise time			650	100	ns
tf	Clock pulse fall time			900	100	ns
t _{SU(H)}	Setup time high J , K to \overline{T}		20	12		ns
t _{SU(L)}	Setup time low J, K to T		20	12		ns
th(H)	Hold time high J,K to \overline{T}		0	10		ns
t _{h(L)}	Hold time low J, K to T		0	- 6		. ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



M74LS113AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

DESCRIPTION

The M74LS113AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , inputs J and K and direct set input \overline{S}_D .

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct set input
- Q and Q outputs
- Wide operating temperature range (T_a = −20~+75°C)

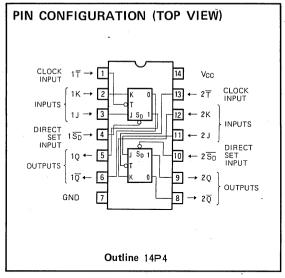
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Ω and $\overline{\Omega}$ in accordance with the function table. By setting $\overline{S_D}$ low, Ω and $\overline{\Omega}$ are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{S_D}$ must be kept high.

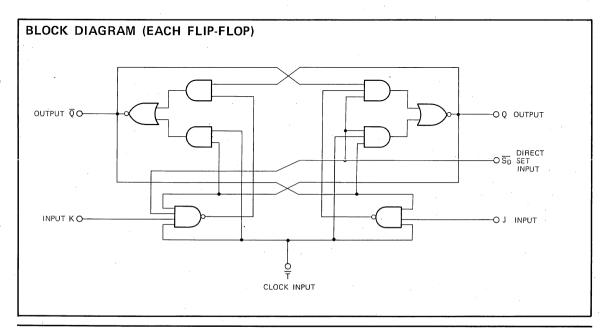
The only difference in functions from M74LS112AP is that this IC has no \overline{RD} input.



FUNCTION TABLE (Note 1)

Ŧ	SD	J	К	Q	ō	
Х	L	X	. X	Н	L	
Į.	Н	Н	Н	Toggle		
. ↓	Н	L	Н	L	Τ	
↓ ↓	Н	Н	L	Н	L	
1	Н	L	L	Q0	<u>Q</u> 0	
Н	Н	Х	X	Q ⁰	Q ⁰	

- 1 👃 : Transition from high to low-level (negative edge trigger)
 - X : Irrelevan
 - Q0: level of Q before the indicated steady-state input conditions were established.
 - $\overline{\mathbb{Q}^0}$: level of $\overline{\mathbb{Q}}$ before the indicated steady-state input conditions were established.
 - Toggle: complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		 -0.5~+7	٧.
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Completed		Parameter			Limits				
Symbol	Paramet	er	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	V			
Гон	High-level output current	V _{OH} ≧2.7V	. 0		-400	μА			
	1	V _{OL} ≦0.4V	0		4	mA			
OL	IoL Low-level output current	V ₀ L≦0.5V	0		8	mA			

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Took oandi			Limits		Unit
Symbol	rarame	tei	lest condi	Test conditions		Typ *	Max	
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage V _{CC} =4.75V, I _{IC} =-18 mA				-1.5	V		
	High-level output voltage		V _{CC} =4.75V, V ₁ =0.8	3V	2.7			
VoH	High-level output voltage		V _I =2V, I _{OH} = -400 µ	$V_{I}=2V$, $I_{OH}=-400 \mu A$		3.4		. V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output vortage		$V_1 = 0.8V . V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	:	J,K					20	
		SD	V _{CC} =5.25V, V _I =2.	7V	,		60	μA
1	Link lavel in a versus	Ŧ					80	
I _{IH}	High-level input current	J,K					0.1	
		SD	V _{CC} =5.25V, V _I =10V	$V_{CC} = 5.25 \text{V}, V_{I} = 10 \text{V}$			0.3	mA
		Ŧ		•			0.4	
		J,K					-0.4	
lıL.	Low-level input current	Low-level input current $\overline{S_D}$ \overline{T}		V _{CC} =5.25V, V _I =0.4V			-0.8	mA
los	Short-circuit output current	Note 2)	V _{CC} =5.25V, V _C =0V		-20		- 100	mΑ
loc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

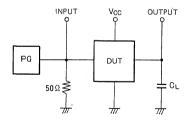
Symbol	Parameter			Unit			
Symbol	Parameter	Test conditions		Min	Тур	Max]. 01110
f _{max}	Maximum clock frequency			30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	15			.8	20 ′	ns
t _{PHL}	time, from T to Q, Q	C _L =15pF (Note 4)			. 7	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(14016 4)			8	20	ns
t _{PHL}	time, from $\overline{S_D}$ to \overline{Q}		· .		7	20	ns

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current measurements should be done with Q and Q set alternately high and T should be set low during actual measurement.

DUAL J.K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

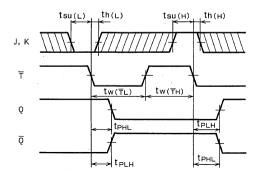
Note 4: Measurement circuit

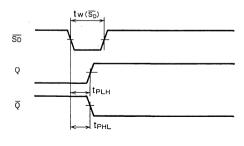


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions			Unit	
Symbol	Parameter	l'est conditions	Min	Тур	Max	Unit
t _W (₹H)	Clock input \overline{T} high pulse width		20	13		ns
tw(s̄₀)	Direct set pulse width		25	10		ns
tr	Clock rise time			650	100	ns
tf	Clock fall time			900	100	ns
t _{SU(H)}	Setup time high J, K to T		20	9		ns
t _{SU(L)}	Setup time low J , K to T		20	12		ns
t _{h (H)}	Hold time high J,K to T		0	-10		ns
t _h (L)	Hold time low J, K to T		0	-5		ns





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET. AND COMMON CLOCK

DESCRIPTION

The M74LS114AP is a semiconductor integrated circuit containing 2 J-K flip-flop circuits with common terminals for clock input T and direct reset input $\overline{R_D}$ and discrete terminals for inputs J and K and direct set inputs $\overline{S_D}$.

FEATURES

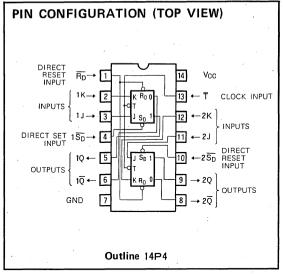
- Negative edge-triggering
- Common clock input and direct reset input
- Discrete direct set input
- Q and Q outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$ this IC can be made into a direct R-S clip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = \overline{Q} = high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.



FUNCTION TABLE (Note 1)

〒	S _D	RD	J	K	Q	Q	
Х	L	. н	×	×	Н	L	
Х	Н	L·	×	×	L	Н	
Х	L	L .	X	Х	Н*	H*	
 	Н	. н	Н	Н	Toggle		
1	Н	Н	L	. н	L	Н	
1	Н	Н	Н	· L	Н	L	
1	Н	Н	L	. L	Q0	Q ₀	

Note 1 ↓ : Transition from high to low-level (negative edge trigger)

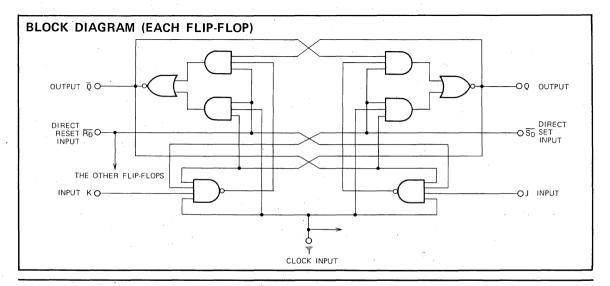
X : Irrelevant

*: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D} \text{ are set high, the status of } Q \text{ and } \overline{Q} \text{ cannot be anticipated.}$

O⁰: Status of output before ↓ change

Q0: level of Q before the indicated steady-state input conditions were established

Toggle: complement of previous state with \downarrow transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ + 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage	,	-0.5~+7	V	
Vı	Input voltage		-0.5~+15	V	
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		−65∼+150	°C	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75$ °C, unless otherwise noted)

Constant	Parameter			Unit		
Symbol	rarameu	ei	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V ₀ L≤0.4V	. 0		4	mA
IoL Low-level ou	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	er	Test condition	nne		Limits		Unit
O y moon	·		rest conditio	7113	Min	Typ *	Max	Unit
V_{IH}	High-level input voltage	,			2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	mA			-1.5	
V _{OH}	High-level output voltage	High-level output voltage		$V_{CC} = 4.75 V, V_{I} = 0.8 V$ $V_{I} = 2 V, I_{OH} = -400 \mu A$		3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
- 5L	2011 level output voltage			I _{OL} =8mA		0.35	. 0.5	V
		J,K		-			20	
	High-level input current	SD	V _{CC} =5.25V, V _I =2.7V				60	μА
		RD					120	
I _{IH}		T	,			160		
'''		J,K					0.1	
		SD	V _{CC} =5.25V, V _I =10V				0.3	
	,	RD	VCC=5.25V, VI=10V				0.6	m∆
	<u> </u>	T					0.8	
		J,K					-0.4	
l _{IL}	Low-level input current	SD	Vac=5 25V Vi=0 4V	(Note 2)			-0.8	
116		R _D Ť	VGC=3.25V, V =0.4V	V _{CC} =5.25V, V _I =0.4V (Note 2)			-1.6	mΑ
os'	Short-circuit output current (Note 3)	$V_{CC} = 5.25V, V_{C} = 0V$		-20		- 100	mA
Icc	Supply current V _{CC} =5.25V (Note 4)			4	6	mA		

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	l arameter	rest conditions	Min	Тур	Max	l omit
fmax	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	20	ns
tpHL	time, from \overline{T} to Q , \overline{Q}	C _L =15pF (Note 4)		7	20	ns .
tpLH	Low-to-high-level, high-to-low-level output propagation			8	20	ns
t _{PHL}	time, from $\overline{S_D}$, $\overline{R_D}$ to Q , \overline{Q}			7	20	ns

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

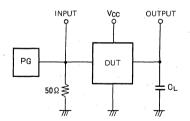
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: Supply current measurements should be done with Q and Q set alternately high and T should be set low during actual measurement.

M74LS114AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET. AND COMMON CLOCK

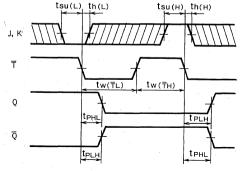
Note 4: Measurement circuit



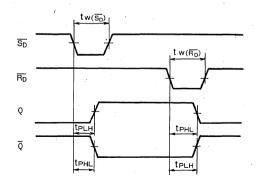
- (1) The pulse generator (PG) has the following characteristics: $PRR = 1 MHz, \, t_r = 6 ns, \, t_f = 6 ns, \, t_w = 500 ns,$
 - $V_{P} = 3V_{P,P}, Z_{O} = 50\Omega.$
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

6	D	Test conditions	Limits			Unit
Symbol	Parameter	l est conditions	Min	Туре	Max	Unit
tw(TH)	Clock input T high pulse width		20	12		ns
$tw(\overline{S_D}, \overline{R_D})$	Direct set, reset pulse width		25	4		ns
tr	Clock rise time	1.		650	100	ns
t f	Clock fall time	1		900	100	. ns
t _{SU (H)}	Setup time high J, K to T	1	20	11		ns
t _{SU(L)}	Setup time low J, K to T	`	20	13		ns
t _{h(H)}	Hold time high J, K to T		0	-11		ns
t _{h(L)}	Hold time low J, K to T	7	0	– 6		ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



DESCRIPTION

The M74LS122P is a semiconductor integrated circuit containing a retriggerable monostable multivibrator circuits with a direct reset input.

FEATURES

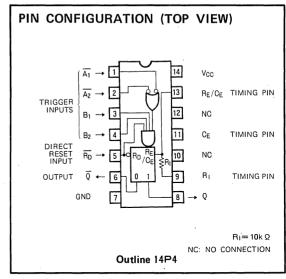
- Long pulse widths can be generated using the retriggerable function.
- Output pulses can be stopped at any time with direct reset inputs.
- A, B complementary inputs provided.
- High breakdown input voltage (V₁ ≥ 15V)
- Q and Q outputs provided
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$
- Internal timing resistance provided (R₁ = 10kΩ)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

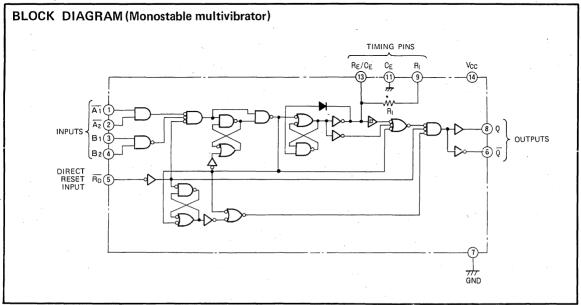
As shown in Fig. 1, the timing pins R_E/C_E and C_E are connected to the external resistance R_T and static capacitance C_T , and when a triggering pulse is applied to inputs $\overline{A_1}$, $\overline{A_2}$ and B_1 or B_2 , a positive pulse appears at output Q, with a negative pulse appearing at \overline{Q} . When the internal timing resistance is used (Fig. 2 (a)), the static capacitance C_T is connected to the C_E and R_E/C_E pins. Thus, connecting the R_1 and V_{CC} pins causes the device to function as a monostable multivibrator and eliminates the need for an external resistance. The width of the pulse (t_w) appearing at output can be controlled by the values for R_T and C_T . (When the internal timing resistance is used, the setting is made with C_T). The trigger is affected by $\overline{A_1}$ or $\overline{A_2}$ switch-



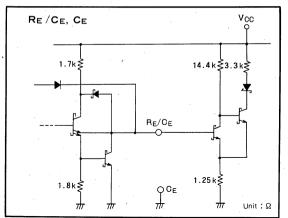
ing from high to low-level, or by B_1 or B_2 switching from low to high.

The retriggering function is used when a wide output pulse width is desired. It is obtained by triggering $\overline{A_1}$ or $\overline{A_2}$, or B_1 or B_2 prior to the pulse being fully output, thus extending its length (See Fig. 2 (b)).

Dropping the direct reset input $\overline{R_D}$ to low-level immediately causes Ω to go low-level and $\overline{\Omega}$ to be set high, regardless of the present output status. This allows the $\overline{R_D}$ signal to be used to shorten the output pulse width to the desired length (See Fig. 2 (c)). A precaution worth noting is that when $\overline{A_1}$ or $\overline{A_2}$ is low-level and $\overline{B_1} = \overline{B_2} = \text{high, and } \overline{R_D}$ is switched from low to high-level, the trigger will be activated changing the status of Ω and $\overline{\Omega}$.



TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

RD	A 1	A ₂	B ₁	B ₂	Q	Q
. L	X	X	Х	X	L	Ŧ
X	Н	н	X	×	L	Н
X	X	X	L;	X	L	н
X	X	X	X	L	L	H
Н	L	Х	1	Н	Л	L
Н	, L	X	Н	1	7	Г
Н .	X	L	1	, H	Л.	7
Н	Х	L,	Н	1	7	
Н	Н	1 ;	Н	Н	7	7
Н	1	. l	H.	Ĥ	7	Ţ
Н	1	Н	Н	Н	7	J
1	L	×	Н	Н	7	7
1	Х	L	Н	Н	\Box	T

Note 1, 1: Transition from low to high (positive edge trigger)

↓ : Transition from high to low (negative edge trigger)

☐: Positive-going one-shot trigger

☐: Negative-going one-shot trigger

X : Irrelevant

OPERATIONAL DESCRIPTION

1. Using the timing pins

Figure 1 shows the timing pins R_E/C_E and C_E connected to the external resistance R_T and static capacitance C_T respectively. An alternate method to connecting R_T is to connect the R_I and V_{CC} Pins together. When a electrolytic capacitor is used as C_T , connect R_E/C_E to the positive (+) side and C_E to the negative (-) side. In this case, the device functions as a TTL IC, and eliminates the requirement for a switching diode. Where noise causes operational problems, connect the C_E pin to GND (located near the 7 pin) as shown by the dashed line in the diagram.

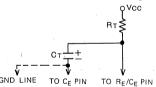


Fig. 1 Connecting External Resistance R_T and Static Capacitance C_T to Timing Pins R_E/C_E and C_E

2. Output Pulse Width tw

Output pulse width t_w is set by the values of R_T and C_T as shown below. When R_1 is used, R_T should equal $10k\Omega.$

- 2-1. When $C_T > 1000 pF$, $t_w = K \cdot R_T \cdot C_T \cdot (1 \pm 0.1) (ns)$. For the value for K, also refer to Typical Characteristics, $K C_T$ characteristics. (The value for R_T does not affect K.)
 - Units for R_{T} and C_{T} are $k\Omega$ and pF respectively.
- 2-2. When $C_T \leq 1000 pF$, refer to the output pulse width vs. C_T , R_T shown in the Typical Characteristics section in back of this specification sheet.

3. Controlling Output Pulse Width

The width of the output pulse can be controlled using three methods, based on the presence or absence of the trigger signal and \overline{R}_{D} signal.

- 3-1. Used as conventional device
 - Figure 2(a) shows the device used in the normal monostable multivibrator mode. Here, output pulse width $t_{\rm w}$ is set using the equations and diagram shown in the above section.
- 3-2. Extending the width of the output pulse by retriggering

Figure 2(b) shows that the output pulse can be extended to any width desired by triggering again before the pulse is fully output.

3-3. Shortening the width of the output pulse by signal

Figure 2(c) shows that the $\overline{R_D}$ signal can be used to terminate the output pulse initiated by the trigger. The output pulse can be shortened to any width desired.

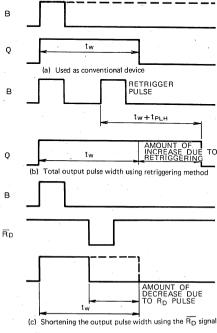


Fig. 2 Output Pulse Width Control

4. Precautions

- 4-1. The retriggering pulse should follow the trigger by $0.22C_T$ (ns), where the unit for C_T is picofarads. During this interval, the retriggering pulse will be ineffective.
- 4-2. The wiring used to connect the external C_T and R_T should be shielded from noise, and be as short as possible (less than 3cm) to minimize line capacitance and noise-induced errors.
- 4-3. Use a capacitor with good high-frequency characteristics and a value of 0.01 to $0.1\mu F$ to connect V_{CC} and GND.
- 4-4. Note that an output pulse will be produced when the power to the device is turned on.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Cumbal	Parameter .					
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Юн	High-level output current	VoH≥2.7V	0		-400	μΑ
lo:	Low-level output current VoL≤0.4V VoL≤0.5V	VoL≦0.4V	0		4	mΑ
loL		0		8	mΑ	
R _T	External timing resistance		5		260	kΩ
Ст	External timing capacitance			No limits		
CR	R _E /C _E pin line capacitance				50	pF

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Constant	D	T		Limits		Unit
Symbol	Parameter	Test conditions	Min	Typ *	Max	
VIH	High-level input voltage		2			٧
VIL.	Low-level input voltage				0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, l _{IC} =-18mA			-1.5	V
Vон	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$	2.7	3.5		
VoL	Low-level output voltage	V _{CC} =4.75V		0.25	0.4	V
1	No.	Vcc=5.25V, Vi=2.7V			20	μΑ
ПН	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mΑ
hL	Low-level input current	Vcc=5.25V, Vi=0.4V			-0.4	mA
los	Short-circuit output current	Vcc=5.25V, Vc=0V	- 20		- 100	mΑ
lcc	Supply current	Vcc=5.25V (Note 2)		6	11	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

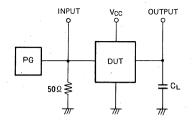


Note 2. I_{CC} is measured with R_E/C_E, C_E open. 4.5V is applied to R_D, A₁, A₂, B₁ and B₂, with the measurement taken after A₁ and A₂ are momentarily dropped to 0V, then raised to 4.5V.

SWITCHING CHARACTERISTICS (Voc=5V, Ta=25°C, unless otherwise noted)

	Parameter	Test conditions		Limits		11-2
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output Q			19	33	ns
t _{PLH}	Low-to-high-level output propagation time, from input B ₁ , B ₂ to output Q			20	44	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output $\overline{\overline{Q}}$	CT=OpF		21	45	ns
t _{PHL}	High-to-low level output propagation time, from input B_1 , B_2 to output $\overline{\mathbb{Q}}$	R _T =5kΩ		23	56	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q	C∟= 15pF (Note 3)		18	27	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output Q]		23	45	ns
twQ(min)	Minimum output pulse width, from inputs $\overline{A_1}$, $\overline{A_2}$, B_1 and B_2 to output Q			70	200	ns
two	Output pulse width, from input \overline{A} , B to output Q	$C_T = 1000 pF, R_T = 10 k \Omega$ $C_L = 15 pF (Note 3)$	4	4.55	5	μs

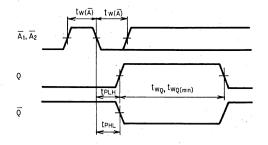
Note 3. Measurement Circuit

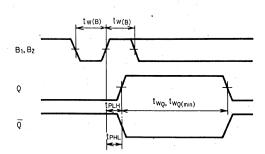


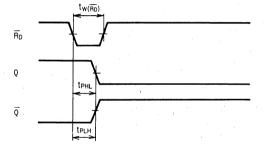
- (1) The pulse generator (PG) has the following characteristics: (1) The pulse generator (PG) has the following charactering PRR = 1MHz (t_{WQ} measurement: 100kHz), t_f = 6ns, t_W = 500ns, V_P = 3V_P, P, Z_O = 50Ω
 (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (Voc=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
- Symbol		Min	Тур	Max	Unit	
$t_{W(\overline{A_1}, \overline{A_2})}$	Trigger A pulse width		40	15		ns
tw(B ₁ , B ₂)	Trigger B pulse width	*	40	10		ns
tw(RD)	Direct reset RD pulse width		40	15		ns



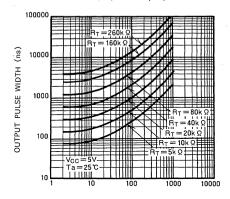




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TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH vs CT, R (C_T≤1000 pF)

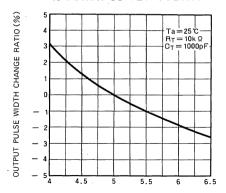


EXTERNAL TIMING CAPACITANCE CT (pF)

K VS CT (C>1000 pF) K (COEFFICIENT TO OBTAIN OUTPUT PULSE WIDTH) 1 0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1

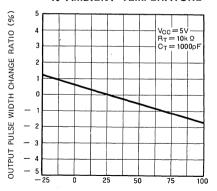
EXTERNAL TIMING CAPACITANCE CT(pF)

CHANGE RATIO OF OUTPUT PULSE vs POWER SUPPLY VOLTAGE



POWER SUPPLY VOLTAGE VCC(V)

CHANGE RATIO OF OUTPUT PULSE vs AMBIENT TEMPERATURE



AMBIENT TEMPERATURE Ta(℃)

DESCRIPTION

The M74LS123P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- A, B complementary inputs provided
- High breakdown input voltage (V₁ ≥ 15V)
- Q and Q outputs provided
- Wide operating temperature range (T_a=-20~+75°C)

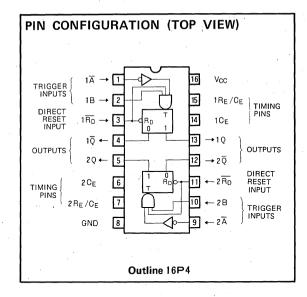
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

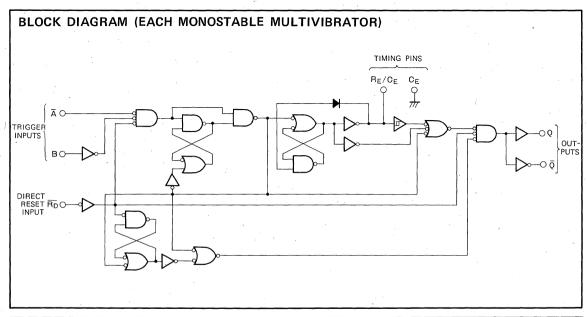
Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1 on the next page, and by applying a trigger from input \overline{A} or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied.

The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from \overline{A} or B immediately before the output pulse is completed, the

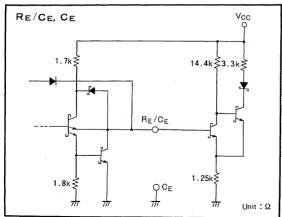


output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and \overline{Q} high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the $\overline{R_D}$ signal. (Fig. 2(c)) When $\overline{R_D}$ changes from low to high with \overline{A} at low and B at high, the trigger is applied and the status of Q and \overline{Q} changes.



TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

$\overline{R_D}$	Ā	В	Q	Q
L	X	X	L	Н
Х	Н	Х	L	Н
Х	X	L	L	н
Н	L	1	TT.	
Н	J	Н		L
1	L	Н	Л	7

Note 1. ↑: Transition from low to high. (positive edge triggering)

↓ : Transition from high to low, (negative edge triggering)

Positive one-shot operation.

☐: Negative one-shot operation.

X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E . Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect C_E to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

 $\begin{array}{c|c} & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & \\ & & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ \end{array}$

Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width tw

The output pulse width tw is set by RT and CT

2-1. When CT is greater than 1000pF

 $t_W = 0.45 \cdot R_T \cdot C_T \text{ (ns)} \times (1 \pm 0.1)$

Refer to K-C_T characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is

brought to K by value of R_T.)

 $R_{\rm T}$ is measured in kilohms and $C_{\rm T}$ in picofarads Depending on the product, fluctuations in the order of 3/-10%may occur.

 R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF

Refer to the output pulse width versus—C_T, R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and \overline{R}_D signal.

3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width t_w can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger func-

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

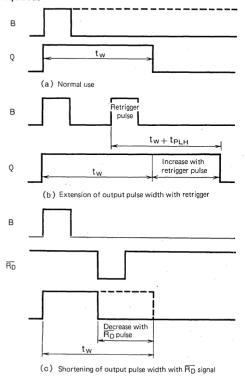


Fig. 2 Output pulse width control

4. Precautions with use

- 4-1. Apply the retrigger pulse after a wait of $0.22C_T$ (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.
- 4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible and avoid signal wires which may be conducive to noise.
- 4-3. Connect an external capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND.
- 4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5∼+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ + 75°C, unless otherwise noted)

Symbol	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$			Limits		Unit	
Syllibol	rarameter		Min	Тур	Max 5.25 -400 . 4 8 260 one	Jill	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
la:		V _{OL} ≦0.4V	0		. ' 4	mA	
'OL		V _{OL} ≦0.5V	0		. 8	mΑ	
RT	External timing resistance		5.		260	kΩ	
Ст	External timing capacitance			No	ne		
CR	RE/CE pin wiring capacitance				50	pF	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Tost and	nditions		Limits		
Зуппоот	i arameter	i est coi	rest conditions		Typ *	Max	Unit
V _{IH}	High-level input voltage			2			٧
VIL	Low-level input voltage		*,			0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	- 18mA			-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0		2.7	3.5		V
VOH	- Ingili level output voltage	V _I =2V, I _{OH} =-400	0μΑ	2.7 3.5	3.5		. •
VoL	Low-level output voltage	V _{CC} =4.75V			0.25	0.4	٧
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA	,	0.35	0.5	٧.
1	High-level input current	V _{CC} =5.25V, V _I =2	.7V			20	μА
ľН	riigh-level impat current	$V_{CC} = 5.25V$, $V_{I} = 1$	0 V			0.1	m A
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0	.4V			-0.4	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =	0V .	-20		— 100	m A
Icc ·	Supply current	V _{CC} =5.25V (Note 3			12	20	mΑ

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

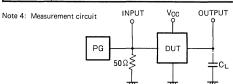


Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, \overline{A} and B and \overline{A} set from 0V momentarily to 4.5V.

SWITCHING CHARACTERISTICS (V_{GC}= 5 V, T_a=25°C, unless otherwise noted)

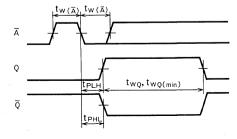
Combal	D.,,,,,,,,,	Total and disional		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input \overline{A} to output Q			19	33	ns
t _{PLH}	Low-to-high-level output propagation time, from input B to output Q	C _T = 0 pF		20	44	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{A} to output \overline{Q}			· 21	45	ns
t _{PHL}	High-to-low-level output propagation time, from input B to output $\overline{\mathbb{Q}}$	R _T = 5 kΩ		23	56	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q	C _L =15pF (Note 4)		18	27	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}			23	45	ns
t _{WQ (min)}	Minimum output pulse width, from inputs A . B to output Q	1		66	200	ns
two	Output pulse width, from inputs \overline{A} . B to output Q	$C_T = 1000 pF$, $R_T = 10 k \Omega$ $C_L = 15 pF$ (Note 4)	4	4.55	5	μs

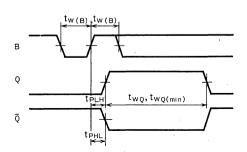


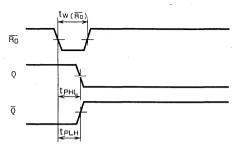
- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz (100kHz with t_{WO} measurement), t_r=6ns, t_r=6ns, t_w≥40ns, V_P=3V_{P,P}, Z_O=50Ω.
- (2) C₁ includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V. Ta = 25°C, unless otherwise noted)

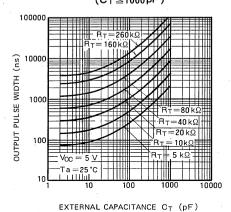
Symbol	Parameter	Test conditions		Unit		
Symbol	i arameter		Min	Тур	Max	Unit
tw(A)	Trigger input A pulse width		40	15		ns
t _{W(B)}	Trigger input B pulse width		40	10		ns
t _{W (RD)}	Direct reset input pulse width RD		40	15		ns .







TYPICAL CHARACTERISTICS OUTPUT PULSE WIDTH VS C_T, R_T (C_T≤1000pF)

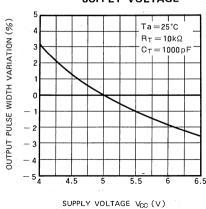


Note 5. Error within ±20% of output width given in the figure above.

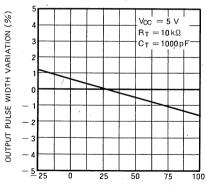
K VS CT (C>1000 pF) K (COEFFICIENT TO OBTAIN OUTPUT PULSE WIDTH) 1.0 0.9 0.8 Ta = 25°C 0.7 0.6 n : 0.4 0.3 0.2 0.1 103 105 106

EXTERNAL TIMING CAPACITANCE CT(pF)

OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



AMBIENT TEMPERATURE Ta (°C)

OUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS125AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input \overline{OC} which is independent for each buffer.

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 52mW typical)
- High speed (tpd = 8ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

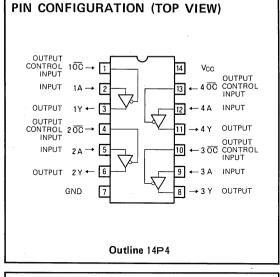
FUNCTIONAL DESCRIPTION

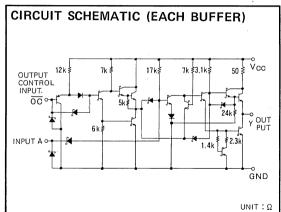
When \overline{OC} is low, high appears in the output Y if input A is high and low appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

ōc	Α	Y
L	L	L
L	н	Н
Н	Х	٠Z

Note 1: X: irrelevant
Z: high-impedance





ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage	,	-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		- 20 ~ + 75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	×*	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA
		V _O L≦0.4V	0		12	mA
IOL	Low-level output current	V _{OL} ≦0.5V	0		24	mA

OUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

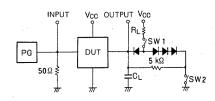
Symbol	Parameter	Test con	ditions	Limits			Unit
Symbol	rarameter	Test conditions		Min	Тур*	Max	Unit
VIH	High-level input voltage			. 2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
	High level gutnut valters	V _{CC} =4.75V, V _I =0.8	IV	2.4 3.1			
VoH	High-level output voltage	$V_1 = 2V$, $I_{OH} = -2.6m$	ıΑ				· ·
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 12 mA		0.25	0.4	V
V _{OL}	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 24 mA		0.35	0.5	. V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I (0C)	=2V, V ₀ =2.4V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I (OC)	=2V, V ₀ =0.4V			-20	. /(A
	Disk leadings a second	V _{CC} =5.25V, V _I =2.7	V			20	μΑ
lін	High-level input current	V _{CC} =5.25V, V _I =10V	1			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 40		-225	mA
Iccz	Supply current, all outputs off	V _{CC} =5.25V, V _I =0V	, V _{I (OC)} =4.5V		11	20	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

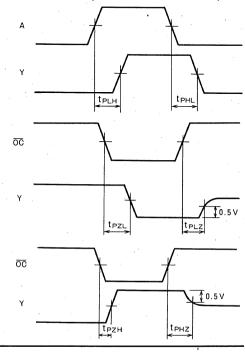
		Total conditions	Limits			11.5
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level,	C _L =45pF		7	15	ns
t _{PHL}	high-to-low-level output propagation time, from input A to output Y	(Note 3)		10	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		12	20	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	20	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$ $C_L=5$ pF (Note 3)	-	. 13	20	ns

Note 3: Measurement circuit



Parameter	SW 1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) All diodes are switching diodes $(t_{rr} = \le 4ns)$
- (3) CL includes probe and jig capacitance





Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

M74LS126AP

OUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS126AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input OC which is independent for each buffer

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (Pd = 59mW typical)
- High speed (tpd = 10ns typical)
- Wide operating temperature range ($T_a = 20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When OC is high, high appears in the output Y if input A is high and low appears if A is low. When OC is low, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

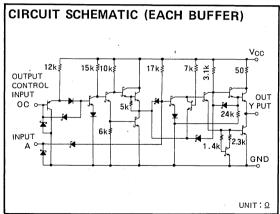
FUNCTION TABLE (Note 1)

ос	Α	Y
Н	L	L
Н	. н	Н
L	Х	Z

Note 1: X: irrelevant

Z: high-impedance

PIN CONFIGURATION (TOP VIEW) OUTPUT CONTROL 10C Vcc INPUT OLITPLIT INPUT 40C CONTROL OUTPUT INPUT OUTDUIT CONTROL 200 OUTPUT 11 INPUT OUTPUT INPUT CONTROL 10 OUTPUT 2 ٧ 6 GND OUTPUT Outline 14P4



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	- Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI .	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	_			Limits				
Symbol	Paramete		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA		
		V _{OL} ≤0.4V	0		12	mA		
loL	Low-level output current	V ₀ L≦0.5V	0		24	mA		

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Tost and	itions	Limits			
Symbol	Farameter	rest cond	Test conditions		Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
.,	High level output volters	V _{CC} =4.75V, V _I =0.8	V	2.4 3.1			V
VoH	High-level output voltage	$V_{I}=2V$, $I_{OH}=-2.6m$	Α				V
V	A	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	, V
VoL	Low-level output voltage	V _I =0.8V, V _I =2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _{I(OC)} =	0.8V, V ₀ =2.4V			2,0	. μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _{I(OC)} =	0.8V, V ₀ =0.4V			-20	μΑ
1	High In all in a decimal and a second	V _{CC} =5.25V, V _I =2.7	V '	-		20	μΑ
liH .	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mΑ
IIL 1	Low-level input current	V _{CC} =5.25V, V _I =0.4	V .			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 40		– 225	· mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =0V			12	22	mA

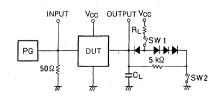
^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V . Ta = 25°C, unless otherwise noted)

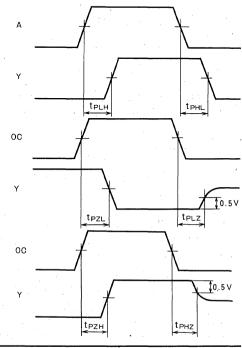
Symbol	Parameter Test conditions	Test conditions	Limits			Unit
Symbol	i dianetei	rest conditions	Min	Тур	Max	Ont
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,	C ₁ = 45pF (Note 3)		7	15	ns
t _{PHL}	from input A to output Y	OL=45pr (Note 3)		10	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		14	25	ns
tpzL	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		16	35	ns
t _{PHZ}	Output disable time from high-level	R _L =667Ω, C _L = 5pF (Note 3)		16	25	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L = 5pF (Note 3)		12	25	ns

Note 3: Measurement circuit



Parameter	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω ,
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns)
- (3) CL includes probe and jig capacitance





QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS132P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 35.2mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

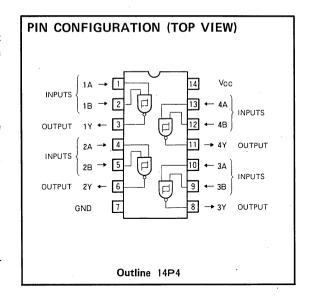
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

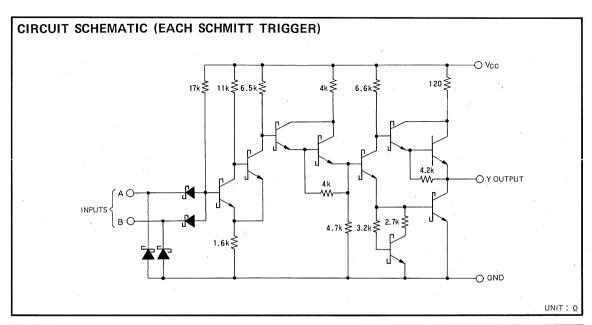
When inputs A and B are high, output Y is low, and when either or both inputs are low, Y is high.

Refer to M74LS14P for the typical characteristics.



FUNCTION TABLE

Α	В	Υ
L	L	• н
Н	L	н
L	Н	Н
Н	Н	L



QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		-65~ + 150	င

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

	Symbol Parameter			Limits		Unit
Symbol			Min	Тур	Max	Unit .
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА
1	Law facel and a	V _{OL} ≤0.4V	0		4	mA
OL Low-leve	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Complete	Parameter	Test conditions			Limits		Unit	
Symbol	r alattictei	rest conc	intions	Min	Typ *	Max	Onit	
V _{T+}	Positive-going threshold voltage	V _{CC} = 5V		1.4	1.6	1.9	V	
V _T -	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	V	
$V_{T+}-V_{T-}$	Hysteresis width .	V _{CC} =5V		0.4	0.8		V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} = - 18mA			- 1.5	V	
Vон	High-level output voltage	$V_{CC}=4.75V, V_1=0.5$ $I_{OH}=-400\mu A$	$V_{CC}=4.75V, V_1=0.5V$ $I_{OH}=-400\mu A$		3.4		· V	
\/	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VoL	Low-level output vortage	V _I = 1.9V	I _{OL} =8mA		0.35	0.5	٧	
· IT+	Input current at positive-going threshold	$V_{CC}=5V$, $V_I=V_{T+}$			-0.14		mA·	
I _T _	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_{T-}$			-0.18		mA	
1	High-level input current	V _{CC} =5.25V V _I =2.7V				20	μА	
· liH	righ-level input current	V _{CC} =5.25V V _I =10V				0.1	mA	
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mΑ	
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0	V	- 20		— 100	mA	
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V	1		5.9	11	mA	
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.	5V		8.2	. 14	mΑ	

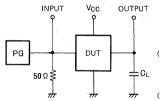
^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C, unless otherwise noted)

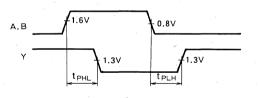
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Oiiit
t _{PLH}	Low-to-high-level output propagation time	C _L = 15pF (Note 2)		. 12	22	ns
t _{PHL}	High-to-low-level output propagation time	CL= 13pr (Note 2)		14	22	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



M74LS133P

SINGLE 13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS133P is a semiconductor integrated circuit containing one 13-input positive-logic NAND gate, usable as a negative logic NOR gate.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 2.5mW typical)
- High speed (t_{nd} = 11 ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

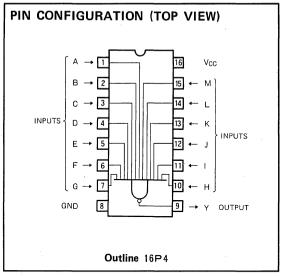
The use of PNP transistors for the inputs and active pull-up transistors for the outputs enables input high breakdown voltage, high speed, low power dissipation and high fan-out,

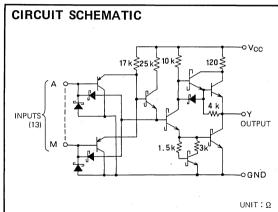
When inputs A through M are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Υ
L	L	Н
Т	L	Н
L	Н	Н
Н	н	L

 $N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

SINGLE 13-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	Symbol Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
		V _{OL} ≦0.4V	0		4	mΑ	
lor	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Complete	Parameter Test conditions		attat		Limits		
Symbol	Parameter	l est con	aitions -	Min	√ Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL '	Low-level input voltage	1				8,.0	V.
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	V
	N N N N N N N N N N N N N N N N N N N	V _{CC} =4.75V, V _I =0	.8V	2.7	3.4		V
V _{OH}	High-level output voltage	$I_{OH} = -400 \mu A$		2.7	3.4		· ·
· · ·	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
I	Uish land issue	V _{CC} =5.25V, V _I =2.	7V			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	. mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4V				0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
I _{CCH}	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.35	0.5	mA
IccL	Supply current, all inputs low	V _{CC} =5.25V, V _I =0r	pen		0.6	1.1	mA

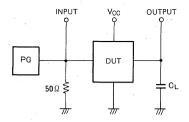
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 1: All measurements should be done quickly.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

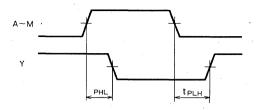
Symbol	Symbol Parameter Test conditions		Unit			
		rest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level/high-to-low-level	C _L = 15 pF (Note 2)		` 6	15	ns
tpHL	output propagation time	OL TSPF (Note 2)		16	38	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- . (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the V_{CC} supply voltage.

M74LS136P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS136P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown output voltage $(V_0 \ge 7V)$
- Low power dissipation (Pd = 30.5mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

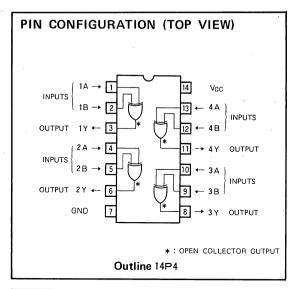
FUNCTIONAL DESCRIPTION

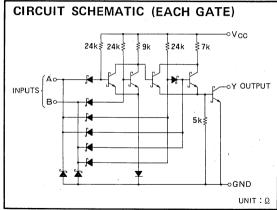
With the use of open collector output, the high-level output impedance can be freely selected by means of an external resistor. This make possible use in the wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high or both low, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Υ
L	L.	L
Н	L	Н
L	Н	Н
н	н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level state	-0.5~+7	٧
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits				
Symbol	Parame	ter .	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V ₀ =5.5V	0		100	μА		
		V _{OL} ≦0.4V	0		4	mA		
lor	Low-level output current	V ₀ L≦0.5V	0		8	mΑ		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

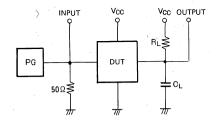
Symbol	D				Limits		Unit
Syllibol	Parameter	Test cond	Min	Typ*	Max	OIII	
ViH	High-level input voltage			2			V
VIL	Low-level input voltage				0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-			-1.5	V	
	High-level output current	V _{CC} =4.75V, V _I =0.			100		
Юн	nightever output current	$V_1 = 2V$, $V_0 = 5.5V$	1		100	μА	
.,		V _{CC} = 4.75 V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =2.7	v			40	μА
Ιιн	High-level input current	V _{CC} = 5.25V, V _I = 10V	/			0.2	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4			-0.8	mA	
Icc	Supply current	V _{CC} =5.25V (Note 1)			6.1	10	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

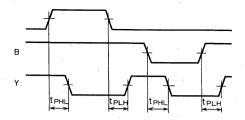
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Syllibol	raiametei	l est conditions	Min	Тур	Max	Onit
tpLH	Low-to-high-level, high-to-low-level output propagation	R _L = 2 kΩ		14	30	ns
tpHL	time,	$C_L = 15 pF$ Other input low (Note 2)		14	30	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	$R_L = 2 k\Omega$. 12	30	ns
tpHL	time,	C _L = 15 pF Other input high (Note 2)		12	30	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



Note 1: I_{CC} is measured with all inputs grounded.

DESCRIPTION

The M74LS137P is a semiconductor integrated circuit containing a 3-line-to-8-line decoder/multiplexer function with address latch

FEATURES

- Address latch capability with latch enable input
- Easy cascade connection with two enable inputs
- Wide operating temperature range (Ta: −20 − +75°C)

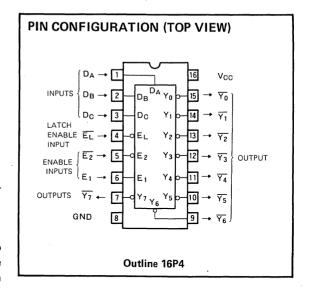
APPLICATIONS

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTIONS

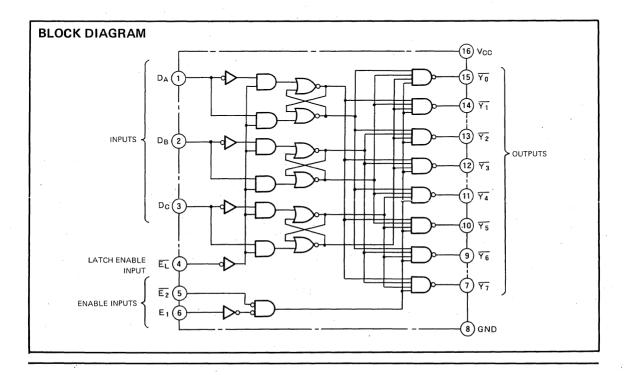
When latch enable input $\overline{E_L}$ is low, the data applied to inputs $D_A - D_C$ are read into the latch; when it is high, the device operates as a decoder/demultiplexer with a function that retains the data

When the device is used as a decoder and inputs D_A-D_C are designated with a 3-bit binary code, one output among outputs $\overline{Y_0}-\overline{Y_7}$ corresponding to the numerical value is set low and the other seven outputs are all set high. In this case, enable input $\overline{E_1}$ is set high and enable input $\overline{E_2}$ is set low. When $\overline{E_1}$ and $\overline{E_2}$ are subject to any other conditions, the outputs are set high regardless of the status of D_A-D_C . (Refer to application examples)



When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making E_1 and $\overline{E_2}$ the data inputs and D_A-D_C the selection inputs.

This IC is the same as the M74LS138P except that it features a latch function in inputs $D_A - D_C$.



FUNCTION TABLE

ĒL	E ₁	E ₂	Dc	D _B	DΔ	$\overline{Y_0}$	$\overline{Y_1}$	Y ₂	Y ₃	$\overline{Y_4}$	Y ₅	$\overline{Y_6}$	<u>Y</u> 7
X	Х	Н	X	Х	Х	Н	Н	Н	Н	Ι	H	Τ	Ι
Х	L	Х	Х	Х	Х	Η	Н	Н	Н	Ι	Н	Н	I
L	Н	L	L	L	L.	L	Н	Н	Н	Н	Н	H	Н
L	Н	L	L	L	Н	Н	L	Н	Н	H.	Н	Ι	Ι
L	Н	L	L	Ĥ	L	Н	Н	L	Н	Η	Н	I	Ι
L	Н	L.	L	Н	Н	Η	Η	Н	L	Ι	Н	н	Ι
L	Н	L	Н	L	۲	Η	Τ	Н	Н	٦	Ξ	Н	H
L	Н	L	Н	L	Ι	Ι	H	Н	Н	Н	L	H	Н
L	Н	L	Н	H.	∟	Ι	Η	Н	Н	H	Ξ	ŗ	Н
. L	Ι	L	Ι	Ι	Ξ	Ι	Ι	Н	Н	Н	Н	Н	Г
н	Ι	L	x	х	×	Output corresponding to stored address, L; all other, H.							

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	· V
V _O	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Colombia al	Parameter		Limits		1.1-14	
Symbol	rarameter	' '	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
loh	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
1	Low-level output current	V _{OL} ≦0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (. $T_a = -20 \sim +75$ °C, unless otherwise noted).

0 1 1						Limits		
Symbol	Parameter		Test conditions		Min	Тур*	Max	Unit
V _{IH}	High-level input voltage	1			2			٧
VIL	Low-level input voltage						0.8	V
V _{IC} ,	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18m	Α			-1.5	٧.
V	High-level output voltage		V _{CC} =4.75V, V _I =0.8V		2.7	3.4		· v
V _{OH}	High-level output voltage		$V_1 = 2 V$, $I_{OH} = -400 \mu A$		2.7	3.4		v .
1/-	Low-level output voltage		V _{CC} =4.75V	1 _{0L} =4mA		0.25	0.4	V
VoL	Low-level output voltage	1.1	V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	V
	Ligh level input ourset		V _{CC} =5.25V, V _I =2.7V				20	. μΑ
Чн	High-level input current		V _{CC} =5.25V, V _I =10V				0.1	· mA
1	Low-level input current	E _L , E ₁ , E ₂	V				-0.4	
lic.	Low-level input current	DA, DB, DC	V _{CC} =5.25V, V _I =0.4V				-0.2	mA
los	Short-circuit output current (Note 2)		$V_{CC} = 5.25V, V_{O} = 0V$		- 20		- - 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			11	18	mΑ

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 3: Supply current should be measured with all inputs grounded.

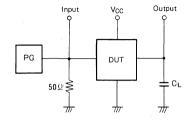


Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

				T		Limits		
Symbol	Parameter	les		Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high, high-to-low output		2			8	17	ns
t _{PHL}	propagation time, from inputs D_A , D_B , D_C to outputs $\overline{Y_0} = \overline{Y_7}$		4			15	38	lis
t _{PLH}	Low-to-high, high-to-low output propagation time, from inputs DA, DB,	gate stages	3			10	24	ns
t _{PHL}	D_C to outputs $\overline{Y_0} - \overline{Y_7}$	ate st	3			13	29	113
t _{PLH}	Low-to-high, high-to-low output propagation time, from input E ₂	delay ga	2	C ₁ = 15pF (Note 4)		9	21	ns
t _{PHL}	to outputs $\overline{Y_0} - \overline{Y_7}$	of del	2	OL Table (Note 4)		10	27	115
t _{PLH}	Low-to-high, high-to-low output propagation time, from input E ₁		3			10	21	ns
t _{PHL}	to outputs $\overline{Y_0} - \overline{Y_7}$	Number	3	•		12	27	113
t _{PLH}	Low-to-high, high-to-low output propagation time, from input E		3			13	27	ns
t _{PHL}	to outputs $\overline{Y_0} - \overline{Y_7}$		4			18	38	115

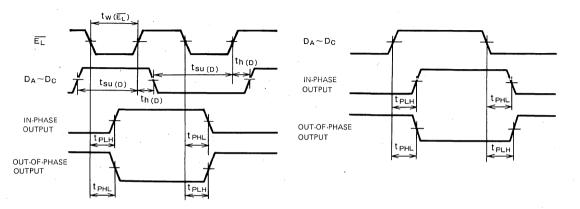
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_r = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50 ohms.
- (2) C_L includes probe and jig capacitance.

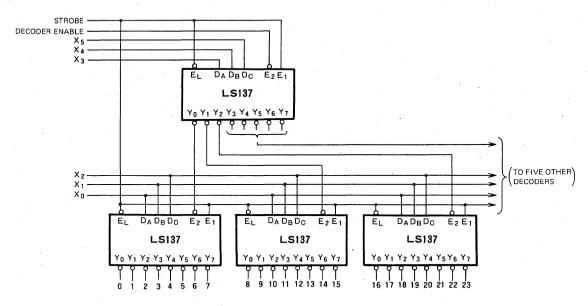
TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

0 1 1		Total and distant		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
tw(EL)	Latch enable EL pulse width		15	4		ņs
t _{su(D)}	Setup time $D_A - D_C$ to $\overline{E_L}$		10	3		ns
t _{h(D)}	Hold time $D_A - D_C$ to $\overline{E_L}$. 10	0		ns

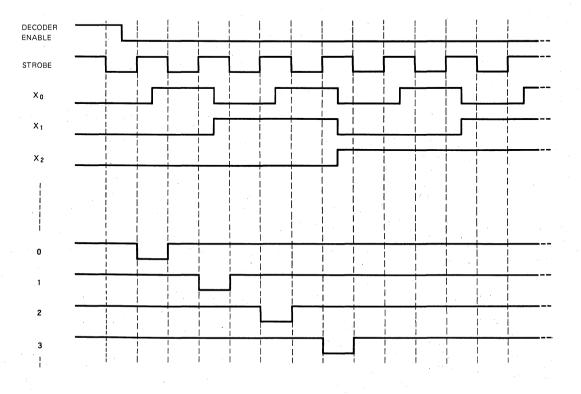


APPLICATION EXAMPLES (6-bit 2-line-to-64-line decoder with address latch)

(a) CIRCUIT DIAGRAM



(b) FUNCTION WAVEFORM



M74LS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS138P is a semiconductor integrated circuit consisting of a 3-bit binary-octal decoder/demultiplexer with enable inputs.

FEATURES

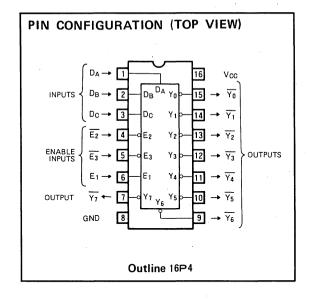
- 3 classes of enable inputs
- 4 to 16 decorder/demultiplexer functions are provided without use of external components.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

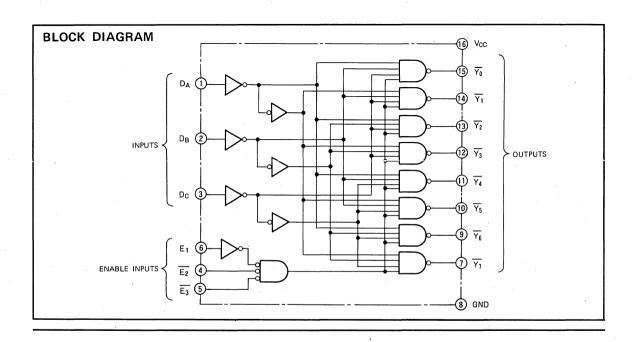
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

For use as a decoder, specify inputs D_A , D_B , and D_C in 3-bit binary code. In the case of decoding function, the E_1 is kept in high state while $\overline{E_2}$ and $\overline{E_3}$ are kept low. If E_1 , $\overline{E_2}$ and $\overline{E_3}$ are not in these conditions, all the outputs become high, irrespective of the status of $D_A \sim D_C$. For use as a demultiplexer, $\overline{E_1}$, $\overline{E_2}$ and E_3 are used as data inputs and D_A , D_B , and D_C as selection inputs. This forms a 1-line to 8-line demultiplexer.





3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

E ₁	Ēχ	Dc	DB	DΔ	$\overline{Y_0}$	<u>Y</u> 1	Y ₂	· Y ₃		<u>Y</u> 5	Y ₆	<u>Y</u> 7
Х	Н	Х	X	X	Н	Н	н	Н	Н	Н	Н	Н
L	Х	×	Х	X	н	Н	Н	н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
H	L	L	L	Н	Н	L	Н	• н	Н	Н	Н	H .
Н	L	L	Н	L	н	ŀН	L	Н	Н	H	н .	Н
Н	L	L	Н	Н	Н	´ H	Н	L	Н	H	Н	Н
Н	L	н	L.	L	Н	н	Н	Н	L	Н	Н	н.
Н	L	.н	L	Η	Ĥ	Н	Н	Н	Н	L	Н	н
Н	L	Н	н	L	Н	Н	Н	Н	Н	Н	L	н
Н	L	Н	н, .	H	Н	Н	Н	Н	Н .	Н	н	L

Note 1: $\overline{E_X} = \overline{E_2} + \overline{E_3}$ X: irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5∼+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

	_		11-7			
Symbol	Paramet	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	1	V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current VoL≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	B	Test sees	Test conditions		Limits		
Symbol	Parameter	Test cond			Typ*	Max	Unit
VIH	High-level input voltage						V
VIL	Low-level input voltage					0.8	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.	8V	2.7			.,
V_{OH}		$V_{I}=2V$, $I_{OH}=-400$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V
		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	High level in the second	V _{CC} =5.25V, V _I =2.	V _{CC} =5.25V, V _I =2.7V			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10	V _{CC} =5.25V, V _I =10V			0.1	mA
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V _{CC} =5.25V, V _O =0V			- 100	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 3)			6.3	10	mΑ

* : All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all output off-state.

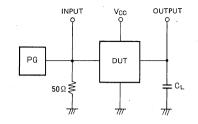


3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

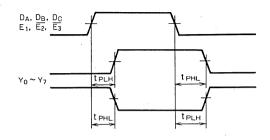
Combal	Parameter .		T Malana	Limits			Unit
Symbol			Test conditions	Min	Тур	Max	Onit
t _{PLH}		delay gate stages			9	20	ns
t _{PHL}	Low-to-high-level, high-to-low-level	2	, in the second		12	41	ns
t _{PLH}	output propagation time, from inputs DA, DB, DC to output Y0-Y7	delay gate stages			16	27	ns
t _{PHL}	DA, DB, SC to salpar to 1,		0 - 15 = 5 (Nave 4)		14	39	ns
tpLH	Low-to-high-level, high-to-low-level	delay gate stages	C _L = 15 pF (Note 4)		10	18	ns
t _{PHL}	output propagation time, from inputs $\overline{E_2}$, $\overline{E_3}$ to outputs $\overline{Y_0} - \overline{Y_7}$	2			15	32	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input	delay gate stages			8	26	ns
t _{PHL}	E ₁ to outputs Y ₀ -Y ₇	3			15	38	ns

Note 4: Measurement circuit



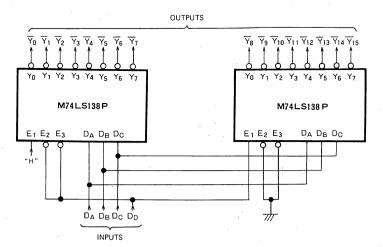
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-line to 16-line decorder/demultiplexer



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS139P is a semiconductor integrated circuit containing two 2-bit 2-line-to-4-line decoders/demultiplexers with separate enable inputs.

FEATURES

- Enable inputs provided
- Two circuits completely separate
- Wide operating temperature range (T_a=-20~+75°C)

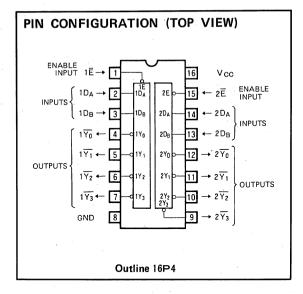
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

For use as a decoder, when inputs D_A and D_B are specified in 2-bit binary code, the output corresponding to the number among $\overline{Y_0} \sim \overline{Y_3}$ is set low and all the other 3 outputs are set high. The enable inputs \overline{E} are kept low. When inputs \overline{E} are high, all the outputs are set high irrespective of the status of D_A and D_B .

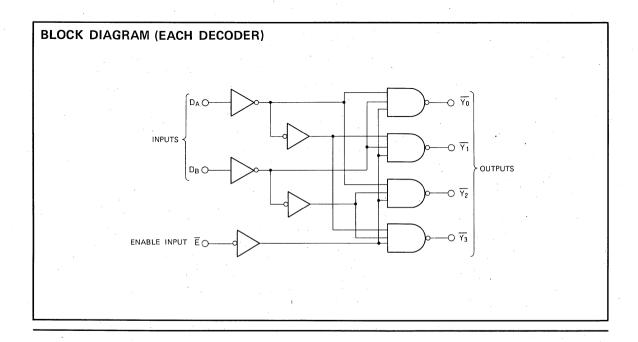
For use as a 1-line-4-line demultiplexer, make inputs \overline{E} the data inputs and D_A and D_B the selection inputs.



FUNCTION TABLE (Note 1)

Ē	DB	DA	$\overline{Y_0}$	<u>Y</u> 1	Y ₂	<u> 7</u> 3
Н	X	X	Ι	Н	Н	I
L	L	L	L.	. н	Н	Н
L	L	· H	н	L	Н	Н
L	Н	L	Н	Н	L	Н
L	Н	н	Н	Н	Н	L

Note 1: X : Irrelevant



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise ntoed)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage	·	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		− 65 ~ + 150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumbal	Parameter			Limits				
Symbol				Тур	Max	Unit		
Vcc	Supply voltage	4.75	5	5.25	V			
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА		
loL		V _{OL} ≤0.4V	0		4	mA		
	Low-level output current	V ₀ L≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

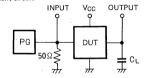
0	Parameter			Limits			Unit
Symbol	Parameter	lest cond	Test conditions			Max	
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
V _{OH}	High-level output voltage	$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-400\mu A$		2.7	3.4		V
VoL	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4	V
1	District the second sec	V _{CC} =5.25V, V _I =2.			0.33	20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 20		- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			6.8	11	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

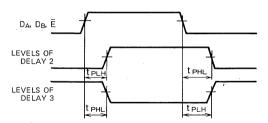
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter		Test conditions .	Limits			Unit
Symbol	rarameter		rest conditions .	Min	Тур	Max	Onit
t _{PLH}		dealy gate stages			8	20	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs				15	33	ns
t _{PLH}	D _A , D _B to outputs $\overline{Y_0} - \overline{Y_7}$				10	29	ns
t _{PHL}		3	C _L = 15 pF (Note 4)		15	38	ns
t _{PLH}	Low-to-high-level, high-to-low-level ou	tput propagation			8	24	ns
t _{PHL}	time, from input \overline{E} to outputs $\overline{Y_0} - \overline{Y_7}$				12	32	ns

Note 4: Measurement circuit



- (1) The pulse generator {PG} has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P .P, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance



Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs in the enable state.

BCD-TO-DECIMAL DECODER/DRIVER

DESCRIPTION

The M74LS145P is a semiconductor integrated circuit provided with BCD-to-decimal decoder/driver function and open collector outputs.

FEATURES

- High output current (I_0 =80mA with $V_{OL} \le 3V$; I_0 = 24mA with $V_0 \le 0.5V$)
- High output breakdown voltage (V_O≥15V)
- All outputs high with reactive input
- Wide operating temperature range (Ta=-20~+75°C)

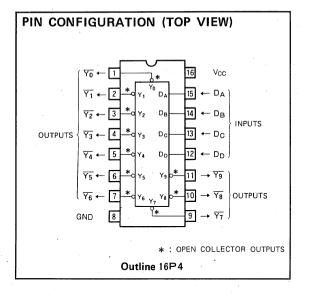
APPLICATION

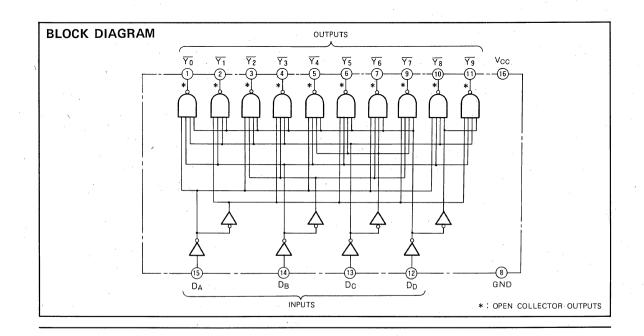
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When inputs D_A , D_B , D_C and D_D are designated with a BCD code in this decoder/driver, the $\overline{Y_0} \sim \overline{Y_9}$ output corresponding to the number is set low while the other 9 outputs are set high. When a binary number of 10 or more is applied to $D_A \sim D_D$, all the outputs are set high.

The outputs are open collector types with a breakdown voltage of 15V and an I_{OL} of 80mA (with $V_{OL} \le 3V$) This device is therefore suitable for use as an LSTTL/MOS interface, display tube and relay driver.





BCD-TO-DECIMAL DECODER/DRIVER

FUNCTION TABLE

Decimal number	D _D	Dc	DB	D _A	Y ₀	<u>Y</u> 1	Y ₂	Y ₃	<u>Y</u> 4	<u>Y</u> 5	Y ₆	Y ₇	<u>Y8</u>	Y ₉
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	Н	Н	Н	н	Н	Н	Н	Н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
3	L	L	Н	I	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	н	L	Н	Н	Н	Н	Н	Н	L	н	Н	Н	Н
6	L	Н	Н	L.	Н	Н	н	Н	Н	Н	L	Н	Н	Н
7	Ľ,	Н	н	I	Н	, н	T	Н	Н	Н	Н	L	Н	н
8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	н
9	Н	L	L	H	Н	н	Н	Н	Н	Н	Н	Н	Н	L
10	Н	L	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
11	Н	L	Н	I	Н	Н	Н	Н	Н	Н	Н	Н	н	Н
12	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
- 13	Н	Н	L	Н	Н	H.	Н	. Н	Н	Н	Н	Н	Н	Н
14 .	н	Н	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
15	Н	Н	н	Н	Τ	Н	Ι	Н	Н	Н	Н	Н	Н	Н

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage .	High-level state	-0.5~+15	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits		11.25
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	·V
Іон	High-level output current	V _{OH} = 15V	0		250	μА
		V _{OL} ≤0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal	D	Total			Limits		
Symbol	Parameter	Test condi	tions	Min	Typ*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V.I _{IC} =-	18mA			-1.5	V
Іон	High-level output voltage	$V_{CC}=4.75V \cdot V_{I}=0 \cdot V_{I}=2V \cdot V_{O}=15V$	8V			250	μА
		V 4 75V	1 _{0L} =12mA		0.25	0.4	V
VoL	Low-level output voltage	$V_{CC} = 4.75 V$ $V_{I} = 0.8 V, V_{I} = 2 V$	I _{OL} =24mA		0.35	0.5	V
		V ₁ =0.8V, V ₁ =2V	I _{OL} = 80mA		2.3	3	V
	IP-lateral in the second	V _{CC} =5.25V, V _I =2.	7 V			20	μΑ
ин	High-level input current	V _{CC} =5.25V, V _I =10	V			0,.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4 V ,			-0.4	mA
lcc	Supply current	V _{CC} =5.25V (Note 1)		7	13	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

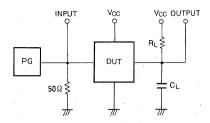
Note 1: I_{CC} is measured with $D_A \sim D_D$ at 0V.

BCD-TO-DECIMAL DECODER/DRIVER

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

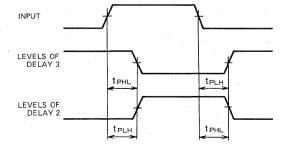
Symbol	Parameter		Test conditions		Limits		Unit
Cymbol	Taranice		rest conditions	Min	Тур	Max	Unit
t _{PLH}		delay gate stages			27	50	ns
t _{PHL}	Low-to-high-level, high-to-low-level	2	$R_1 = 665\Omega$, $C_L = 45pF$ (Note 2)		. 17	50	ns
t _{PLH}	output propagation time	delay gate stages	RL=6659, OL=45PF (Note 2)		27	50	ns
t _{PHL}		3			17	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference=1.3V)



10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

DESCRIPTION

The M74LS147P is a semiconductor integrated circuit containing a 10-line BCD encoder with a priority function.

FEATURES

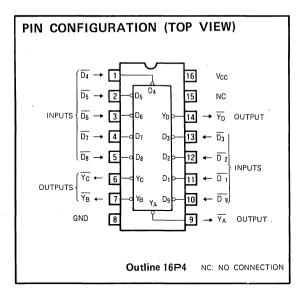
- Priority decoding of the data inputs
- Data inputs and outputs both active-low
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

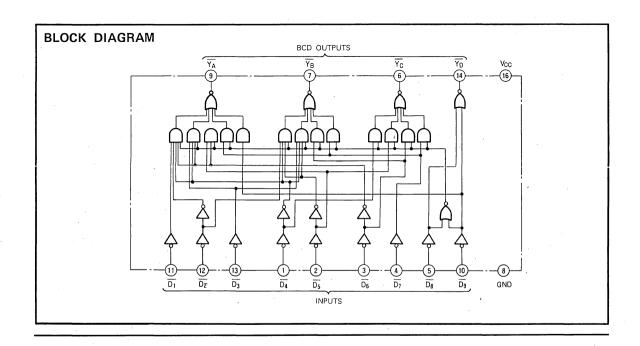
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions to encode a pulse entered through one of the nine input pins $(\overline{D_1} \sim \overline{D_9})$ into a BCD code by producing an inverted signal (based on input) at output $\overline{Y_A} \sim \overline{Y_D}$. The encoder handles all inputs in a priority sequence, so that when two or more are present at input at the same time, the signal present at the highest priority pin will be encoded. $\overline{D_0}$ does not exist as an input, and when all inputs are at high-level, all outputs will also be high-level, yielding a 0 output. Ideally suited for use as a keyboard encoder or range selector.





10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

FUNCTION TABLE (Note 1)

D ₁	D2	D ₃	D ₄	D ₅	D ₆	D ₇	D8	D ₉	ΥD	Yc	YB	Ϋ́A
н	.H	Н	Н	Н	Н	н	Н	Н	Н	Н	Н	Н
Х	X	×	×	Х	X	X	Х	L	L	н	Н	L
Х	Х	X	X.	Х	X.	X	L	Н	L	Н	Н.	H ·
Х	Х	Х	Х	Х	X	· L	Н	Н	Н	Ļ	L	L
Х	Х	Х	X	. X	L	н	Н	Н	Н	L	L	Н
Χ -	Х	Х	Х	· L	Н	Н	Н	Н	н	, L	Н	L
X	X	X	L	Н	Н	Н	. H	Н	Н ,,	L	Η	Н
Χ .	×	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L
. X	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	Н	· н	Н	Н	. Н	Н	Н	Н	Н	Н	Н	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level output	-0.5 ~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits		11.5
Symbol	rarameter		Min	Тур	Max	Unit
Vcc	Supply voltage	÷	4.75	5	5.25	· V
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА
	Low-level output current	V ₀ L≦0.4V	0		4	mΑ
lor	cow-level output current	V ₀ L≦0.5V	0		8	mΔ

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Test Con	atat -		Limits		
Syllibol	Farameter	lest Con	ditions	Min	Typ *	Max	Unit
VIH	High-level input voltage	*		2			٧
VIL	Low-level input voltage				,	0.8	٧
Vic	Input clamp voltage	Vcc=4.75V, lic=-	- 18mA			-1.5	· V
Vон	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		· V
Vol	Low-level output voltage	Vcc=4.75V	IoL=4mA		0.25	0.4	V
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	IoL=8mA		0.35	0.5	V
Ін	High-level input current	Vcc=5.25V, Vi=2.	7∨			20	μА
יוח	riigii-level iliput current	Vcc=5.25V, Vi=10	V			0.1	mA
lıL.	Low-level input current	Vcc=5.25V, Vi=0.	4V			-0.4	mA
los	Short-circuit output current (Note 2)	Vcc=5.25V, Vo=0	V .	-20		— 100	mA
ICC1	Supply current	Vcc=5.25V (Note 3)			12	20	mA
ICC2	Supply current	Vcc=5.25V (Note 4)			10	17	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} I_{CC1} is measured with $\overline{D_7}$ at 0V, and all other inputs open.

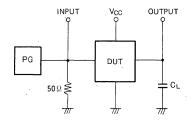
^{4.} I_{CC2} is measured with all inputs open.

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

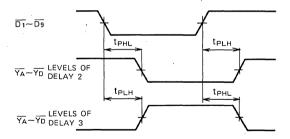
Symbol	Parameter	Test Conditions		Limits		11-14
Зупци	·	rest Conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			9	18	ns
t _{PHL}	from input $\overline{D}_1 \sim \overline{D}_9$ to output $\overline{Y}_A \sim \overline{Y}_D$ (levels of delay 2)	C _L = 15pF (Note 5)		14	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			25	33	ns
t _{PHL}	from input $\overline{D_1} \sim \overline{D_9}$ to output $\overline{Y_A} \sim \overline{Y_D}$ (levels of delay 3)			15	23	ns

Note 5. Measurement Circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P , v_t $Z_0 = 50\Omega$. (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



8-LINE TO 3-LINE PRIORITY ENCODER

DESCRIPTION

The M74LS148P is a semiconductor integrated circuit provided with an 8-line to 3-line priority encoder function and priority sequence function.

FEATURES

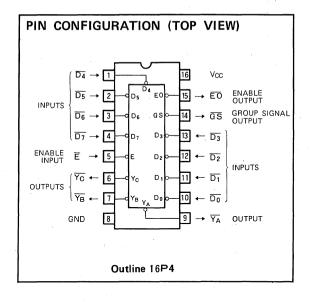
- Priority decoding of the data input
- Easy expansion of the number of input bit
- Wide operating temperature range (T_a=-20~+75°C)

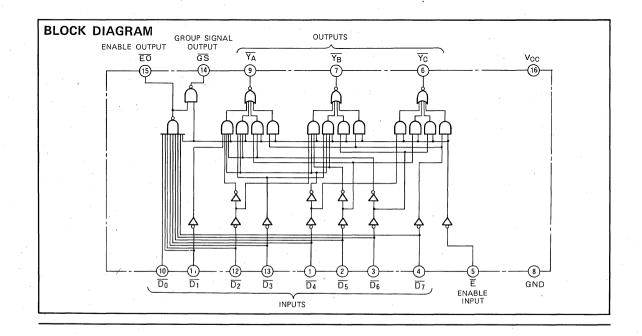
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When signals are applied to one of this encoder's eight inputs $\overline{D}_0 \sim \overline{D}_7$, the 3-bit binary number corresponding to the input pin appears at outputs $\overline{Y}_A \sim \overline{Y}_C$. Since priority is given to each input, the highest-level input pin signal is encoded when more than one signals are applied simultaneously. The number of input data can easily be increased as shown in the application example using the enable input \overline{E} , enable output $\overline{E}\overline{O}$ and group signal output \overline{GS} . This device is suitable for use as a keyboard encoder or for range selection.





8-LINE TO 3-LINE PRIORITY ENCODER

FUNCTION TABLE (Note 1)

Ē	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Yc	YB	YA	GS	ΕŌ
Н	X	X	X	×	X	×	X	X	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	н	Н	Н	Н	н	Н	L
L	×	Х	×	X	X	X	×	L	L	L	L	L	I
L	×	X	×	X	×	X	L	Н	L	L	Н	L	Н
L	×	X	Х	Х	X	L	н	Н	L	Н	L	L	Н
L	X	X	X	X	L	Н	Н	н	L	Н	Н	L	Н
L	×	×	×	L	Н	Н	Н	н	Н	L	L	L	Н
L	X	Х	Ŀ	Н	Н	Н	Н	н	Н	L	Н	L	Н
L	Х	L	Н	Н	Н	Н	Н	Н	Н	н	L	L	н
L	L	Н	Н	Н	Н	Н	н	Н	Н	Н	Н	L	н

Note 1 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range	·	-20~+75	°C
Tstg	Storage temperature range		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol			11-14			
Symbol	Paramet	er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μA,
	Low-level output current	V _{OL} ≤0.4V	. 0		4	mA
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

						Limits		Unit
Symbol	Paramet	er	Test condit	ions .	Min	Тур 🛊	Max	Onit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage	ut clamp voltage		18 mA			-1.5	V
V _{OH}	High-level output voltage			$V_{CC} = 4.75 \text{ V}, V_{I} = 0.8 \text{ V}$ $V_{I} = 2 \text{ V}, I_{OH} = -400 \mu \text{ A}$		3.4		V
.,	Low-level output voltage		V _{CC} =4.75V loL 4mA			0.25	0.4	. v
VoL	Low-level output voltage	0.00	$V_1 = 0.8V, V_1 = 2V$	I _{OL} 8mA		0.35	0.5	V
		D ₀ , E	V 5 0514 14 0 514				20	
	18 de Janes Carrera	$\overline{D_1} \sim \overline{D_7}$	$V_{CC} = 5.25V, V_I = 2.7$	V	40	40	μA	
I _{IH}	High-level input current	Do, E					0.1	A
		$\overline{D_1} \sim \overline{D_7}$	$V_{CC}=5.25V, V_{I}=10V$				0.2	mA
	Low-level input current	D ₀ , E					-0.4	mA
IIL	Low-level input current	$\overline{D_1} \sim \overline{D_7}$	$V_{CC}=5.25V, V_{I}=0.4V$				-0.8	11112
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
I _{CC1}	Supply current		V _{CC} =5.25V (Note 3)			12	20	mA
I _{CC2}	Supply current		V _{CC} =5.25V (Note 4)			10	17	mA

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with $\overline{D_7}$ and \overline{E} at 0V and with all other inputs open.

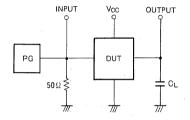
Note 4: I_{CC2} is measured with all inputs open.

8-LINE TO 3-LINE PRIORITY ENCODER

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

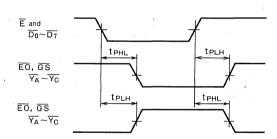
				Limits		
Symbol	Parameter	Test conditions	Min-	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	18	ns
t _{PHL}	time, from inputs $\overline{D_1} \sim \overline{D_7}$ to outputs $\overline{Y_A} \sim \overline{Y_C}$ (levels of delay 2)			14	25	ns
t PLH	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D}_1 \sim \overline{D}_7$ to outputs $\overline{Y}_A \sim \overline{Y}_C$			15	36	ns
t PHL	(levels of delay 3)	÷		18	29	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	18	ns
t _{PHL}	time, from inputs D ₀ ~ D ₇ to output E O (levels of delay 3)			24	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C ₁ = 15 pF (Note 5)		31	55	ns
t PHL	time, from inputs $\overline{D_0} \sim \overline{D_7}$ to output \overline{GS} (levels of delay 2)	OL 13 pr (Note 3)		8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	25	ns
t _{PHL}	time, from input \overline{E} to outputs $\overline{Y_A} \sim \overline{Y_C}$ (levels of delay 2)			14	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	17	, ns
t _{PHL}	time, from input E to output GS (levels of delay 2)			13	36	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output E O			11	21	ns
t _{PHL}	(levels of delay 2)			27	35	ns

Note 5: Measurement circuit



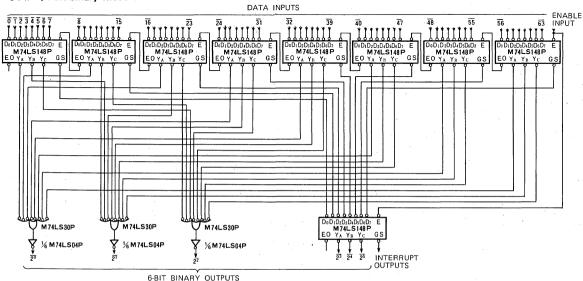
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r = 6ns, t_f = 6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

64-line/4-bit binary encoder



Expansion is possible up to 2ⁿ bits in accordance with the above application example.

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS151P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function.

FEATURES

- Strobe input provided
- Complementary output provided
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

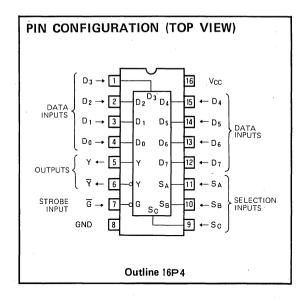
APPLICATION

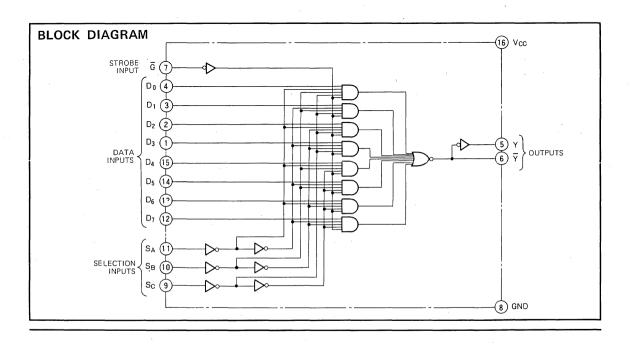
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and a multiplexer function which converts the 8-bit parallel data into serial data. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A , S_B and S_C , the input signal is output at Y and the inverted signal from output \overline{Y} . By applying 8-bit parallel data to $D_0{\sim}D_7$ and connecting a synchronous octal counter output to S_A , S_B and S_C , the data appear in Y in $D_0{\sim}D_7$ order and in \overline{Y} in $\overline{D_0{\sim}D_7}$ order as synchronized with the clock pulse. When strobe input \overline{G} is set high, Y is set low and \overline{Y} high.

M74LS151P has the same functions and pin connections as M74LS251P but the latter is provided with 3-state outputs.





8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

sc	SB	SA	G	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Y	Ÿ
Х	×	X	Н	×	× .	X	X	×	' X	Х	×	L	Н
L	L	L	L	L	Х	X	X	X	Х	X	, X	L	н
L	L	L	L	Н	Х	Х	×	×	X	Х	Х	Н	L
·L	L	. H	L	X	L .	X	×	X	Х	X	×	L	Н
L	L	Н	L	· X	Н	X	×	×	X	X	Х	Н	L
L	н	L	L	X	X	L	×	X	Х	X	×	L	н
L	Н	L	L	Х	Х	Н	X	Х	X	X	X	Н	L .
L	н	Н	L	X	×	X	L	X	Х	×	×	L	Н
L	Н	Н	L	X	X	X	н	Χ.	×	×	Х	Н	L
Н	L	L	L	Х	×	Х	Х	L	Х	X	· X	L	Н
Н	L	L	L	Х	×	Х	Х	Н	х	×	Х	Н	Ĺ
н	L	н	L	X	×	×	×	X	L	×	X	L	Н
Н	L	н	L	X	×	X	×	X	Н	×	Х	н	L
Н	Н	L	L	X	X	Х	Х	X	Х	L	X	L	Н
н	Н	L.	L	Х	X	X	X	Х	Х	Н	- X ,	Н	L
H	Н	Н	L	Х	Х	X	×	×	X	×	L	L	Н
Ι	. н	Η	L	×	Х	Х	X	Х	Х	X	H	Н	L

Note 1 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parame		11-:-			
Symbol	r arame	Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	V.	
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
loL	- Low-level output current	V _{0L} ≤0.5V	0		8	mA

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

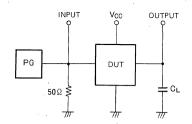
0	Parameter	Test cond	itions		Limits		11-14
Symbol	rarameter	Test cond	, , , , , , , , , , , , , , , , , , , ,			Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage	1				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-			-1.5	V	
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.8V		V _{CC} =4.75V, V _I =0.8V	2.4		
VoH	riiginevei output voitage	$V_1 = 2V \cdot I_{OH} = -400 \mu$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V ,
	Law Indiana and American	V _{CC} =4.75V	$I_{OL} = 4mA$		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V
	Lich land in a second	V _{CC} =5.25V, V _I =2.	7V			20	μА
Iн	High-level input current	V _{CC} =5.25V, V _I =10°	v •	•		0.1	mA
IIL.	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0\	/	-20		- 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			6	10	mA

^{* :} All typical values are at V_{CC} =5V, T_a =25°C. Note 2: All measurements should be done quickly. Note 3: I_{CC} is measured with all inputs at 4.5V

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

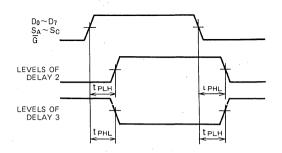
Symbol	Parameter	Test conditions		Limits		N. C.
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	23	ns
tpHL	time, from inputs S_A , S_B , S_C to output \overline{Y}			15	32	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			22	43	ns
tphL	time, from inputs S_A , S_B , S_C to output Y			16	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	24	ns
t _{PHL}	time, from input $\overline{\mathbf{G}}$ to output $\overline{\mathbf{Y}}$	C ₁ = 15 pF (Note 4)		14	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OE-13pi (Note 4)		21	42	ns
t _{PHL}	time, from input $\overline{\mathbf{G}}$ to output \mathbf{Y}			16	32	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	21	ns
t _{PHL}	time, from inputs $D_0 \sim D_7$ to output \overline{Y}			8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			17	32	ns
t _{PHL}	time, from inputs $D_0 \sim D_7$ to output Y			12	26	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference=1.3V)



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS153P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C)

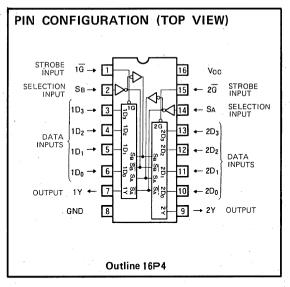
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 2-line to 1-line selection of 4 pairs of input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B , the input signal is output at Y. By applying 4-bit parallel data to D_0 , D_1 , D_2 and D_3 , and connecting a synchronous divide-by-4 counter output to S_A and S_B , the D_0 , D_1 , D_2 and D_3 data appear in the order of D_0 , D_1 , D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high, 1Y and 2Y are set low irrespective of the status of the input.

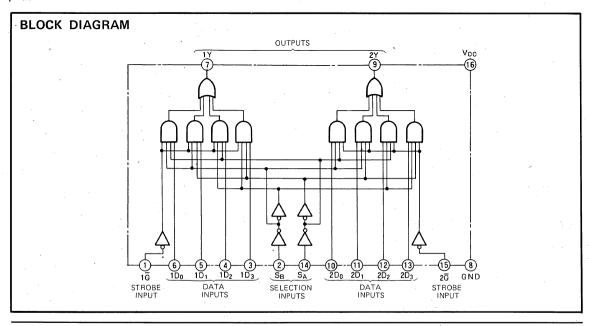
M74LS153P has the same functions and pin connections as M74LS253P but the latter is provided with 3-state outputs.



FUNCTION TABLE (Note 1)

SB	SA	D ₀	D ₁	D ₂	D ₃	G	Υ
X	Х	Х	×	X	X	Н	ا ا
L	L	L	×	X	X	١	٦
L	L	н	×	×	Χ.	L	Н
` L	н	×	L	х	X	L	. L
·L	Н	×	Н	X	Χ .	٦	Ι
н	L	×	×	L	X	L	L
н	L	×	×	Н	X	L	Ξ
Н	н	×	×	· X	L	L	L
Н	Н	×	×	X	Н	L	Н

Note 1 X : Irrelevant



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter ·	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V _O	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Darama		Unit			
Symbol	Paramet	Parameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
10.	Low-level output current	V _{OL} ≤0.4V	0		4	mA
lor	Low-lever output current	0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test cond	:•:		Limits		Unit
Symbol	rarameter	l est cond	rest conditions			Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{1C} =-1	V _{CC} =4.75V, I _{IC} = - 18mA			1.5	٧
	High-level output voltage	V _{CC} =4.75V, V _I =0.8V		0.7	3.4	i	
Voн	nigh-level output voltage	$V_1 = 2 V, I_{OH} = -400 \mu$	$= 2 \text{ V}, \text{ I}_{OH} = -400 \mu \text{A}$				٧
Va.	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.7V	V			20	μА
ΙН	Inginiever input current	V _{CC} =5.25V, V _I =10V				0.1	mA
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4V	V _{CC} =5.25V, V _I =0.4V			-0.4	mA .
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V	V _{CC} =5.25V, V _O = 0 V			- 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			6.2	10	mA

 $[\]boldsymbol{*}$: All typical values are at VCC=5V, Ta=25°C.

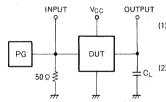
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: ICC is measured with all inputs at OV.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Зуппоп	r drameter	rest conditions	Min	Тур	Max	Offic
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	y.		8	15	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output Y			12	26	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			12	29	ns
t _{PHL}	time, from inputs SA, SB to output Y	C _L =15pF		13	38	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 4)		12	24	· ns
t _{PHL}	time, from input \overline{G} to output Y			12	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P.P}, Z_0 = 50\Omega.$

(2) CL includes probe and jig capacitance.

$D_0\!\sim\!D_3$ SA, SB, G LEVELS OF DELAY 2

TIMING DIAGRAM (Reference level = 1.3V)

M74LS155P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS155P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers.

FEATURES

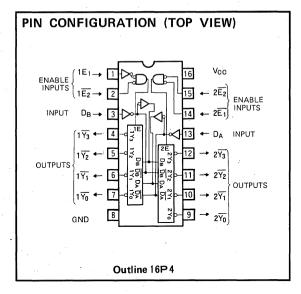
- Low output impedance
- Enable inputs provided
- 8-bit output decoder/demultiplexer functions are provided without the use of external components
- Wide operating temperature range (T_a =-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

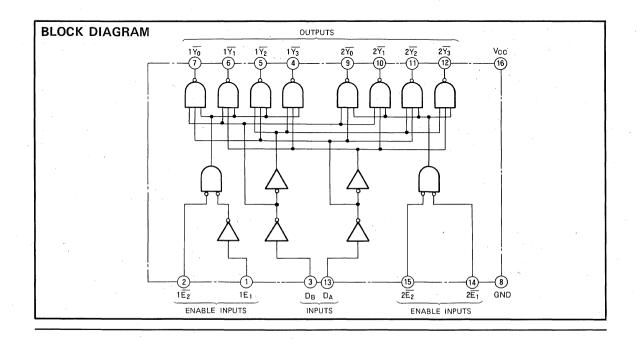
FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded in quaternary numbers and the 2-bit binary number is applied to inputs D_A and D_B , the corresponding $\overline{Y_0} \sim \overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number, the outputs appear in $2\overline{Y_0} \sim 2\overline{Y_3}$ and $1\overline{Y_0} \sim 1\overline{Y_3}$, in accordance with the function table.



For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0} \sim \overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $2\overline{E_1}$ are connected to make them the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to make the data inputs so that the outputs appear in $2\overline{Y_0} \sim 2\overline{Y_3}$ and $1\overline{Y_0} \sim 1\overline{Y_3}$.

M74LS155P has the same functions and pin connections as M74LS255P but the latter is provided with open collector outputs.



DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

DΒ	D_{A}	1E ₂	1E 1	1 7 0	1 7 1	$1\overline{Y_2}$	1 7 3
Х	Х	Н	Х	Ι	Н	Н	Н
L	L	L	I	L	Н	Н	Ι
L	Н	L	Н	Н	L	Η	Ι
Н	L	∟	Ι	Η	Н	L	Ι
Н	Н	L	Ι	Η	Н	Н	L
Х	Х	Х	Г	Ι	Н	Н	Н

Dв	DΔ	2E2	2E ₁	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	2 \overline{Y_3}
Х	Х	Н	Х	Н	Н	Н	Н
L	L	L	L	L	Н	Н	Н
L	Н	L	L	Ι	L	Н	Н
Н	L	L	L	Η	Н	L	Н
Η	н	L	L	Н	Н	н	L
Х	Х	х	Н	Н	Н	Н	Н

(3-bit binary to 8-line decoder/1 line to 8-line demultiplexer)

Dc	Dв	D_A	E	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$	1 \ \ 1\\ 0	1₹1	1 Y 2	1 _{Y3}
Х	Х	Х	Н	Η	Н,	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	н	Н	Н	Н	Н
L	L	Н	L	Η	L	Н	Н	Н	Н	н	Н
L	Н	L	L	Н	Н	L	н	Н	Н	Н	Н
L	н	Н	L	Η	Н	н	L	Н	Н	Н	Н
Н	L	L	L	Ι	Н	н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	L	Н	Н
Н	Н	L	L	Н	Н	н	Н	Н	Н	L	Н
Н	Н	H.	L	Н	Н	Н	Н	Н	Н	Н	L

Note 1 X : Irrelevant

 D_C : Pin connecting $1E_1$ and $2\overline{E_1}$ \overline{E} : Pin connecting $1\overline{E_2}$ and $2\overline{E_2}$

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	٧
Vo .	Output voltage	High-level state	-0.5~Vcc	V
Topr	Operating free-air ambient temperature range		-20~ +75	υ
Tstg	Storage temperature range		−65∼+150	Ċ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

				Limits		
Symbol	Parame	ter .	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	. 0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

Cumbal	Parameter	Test conditi	000		Limits		Unit
Symbol	Farameter	rest conditi	ons	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu\Delta$					٧
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	High Investigation of a superson	V _{CC} =5.25V V _I =2.7V				20	μΑ
Ιн	High-level input current	V _{CC} =5.25V V _I =10V				0.1	mA
liL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			6.1	10	mA

* : All typical values are at V_{CC}= 5V, T_a= 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time

Note 3: I_{CC} is measured with inputs $1\overline{E_2}$, $2\overline{E_1}$ and $2\overline{E_2}$ at 0V and with D_A, D_B and 1E₁ at 4.5V

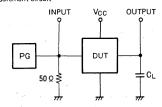


DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

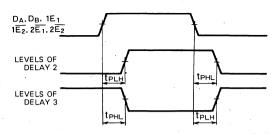
	Parameter		Test conditions		Limits			
Symbol	Parameter		· Test conditions	Min	Тур	Max	Unit	
tpLH		delay gate stages			8	15	ns	
t _{PHL}	Low-to-high-level, high-to-low-level	2			15	30	ns	
tpLH	output propagation time, from inputs D_A , D_B to outputs $\overline{Y_0} \sim \overline{Y_3}$	delay gate stages			10	26	ns	
t _{PHL}	DA, DB to see, page 10 - 13	3	0 45 5 (1)		15	30	ns	
t _{PLH}	Low-to-high-level, high-to-low-level ou	tput propagation	C _L = 15 pF (Note 4)		- 8	15	ns	
t _{PHL}	time, from inputs 1E2, 2E1, 2E2 to	outputs $\overline{Y_0} \sim \overline{Y_3}$			11	30	ns	
t _{PLH} .	Low-to-high-level, high-to-low-level output propagation				17	27	ns	
t _{PHL}	time, from input 1E ₁ to outputs 1Y ₀	~ 1 \overline{Y_3}		-	15	27	ns	

Note 4: Measurement circuit



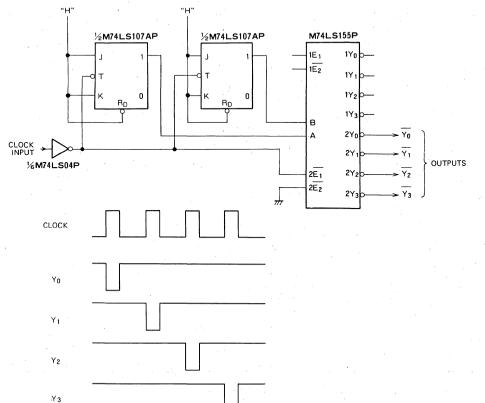
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C₁ includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-phase clock pulse generator



M74LS156P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS156P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers with open collector outputs

FEATURES

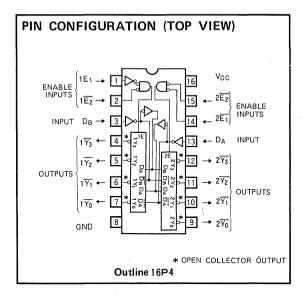
- Usable in AND Tie connection
- Enable inputs provided
- 8-bit output decoder/demultiplexer function is provided without the use of external components
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

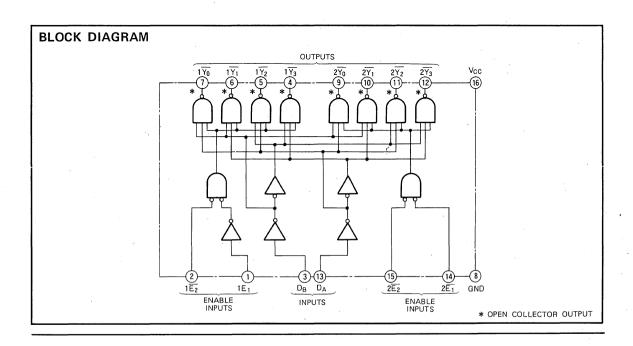
FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded as a quaternary number and the 2-bit binary number is applied to inputs D_A and D_B , the corresponding $\overline{Y_0} {\sim} \overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number to them, the outputs appear in $2\overline{Y_0} {\sim} 2\overline{Y_3}$ and $1\overline{Y_0} {\sim} 1\overline{Y_3}$, in accordance with the function table.



For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0} \sim \overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $1\overline{E_1}$ are connected to to be made the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to be made the data inputs so that the outputs appear in $2\overline{Y_0} \sim 2\overline{Y_3}$ and $1\overline{Y_0} \sim 1\overline{Y_3}$.

M74LS156P has the same functions and pin connections as M74LS155P but the latter is provided with active pull-up resistor outputs.



DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

DΒ	D_A	1E ₂	1E ₁	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	1 Y 3
X	Х	Н	X	Η	Н	Н	Н
L.	L	L	I	_	Н	Н	Н
∟	I	L	π	Ι	L	I	Ι
Н	┙	L	Н	Η	Ι	L	Ι
Н	I	┙	I	Ι	Τ	Н	Γ
Х	X	Х	Г	Ι	Τ	Ι	Ι

DΒ	DA	2E ₂	2E ₁	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	2 <u>Y</u> 3
Х	Х	Н	X	Ξ	Н	Н	Н
Ĺ	L	L	L	L	Н	Н	Н
J.	Н	L	L	Ι	L.	Н	Н
Τ	L,	L	Г	Н	Н	٦	Н
Η	Н	L	Γ	Н	Н	Н	L
Х	Х	Х	H	Н	Н	Н	Н

(3-bit binary to 8-line decoder/1 line to 8 line demultiplexer)

Dc	Dв	DΑ	Ē	$2\overline{Y_0}$	$2\overline{Y_1}$	2 Y 2	$2\overline{Y_3}$	1 Y 0	1 \ \	$1\overline{Y_2}$	$1\overline{Y_3}$
Х	Х	Х	Н	Н	Н	Н	Н	Н	Н.	Н	Н
L	L	L	L	L	н	н	н	Н	Н	Η	I
L	L	Н	L	Η	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	н.	L	Н.	Н	Н	Η	н
L	Н	Н	L	Ξ	Н	Н	L	н	Н	Н	Н
Н	L	┙	L	Ι	Н	Н	Н	┙	Ι	Ι	Н
Н	L	Н	L	Н	Н	н	Н	Н	L	Н	Н
Н	Н	L	٦	Ι	Н	Н	Н	Η	Н	Γ	I
Н	Н	Н	L	Ι	Η	H	Í	Ι	Ι	Η,	Γ

Note 1 . X : Irrelevant

 D_C : Pin connecting $1E_1$ and $2\overline{E_1}$ \overline{E} : Pin connecting $1E_2$ and $2\overline{E_2}$

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

			· · · · ·	
Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	င
Tstg	Storage temperature range		-65~+150	ొ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	rarameter	Min	Тур	Max ·	Unit		
Vcc	Supply voltage .		4.75	5	5.25	٧	
Гон	High-level output current	V ₀ =5.5V	0		100	μА	
	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
I OL .	mwiever output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Test cond	itions		Limits		
Symbol	raranietei	rest conditions		Min	Typ ∗	Max	Unit
· VIH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				- 1.5	٧
lou	IOH High-level output current	V _{CC} =4.75V, V _I =0.8	V .		100		
TOH	Thigh lover output current	$V_1=2V, V_0=5.5V$				100	μΑ
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μΑ
I _{IH}	riigh-leveriirpat carrent	V _{CC} =5.25V, V _I =10V				0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mΑ
lcc	Supply current	V _{CC} =5.25V (Note 2)			6.1	10	mA

* : All typical values are at V_{CC}= 5V, T_a= 25°C.

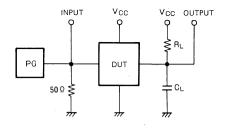
Note 2: I_{CC} is measured with inputs $1\overline{E_2}$, $2\overline{E_1}$ and $2\overline{E_2}$ at 0V and with D_A , D_B and $1E_1$ at 4.5V

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

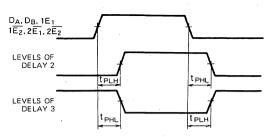
0	Parameter	Test conditions	Limits			Unit	
Symbol	Parameter		rest conditions		Тур	Max	On the
t _{PLH}		delay gate stages			18	40	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A , D_B to outputs $\overline{Y_0} \sim \overline{Y_3}$ dela	2	·		18	51	ns
t _{PLH}		delay gate stages	 R _L =2kΩ		20	46	ns
t _{PHL}		3	$C_L = 15pF$		18	51	ns
tpLH	Low-to-high-level, high-to-low-level or	utput propagation	(Note 3)		16	40	ns
t _{PHL}	time, from inputs $1\overline{E_2}$, $2\overline{E_1}$, $2\overline{E_2}$ to outputs $\overline{Y_0} \sim \overline{Y_3}$		(Note 3)		20	51	ns
t _{PLH}	Low-to-high-level, high-to-low-level or	tput propagation	•		20	48	ns
t _{PHL}	time, from input $1E_1$ to outputs $1\overline{Y}_0$	$\sim 1\overline{Y_3}$			25	48	ns

Note 3: Measurement circuit



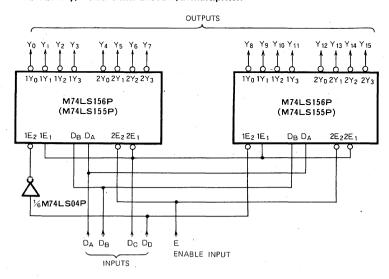
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P = 3 $V_{P,P}$, Z_Q =50 Ω .
- (2) C₁ includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-bit binary/hexadecimal decoder/demultiplexer



M74LS157P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DESCRIPTION

The M74LS157P is a semiconductor integrated circuit containing four 1-line to 2-line data selector/multiplexer circuits.

FEATURES

- Common strobe input for all 4 circuits
- Common select input for all 4 circuits
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

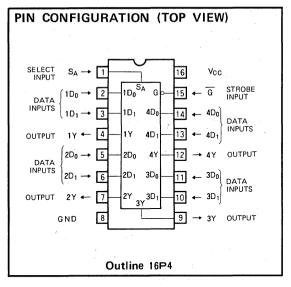
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has 4 circuits, each of which has a data selection function which selects one-line out of a 2-line signal and a multiplexing function to convert 2-bit parallel data into serial data by time sharing. When 2-line signals are fed to at inputs D_0 and D_1 and one of these is specified by the selection input S_A , the specified input signal is selected taken from output Y. The S_A and strobe inputs are common to all 4 circuits. When \overline{G} is high, all the outputs, 1Y, 2Y, 3Y, and 4Y are low, regardless of the inputs.

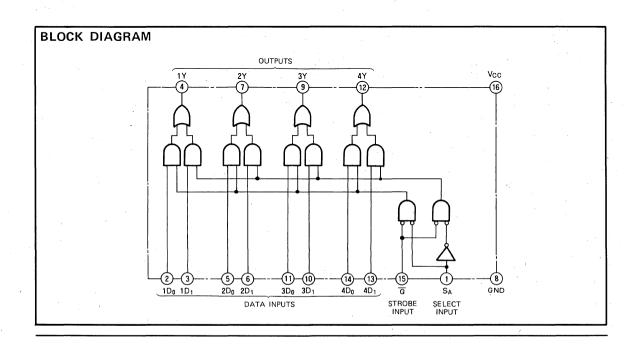
M74LS157P has the same functions and pin connections as M74LS257P but the latter is provided with 3-state outputs.



FUNCTION TABLE (Note 1)

Ğ	SA	D ₀	D ₁	Υ .
Н	Х	X	. X	L
L	L	L	Х	L
L	L	н	X	Н
L	н	X	L	L
L	Н	Х	Н	Н

Note 1: X: irrelevant



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	٧
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		- 65 - + 150	°

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	- arameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{0H} ≥2.7V	0		400	μА	
l lo	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
IOL Low-leve	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

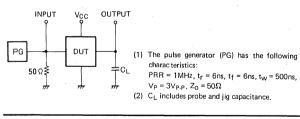
Symbol	Danamata	Parameter		!#!		Limits		
Symbol	raramete			Test conditions		Typ*	Max	Unit
VIH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	I8mA			-1.5	V
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		V
VoL	Low-level output voltage	oltage $V_{CC} = 4.75V$ $I_{OL} = 4mA$ $V_{I} = 0.8V, V_{I} = 2V$ $I_{OL} = 8mA$			0.25	0.4	V	
		D ₀ , D ₁	V _{CC} =5.25V V _I =2.7V	102 3117			20	μΑ
liH	High-level input current	D ₀ , D ₁	V _{CC} =5.25V V _I =10V	V _{CC} =5.25V			0.1	mA
IIL	Low-level input current	D_0 , D_1 S_A , \overline{G}	V _{CC} =5.25V V _I =0.4V				-0.4 -0.8	mA
los	Short-circuit output current (N		V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
Icc	Supply current V _{CC} =5.25V (Note 3)			9.7	16	mA		

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

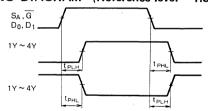
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
	Tarameter	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		7	14	ns
tphL	time, from input D ₀ , D ₁ to output Y			9	14	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			11	23	ns
tpHL	time, from input SA to output Y	0 -15.5 (0)		14	27	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		12	20	ns
tphL	time, from input \overline{G} to output Y			12	21	ns

Note 4: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: ICC is measured with all inputs at 4.5V.

M74LS158P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

DESCRIPTION

The M74LS158P is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits

FEATURES

- Converted outputs provided
- Strobe inputs provided independently for each circuits
- Selection inputs common to four circuits
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C).

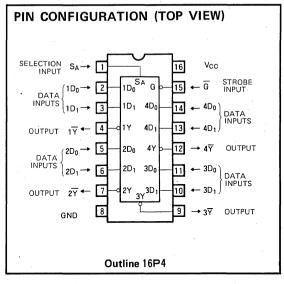
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 2-line to 1-line selection for 4 pairs of signals using four multiplexer circuits which convert the 2-bit parallel data into serial data with time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1 and 1 data is specified from among the data from selection input S_A , the input signal is inverted and can be output at \overline{Y} . By applying 2-bit parallel data to D_0 and D_1 , and connecting a binary counter output to S_A , the D_0 and D_1 data are inverted and appear in the order to D_0 and D_1 synchronized with the clock pulse. S_A and strobe input \overline{G} are common to all four circuits. When \overline{G} is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are set high irrespective of the status of the inputs.

M74LS158P has the same functions and pin connections

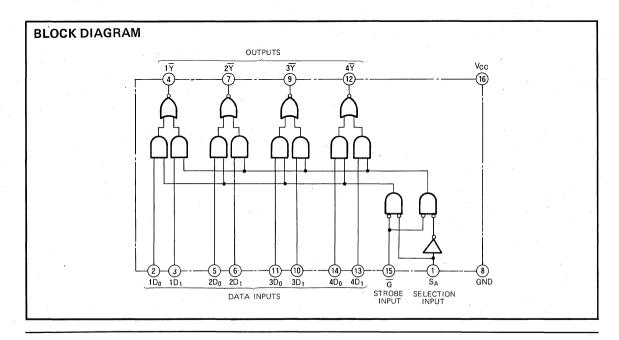


FUNCTION TABLE (Note 1)

G	SA	D ₀	D ₁	7
Н	X	Х	Х	н
L	L	L	Х	H
L.	L	Н	Х	L
L	Н	Х	L	н
L	н	×	Н	L

Note 1 X : Irrelevant

as M74LS258P but the latter is provided with 3-state outputs.



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75℃, unless otherwise noted)

				11.5		
Symbol	Parame	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
loL		V _{OL} ≦0.4V	0		4	mΑ
	Low-level output current VoL≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75℃, unless otherwise noted)

Combal	Parameter		Test condi	Test conditions		Limits		
Symbol	Paramete	şr	rest condi	rest conditions		Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage	Low-level input voltage					0.8	٧
Vic	Input clamp voltage V _{CC} =4.75\		V _{CC} =4.75V, I _{IC} =-1	I8mA			— 1.5	V
	√OH High-level output voltage		V _{CC} =4.75V, V _I =0.8	V	2.7			
VOH			$V_1 = 2V$, $I_{OH} = -400 \mu$	V _I =2V, I _{OH} = -400μA		3.4		, ν
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		D ₀ , D ₁	V _{CC} =5.25V	V _{CC} =5.25V			20	
	High-level input current	SA, G	V ₁ =2.7V				40	μΑ
Ιιн	riigii-iever input current	D ₀ , D ₁	V _{CC} =5.25V				0.1	
	S _A , \overline{G}		V _i = 10 V				0.2	mA
	Low-level input current	· D ₀ , D ₁	V _{CC} =5.25V				-0.4	mA
l _{IL}	Low-level input current	SA, G	V _I =0.4V				-0.8	
los	Short-circuit output current (N	Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		- 100	mA
Іссн	High level Supply current		V _{CC} =5.25V (Note 3)			4.8	8	mA
ICCL	Low-level supply current V _{CC} = 5.25V (Note 4)			6.5	11	mA		

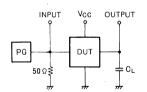
^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time. Note 3: ICC is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

	_				Unit	
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
tpLH	Low-to-high-level, high-to-low-level output propagation			5	12	ns
tphL	time, from inputs D_0 , D_1 to output \overline{Y}			5	12	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	O 15-5 (New 5)	/	9	20	ns
t _{PHL}	time, from input SA to output Y	C _L = 15pF (Note 5)		10	24	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			8	17	ns
tphL	time, from input G to output Y			8	18	ns

Note 5: Measurement circuit



(1) The pulse generator (GP) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_P$.P, Z_O = 50Ω .

(2) C_L includes probe and jig capacitance.

SA, G D0, D1 LEVELS OF DELAY 2 LEVELS OF DELAY 3 LPHL LPHL LPHL

TIMING DIAGRAM (Reference level = 1.3V)

Note 4: The supply current should be measured with $1D_0 \sim 4D_0$ at 4.5V and the other inputs at 0V.

DESCRIPTION

The M74LS160AP is a semiconductor integrated circuit containing a presettable synchronous decade counter function with a direct reset input.

FFATURES

- Direct reset and synchronous preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

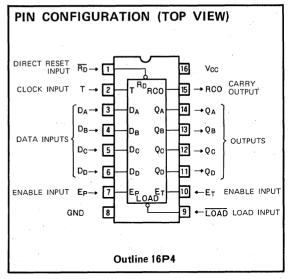
FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A , Q_B , Q_C and Q_D synchronized with the count pulse. Counting is done when T changes from low to high.

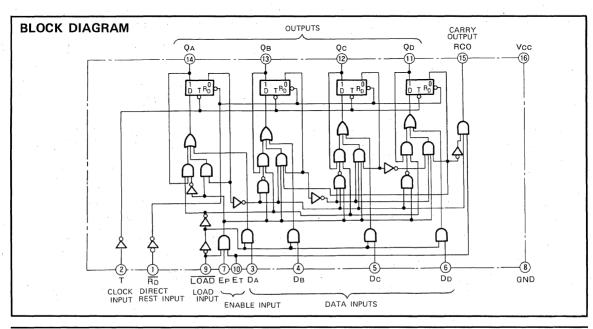
Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low and T is changed from low to high, the signals D_A , D_B , D_C and D_D appear at the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T , thereby presetting the counter.

When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

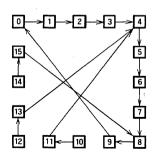
Resetting is asynchronous. Q_A , Q_B , Q_C and Q_D are set low by setting direct reset input $\overline{R_D}$ low, regardless of the status of the other inputs.



Carry output RCO is high only when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. E_P , E_T and RCO are used for synchronous counter cascade connection and for configuration of a divide-by- 10^n counter. (Refer to the application examples.)



STATE DIAGRAM



FUNCTION TABLE (Note 1)

$\overline{R_D}$	LOAD	ΕT	Ер	Т	QA	QB	Qc	Q□	RCO
L	×	Х	Х	X	L	L	L	L	L
Н	L	L	Х	1		_	n	n-	L
Н	L	Н	Х	1	DA	DB	B D _C	DD	L*
Н	н	Н	Н	1		Co	unt		L*
Н	н	L	X	Х	Inhibit			L	
Н	Н	Н	L	Х	Inhibit			L*	

Note 1. \uparrow : Transition from low to high (positive edge

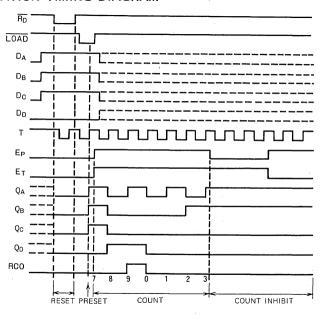
trigger)

* : RCO is normally low but is high when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. Therefore, RCO = Q_A · Q

is various.

X: Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Unit			
Symbol	. Farameter	. , , , , , , , , , , , , , , , , , , ,			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V ₀ ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
loL	Low-level output culterit	V _O L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	B		Test condit	ione		Limits		
Symbol	Paramet	er	l est condit	ions	Min	. Typ*	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8$ $V_{I} = 2V, I_{OH} = -400\mu$		2.7	3.4		Ý
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V OL	Low lover output vortage		V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	٧
	DA, DB, DC, DD, EP					20		
		LOAD, T, ET	$V_{CC} = 5.25V, V_1 = 2.7V$				40	μΑ
l _{IH}	High-level input current	RD .				20		
чн	· ingn-iever impat current	DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} =5.25V, V _I =10V				0.2	mA
		RD	*				0.1	
		DA, DB, DC, DD, EP					-0.4	
hL.	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4	V			-0.8	mΑ
		RD					-0.4	1.
los	Short-circuit output current (f	Short-circuit output current (Note 2)			-20		100	mA
Іссн	Supply current, all outputs hig	Supply current, all outputs high				18	31	mA
ICCL	Supply current, all outputs lov	Supply current, all outputs low				19	32	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits	,	Unit
Symbol	r aratheter	rest conditions	Min	Тур	Max	Onit
· f _{max}	Maximum clock frequency		25	55		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns
t PHL	from input T to output RCO			- 20	35	ns
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t PHL	(when \overline{LOAD} is high), from input T to outputs Q_A , Q_B , Q_C , Q_D	$C_L = 15pF$		16	27	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
t PHL	(when LOAD is low), from input T to outputs QA, QB, QC, QD			16	27	ns
t PLH	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns
t PHL	from input E _T to output RCO			8 .	14	ns
t PHL	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A , Q_B , Q_C , Q_D		,	15	28	ns

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	D	Tarran Ref		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	7
tw(TH)	Clock input T high pulse width		25	7		ns
tw(TL)	Clock input T low pulse width		25 ·	6		ns
tw(RD)	Direct reset RD pulse width		20	6		ns
tr	Clock pulse rise time			400	100	ns
t _{SU(D)}	Setup time DA~DD to T		. 20	3		ns
t _{SU(LOAD}	Setup time LOAD to T (Note 8)		20	6		ns
t _{SU(E)}	Setup time Ep, ET to T		20	8		ns
t _h (D)	Hold time D _A ∼D _D to T		3	0		ns
th(LOAD)	Hold time LOAD to T (Note 8)		3	-3 .		ns
t _{h(E)}	Hold time Ep, ET to T		3	-3		ns
trec(RD)	Recovery time RD to T		15	6		ns

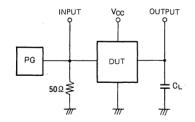
^{*:} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CCH} is measured with D_A, D_B, D_C, D_D, E_P, E_T, and R_D at 4.5V, LOAD at 0V, and T set from 0V to 4.5VA

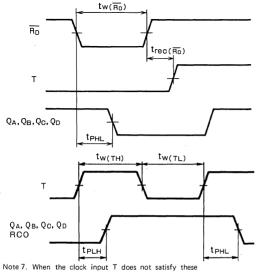
Note 4. I_{CCL} is measured with D_A, D_B, D_C, D_D, E_P, E_T and R_D, LOAD at 0V and T set from 0V to 4.5V.

Note 5. Measurement circuit



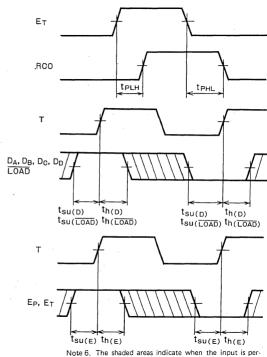
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) CL includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

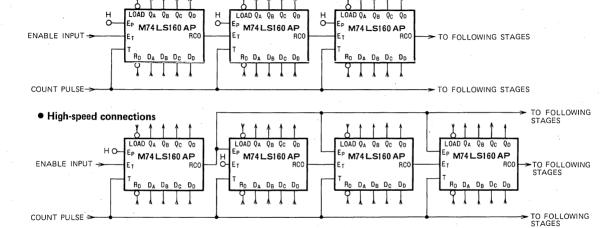


- Note 7. When the clock input T does not satisfy these standards, an incorrect counting operation may result.
- Note 8. When the load input LOAD setup time and hold time are not satisfied, the incorrect data may be preset. (When LOAD changes within ±5ns of the LOAD input transition from low to high, presetting may be made to low when the data input is high.)

APPLICATION EXAMPLE Cascade-connected divided-by-10ⁿ counter • Low-speed connections



Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.



M74LS161AP

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

DESCRIPTION

The M74LS161AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with direct reset input.

FEATURES

- Direct reset and synchronous preset inputs
- Enable input and carry output for cascaded operation
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range $(T_a = -20 \sim 75^{\circ}C)$

APPLICATION

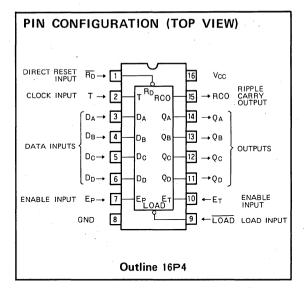
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPITON

When a counting pulse is applied to the T input, the 4-bit binary representation of the count is output at Q_A , Q_B , Q_C and Q_D in synchronization with the count pulse. Counting is done on the transition of the T input signal from low to high

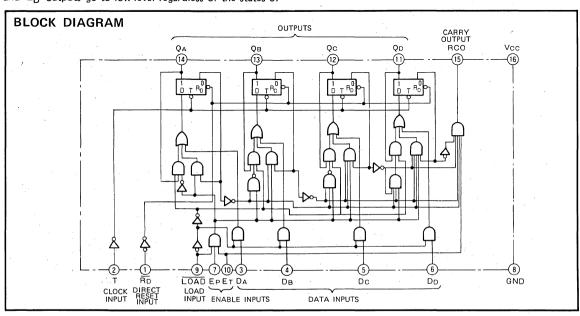
Presetting is accomplished in synchronization with the counting pulse. When preset data is applied to the D_A , D_B , D_C and D_D inputs, the load input \overline{LOAD} is made low, and T is changed from low to high, this data will appear in the Q_A , Q_B , Q_C and Q_D outputs, respectively regardless of the status of the enable inputs E_P and E_T , thereby presetting counter.

Resetting is performed asynchronously by setting the direct reset input $\overline{R_D}$ to low at which time the Q_A , Q_B , Q_C and Q_D outputs go to low-level regardless of the states of



the other inputs.

The ripple carry output RCO is high only when all Ω outputs and E_T are high. The two enable inputs E_P and E_T and the RCO carry output can be used to form an n-bit synchronous counter by means of cascade connection of several ICs (refer to the application example for the M74LS160AP).



SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

FUNCTION TABLE (Note 1)

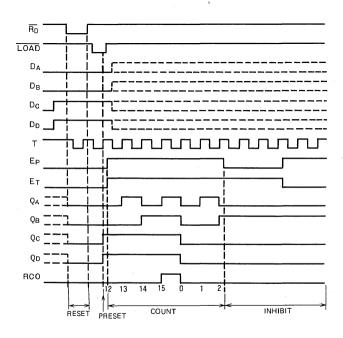
R _D	LOAD	ΕT	Eρ	Т	QA	Qв	Q _C	QD	RCO
L	×	×	X	×	L	L	L	L	Γ
н	L	L	×	1	D.	D-	n.	D-	٦
Н	L	Н	X	1	D _A D _B		D _C	D _D	L*
Н	Н	Н	Н	1	Cour	it			L*
Н	Н	L	X	X	Inhibit			L	
Н	Н	Н	L	X	Inhit	it			L*

Note 1: ↑: Indicates a transition from low to high (positive edge triggering).

* : RCO is normally low but is high when all Ω outputs and E_T are high simultaneously, i.e., RCO = Q_A • Q_B •Q_C•Q_D•E_T

X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		-65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumbel	Parameter			Limits				
Symbol	, rarameter	, arameta			Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
		V ₀ ∟≤0.4V	0		4	mA		
loL	Low-level output current	V ₀ L≦0.5V	. 0		8	.mA		

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D		Test condi	tions		Limits		
Зуптвоі	Parame	eter	l est condi	tions	Min	Тур*	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	· V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mÁ			-1.5	·V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8$ $V_{I} = 2V, I_{OH} = -400\mu$		2.7	3.4		٧
	Low-level output voltage	/	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V, V _I =2V	I _{OL} = 8mA		0.35	0.5	V
,		DA, DB, DC, DD, EP					20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7	, ∨			40	μΑ
I	High-level input current	RD					20	
Ιн	riigii-level ilipat carrent	DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} =5.25V, V _I =10\				0.2	mΑ
		Ro	· ·			0.1		
		Da, DB, Dc, DD, EP					-0.4	
l _{IL}	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4	V			-0.8	mA
		Ro					-0.4	'
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		20		- 100	mΑ
Іссн	Supply current, all outputs h	Supply current, all outputs high				18	31	mA
IccL	Supply current, all outputs to	ow	V _{CC} =5.25V (Note 4)			19	32	mA

^{* :} Typical values are for V_{CC} =5V and T_a =25°C

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	lest conditions	Min	Тур	Max	Oille
f _{max}	Maximum clock frequency		25	55		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation time,			20	,35	ns
t PHL	from input T to output RCO			20	35	ns
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t ÞHL	(when LOAD is high), from input T to outputs QA, QB, QC, QD	$C_L = 15pF$		16	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
t _{PHL}	(when \overline{LOAD} is low), from input T to outputs Q_A , Q_B , Q_C , Q_D			16	27	ns
tPLH	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns
t PHL	from input E _T to output RCO			8	14	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A , Q_B , Q_C , Q_D			15	28	ns

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test and district	Limits			Unit
Зуппоот		Test conditions	Min -	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		25	7		ns
tw(TL)	Clock input T low pulse width	7	25	6		ns
tw(RD)	Direct reset R _D pulse width		20	6		ns
tr	Clock pulse rise time			400	100	ns
t _{SU(D)}	Setup time DA - DD to T		20	3		ns
t _{SU(LOAD}	Setup time LOAD to T (Note 8)	7	20	6		ns
t _{SU(E)}	Setup time Ep, ET to T		20	8		ns
t _h (D)	Hold time $D_A \sim D_D$ to T		3	.0		ns
th(LOAD)	Hold time LOAD to T (Note 8)		3	– 3		ns
t _{h(E)}	Hold time Ep, ET to T		3	-3		ns
trec(RD)	Recovery time RD to T	1	15	6		ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

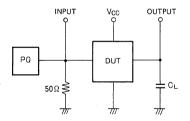
^{3:} Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T and R

and the LOAD input at 0V, changing the T input from 0V to 4,5V.

^{4:} Measurement of the high-level power supply current is performed with all data inputs, Ep, ET, RD and LOAD at 0V, changing the T input from 0V to 4.5V.

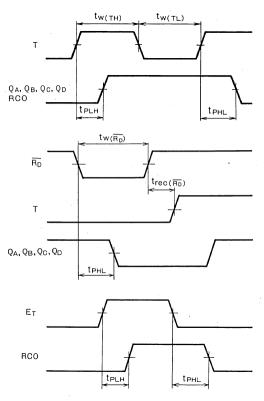
SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

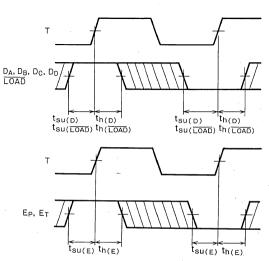
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C₁ includes probe and jig capacitance.

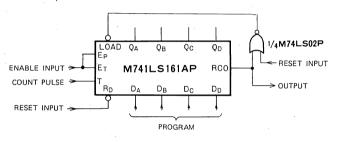
TIMING DIAGRAM (Reference level = 1.3V)





Note 6. The shaded area indicates the period within which switching may take place.

APPLICATION EXAMPLE Programmable divider



Note 7:	Reset is performed by applying countpulse with reset input
	high. $\overline{R_D}$ pin cannot be used since $Q_A{\sim}Q_D$ should be set low.

Da	DB	DC	D _D	Divide rate
L	L	L	L	1/16
Н	L	١	L	1/15
L	Н	اـ	L	1/14
Н	н	L	L	1/13
L	L	Н	L	1/12
Н	L	Н	·L	1/11
L	Н	Н	L	1/10
Н	Н	Н	L	1/9
L	L	L	Н	1/8
Н	L	L.	Н	1/7
L	Н.	L	Н	1/6
Н	н	L	. Н	1/5
L	L	Н	Ξ	1/4
Н	L	Н	I	1/3
L	Ξ	Н.	Н	1/2

DESCRIPTION

The M74LS162AP is a semiconductor integrated circuit containing a synchronous presettable decade counter function with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

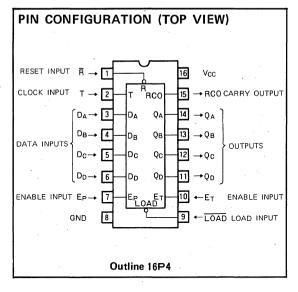
FUNCTIONAL DESCRIPTION

When the count pulses are applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A , Q_B , Q_C , Q_D synchronized with the count pulses. Counting is done when T changes from low to high.

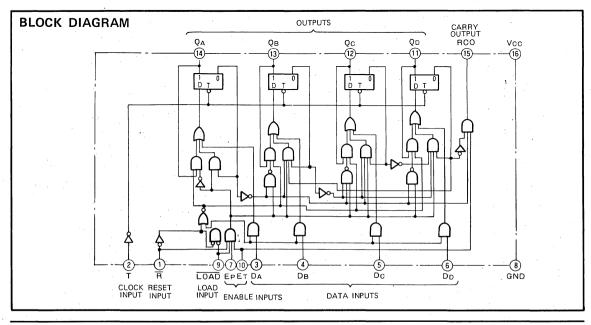
Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low and T is changed from low to high, the signals D_A , D_B , D_C and D_D appear at the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T , thereby presetting the counter. When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

Resetting is synchronized with the count pulses. Q_A , Q_B , Q_C and Q_D are set low by setting reset input \overline{R} low and by changing T from low to high.

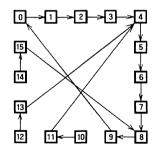
Carry output RCO is high only when QA is high, QB is



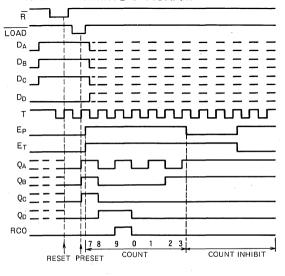
low, Q_C is low, Q_D is high and E_T is high. E_P , E_T and RCO are used for synchronous counter cascade connection and for configuration of an n-bit counter. (Refer to the application examples of the M74LS160AP.)



STATE DIAGRAM



OPERATION TIMING DIAGRAM



FUNCTION TABLE (Note 1)

R	LOAD	ΕŢ	EР	T	QΑ	Qв	Qc	QD	RCO
L	Х	Х	Х	1	L	L	L	L	L
Н	L	L	Х	1	Γ.	DB	Dc	DD	L
Н	L	Н	Х	1	DA	DB		UB	L*
Н	H.	Н	Н	1	Count			L*	
Н	н	L	Х	Х		Inh	ibit		L
Н	Н	Ι	L	Х		Inh	ibit		L*

Note 1 ↑: Transition from low to high (positive edge trigger)

*: RCO is normally low but is high when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. Therefore, RCO = Q_A·Q_B·Q_C·Q_D
•E_T

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = 20~ + 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state .	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃ .

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75℃, unless otherwise noted)

Complement	Deservator			Limits		
Symbol Parameter		,	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
I OL Low-level output current	V _{OL} ≤0.4V	0		· 4	mA	
	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Complete		0		Test conditions		Limits		
Symbol	Parameter		i est condi	tions	Min	Тур*	Max	Unit
ViH	High-level input voltage				. 2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage	High-level output voltage		BV (A	2.7	3.4		٧
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage	`	V _I =0.8V. V _I =2V	I _{OL} = 8mA		0.35	0.5	٧
		DA, DB, DC, DD, EP					20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7V				40 ⁻	μА
	High-level input current	R	1				40	
I _{IH}	righ-level input current	DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} =5.25V, V _I =10V				0.2	mA
	R		1	,		0.2		
		DA, DB, DC, DD, EP					-0.4	
I _{IL}	Low-level input current	LOAD, T, ET	$V_{CC} = 5.25V \cdot V_{I} = 0.4$	IV			-0.8	mA
		R	1				-0.8	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		20		- 100	mA
Іссн	Supply current, all outputs high.		V _{CC} =5.25V (Note 3)			18	31	mA
Iccl	Supply current, all outputs lov	ν .	V _{CC} =5.25V (Note 4)			19	32	mA

^{* :} All typical values are at Vcc = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter Test conditions		Limits		Unit	
Symbol	i arameter	rest conditions	Min .	Тур	Max]
f _{max}	Maximum clock frequency		25	55		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns
t PHL	from input T to output RCO			20	35	ns
t PLH	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t PHL	(when LOAD is high), from input T to outputs Q_A , Q_B , Q_C , Q_D	$C_L = 15pF$		16	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
· t _{PHL}	(when LOAD is low), from input T to outputs QA, QB, QC, QD			16	27	ns
t PLH	Low-to-high-level, high-to-low-level output propagation time,	•		8	14	ns
t _{PHL}	from input E _T to output RCO			. 8	14	ns

TIMING REQUIREMENT ($V_{CO}=5 \text{ V}$, $T_a=25 \text{ C}$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		l lada
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input Thigh pulse width		25	7		ns
tw(TL)	Clock input T low pulse width		25	. 6		ns
tr	Clock pulse rise time			400	100	ns
t _{su(D)}	Setup time DA~DD to T		20	3		ns
tsu(LOAD)	Setup time LOAD to T (Note 8)		20	6		ns
t _{su(R)} ·	Setup time R to T		20	11		ns
t _{su(E)}	Setup time Ep, E _T to T		20	8		ns
th(D)	Hold time DA~DD to T		3	0		ns
th(LOAD)	Hold time LOAD to T (Note 8)		3	- 3		ns
th(R)	Hold time R to T		3	- 8		ns
th(E)	Hold time Ep, E _T to T		3	- 5		ns

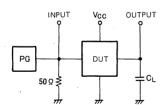
Note 2. All measurements should be done guickly and not more than one output should be shorted at a time.

Note 3. I_{CCH} is measured with D_A, D_B, D_C, D_D, E_P, E_T, and \overline{R} at 4.5V, LOAD at 0V, then 4.5V applied to T input. Note 4. I_{CCL} is measured with D_A, D_B, D_C, D_D, E_P, E_T and \overline{R} , \overline{R} , \overline{LOAD} at 0V and T set from 0V to 4.5V.

Note 5. Measurement circuit

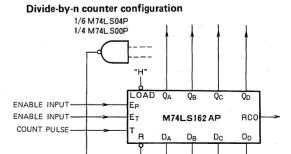
E_P, E_T

tsu(E) th(E)



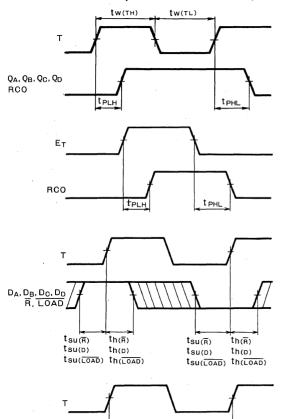
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, VP = 3Vp.p, Zo = 50 Ω .
- (2) C_L includes probe and jig capacitance

APPLICATION EXAMPLES



Divide-by-n counter	Pins connected to gate input
Ternary counter	Q _B
Divide-by 5 counter	Q _C
Divide-by-6 counter	QA, QC
Divide-by-7 counter	Q _B , Q _C
Divide-by-9 counter	Op.

TIMING DIAGRAM (Reference level = 1.3V)



Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.

tsu(E) th(E)

M74LS163AP

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS163AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs.
- Cascade connected enable input and carry output.
- High speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

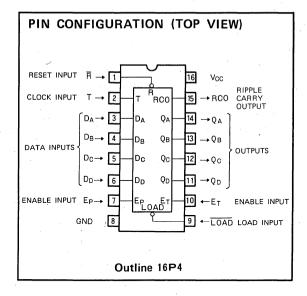
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

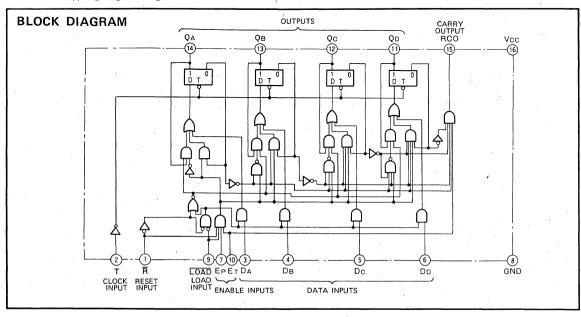
When count pulses are applied to the clock input T, the number of count pulses appears as a 4-bit binary code in the outputs Q_A , Q_B , Q_C , and Q_D synchronized with the count pulses. Counting is done when T changes from low to high.

Presetting is performed to synchronize the count pulse. When data is applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low, and T is changed from low to high, the signals D_A , D_B , D_C , and D_D appear at the Q_A , Q_B , Q_C , and Q_D outputs, respectively, regardless of the status of the enable inputs E_P and E_T , thereby presetting the counter.

Reset is performed, synchronized with the count pulse. When the reset input \overline{R} is made low, and T is changed from low to high, Q_A , Q_B , Q_C , and Q_D will be low.



The ripple carry output RCO is high only when $Q_A = Q_B = Q_C = Q_D$ = high and E_T = high. E_P , E_T and RCO are used when the counter is cascade connected in a synchronous manner to from an n-bit counter. (See the M74LS160AP application example).



FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

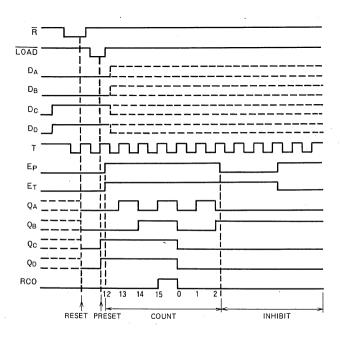
R	LOAD	ΕT	EР	Т	QΔ	QB	Q _C	QD	RCO
L	×	X ·	X	Ť	٦	L	L	L	L
Н	L	L	X	î		D _A D _B D _C	DD	L	
Н	L	Н	X	1	٨		De	56	L*
Н	Н	Н	н	1	Coun	it			, L *
Н	Н	L	X	X .	Inhib	L			
Н	Н	Н	L	X	Inhib	. ∟∗			

Note 1: † : transition from low to high level

* : RCO output is normally low-level, but RCO output is high-level when E_T input is high-level while the counter is in its maximum count state (HHHH).

X: irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C; unless otherwise noted)

Symbol						
Зуппрог	Paramet	er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА
	I _{OL} Low-level output current	V _{OL} ≤0.4V	0		4	mA
'OL		V _{OL} ≤0.5V	0		8	mA



FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal			Test condit	ione		Limits		11-14
Symbol	Parame	ter	rest condit	ions	Min	Тур*	Max	Unit
ViH	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage	Input clamp voltage		18 mA			-1.5	ν.
Voн	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8$ $V_{I} = 2V, I_{OH} = -400\mu$		2.7	3.4		٧
.,	Low-level output voltage	Output voltage V _{CC} =4.75V I _{OL} =4mA			0.25	0.4	V	
V_{OL}	Low-level output voltage		V _I =0.8V, V _I =2V	I _{OL} = 8 mA		0.35	0.5	V
	High-level input current	DA, DB, DC, DD, EP					20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7V				40	μА
		R				40		
ΊΗ		DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} =5.25V, V _I =10V				0.2	mA
		R					0.2	
		Da, DB, Dc, DD, Ep					-0.4	
lı_	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4	V			-0.8	mA
		R					-0.8	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		- 20		— 100	mA
Іссн	Supply current, all outputs high		V _{CC} =5.25V (Note 3)			18	31	mA
ICCL	Supply current, all outputs lo	Supply current, all outputs low				- 19	32	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions			Unit	
Symbol	, and the tel	rest conditions	Min	Тур	Max	Oilit
f _{max}	Maximum clock frequency		25	55		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns
t PHL	from input T to output RCO	. 1		20 .	35	ns
t PLH	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t PHL	(when LOAD is high), from input T to outputs QA, QB, QC, QD	$C_L = 15pF$		16	27	ns
t PLH	Low-tö-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns ·
t PHL	(when LOAD is low), from input T to outputs QA, QB, QC, QD			16	27 :	ns
t PLH	Low-to-high-level, high-to-low-level output propagation time,	And the second of the second		8	14	ns .
t PHL	from input E _T to output RCO			8	14	ns

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

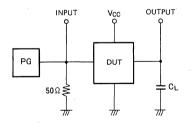
C	D	Total and distance		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		25	7		ns
tw(TL)	Clock input T low pulse width	1	25	6		ns
tr	Clock pulse rise time	1		400	100	ns
t _{SU(D)}	Setup time DA~DD to-T		20	3		ns
t _{SU(LOAD)}	Setup time LOAD to T (Note 7)		20	6		ns
t _{SU} (Ā)	Setup time R to T		20	11		ns
t _{SU(E)}	Setup time Ep, E _T to T		20	8		ns
t _{h(D)}	Hold time $D_A \sim D_D$ to T	1	3	0		ns
th(LOAD)	Hold time LOAD to T (Note 7)		3	- 3		ns
t _{h(鬲)}	Hold time R to T	1	3	- 8		ns
t _h (E)	Hold time Ep, ET to T	1	3	- 5		กร

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Ican in measured with DA, DB, Dc, DD, E†, R inputs at 4.5V, ICAD input one shorted and a momentary ground, then 4.5V, applied to T input.
 Ican is measured with DA, DB, Dc, DD, E†, R inputs at 4.5V, ICAD input grounded and a momentary ground, then 4.5V, applied to T input.
 Ican is measured with DA, DB, Dc, DD, E†, R incomplete inputs grounded and a momentary ground, then 4.5V, applied to T input.

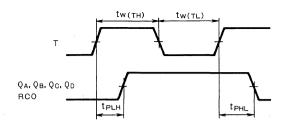
FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

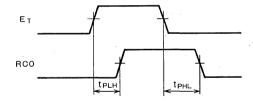
Note 5: Measurement circuit

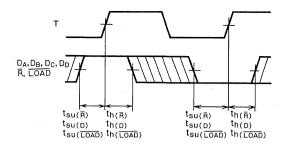


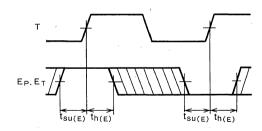
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_W = 500ns$, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





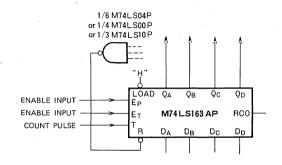




Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Variable modulo counter



Divide rate	Outputs connect to inputs of GATE
3	QB
5	Q _C
6	QA. QC
7	Q _B , Q _C
9	· Q _D
10	QA, QD
11	Q _B , Q _D
12	QA, QB, QD
13	Q _C , Q _D
14	QA, QC, QD
15	Q _B , Q _C , Q _D

M74LS164P

8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS164P is a semiconductor integrated circuit containing an 8-bit serial input-serial/parallel output shift register function with direct reset input.

FEATURES

- Serial input-serial/parallel output
- Direct reset input provided
- 8-bit for high space factor
- Input load factor of 1 for each input
- Wide operating temperature range (T_a= -20~+75°C)

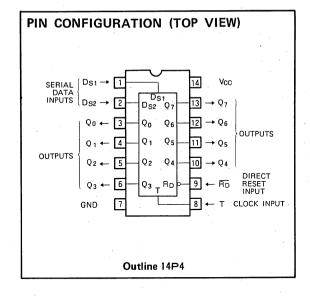
APPLICATION

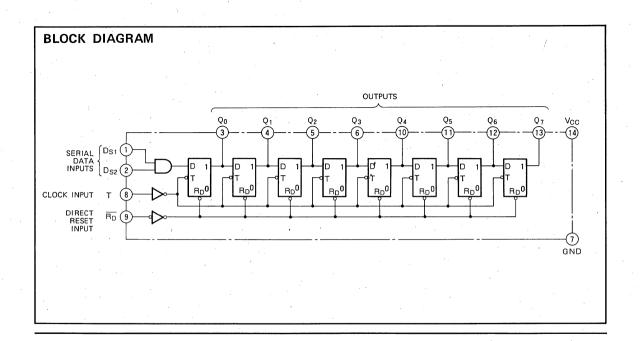
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is configured with 9 D-type edge-triggered flip-flops and the serial data inputs D_{S1} and D_{S2} logic product D_{S1} x D_{S2} represents the first-stage flip-flop data input. Outputs $Q_0 \sim Q_7$ are taken out from the flip-flop Q outputs. When D_{S1} and D_{S2} are both high and the clock pulse is applied to T, the high signal is shifted in sequence into Q_0 , Q_1 ... Q_7 . When either D_{S1} or D_{S2} or both are low and the clock pulse is applied to T, the low signal is shifted into Q_0 , Q_1 ... Q_7 in sequence. Shifting is performed when T changes from low to high.

When the direct reset input R_D is set low, all the outputs are reset low irrespective of the other input signals. $\overline{R_D}$ should be kept at high when using this device as a shift register.





8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

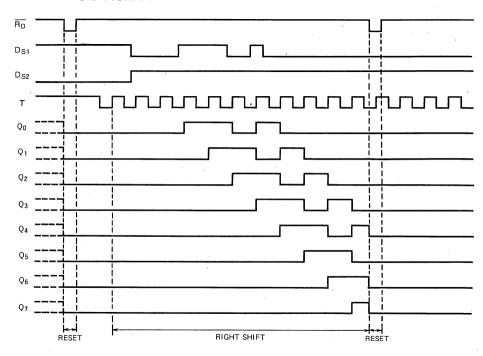
Operational mode	RD	Т	D _{S1}	D _{S2}	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Reset	L	Х	Х	×	L	L	L	L	L	L	L	L
	Н	1	L	L	L	Q ₀ ⁰	Q ₁ 0	Q2 ⁰	Q_3^0	Q_4^0	Q ₅ 0	Q ₆ 0
Right shift	Н	1	. Н	L	L	Q ₀ ⁰	Q1 ⁰	Q2 ⁰	Q ₃ ⁰	Q_4^0	Q5 ⁰	Q ₀
Trigitt stifft	Н	1	L	. н	L	Q ₀ ⁰	Q1 ⁰	Q ₂ ⁰	Q_3^0	Q_4^0	Q ₅ 0	Q ₆ 0
	Н	1	Н	Н	Н	Q ₀ ⁰	Q ₁ 0	Q_2^0	Q3 ⁰	Q ₄ ⁰	Q5 ⁰	Õ.0

Note 1 ↑: Transition from low to high (positive edge trigger)

 Q^0 : Level of output before the change from low to high

X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits				
Symbol	raranieter		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА		
1	I am land a dam a mana	V _{OL} ≤0.4V	0		_4	mA		
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA		

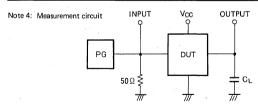
8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

					Limits			
Symbol	Parameter	l est condi	Test conditions			Max	Unit	
VIH	High-level input voltage		2			٧		
VIL	Low-level input voltage				0.8	V		
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-			-1.5	٧		
.,	High level automorphisms	V _{CC} =4.75V, V _I =0.	8V	2.7	3.5		.,	
Voн	High-level output voltage	V _I =2V, I _{OH} =-400µ	$V_1 = 2V$, $I_{OH} = -400 \mu A$				V	
.,		V _{CC} =4.75V	I _{OL} =4mA	100	0.25	0.4	V	
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V	
	TP-1-1-1	V _{CC} =5.25V, V _I =2.7V				20	μА	
ин	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA	
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4			-0.4	mA		
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0	-20		- 100	mA		
loc	Supply current	V _{CC} =5.25V (Note 3)		16	27	mA		

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Combal	Parameter	Test conditions		Limits			
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit	
f _{max}	Maximum clock frequency		25	50		MHz	
tpLH	Low-to-high-level, high-to-low-level output propagation	0 45 5		13	27	ns	
t _{PHL}	time, from input T to outputs Q ₀ ~Q ₇	C _L =15pF		· 14	32	ns	
+	Low-to-high-level, high-to-low-level output propagation	(Note 4)		18	36		
tpHL	time, input $\overline{R_D}$ to outputs $Q_0 \sim Q_7$			18	36	ns	

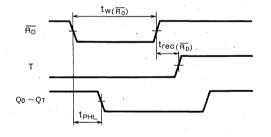


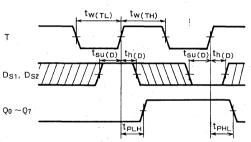
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Zo=50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

	Parameter	Test conditions			Unit	
Symbol		lest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		20	8		ns
tw(TL)	Clock input T low pulse width	1	20	.10		ns
tw(R□)	Direct reset RD pulse width		20	9		ns
tsu(D)	Setup time D _{S1} , D _{S2} to T		15	3		ns
th(D)	Hold time D _{S1} , D _{S2} to T	1	5	2		ns
trec (Āp)	Recovery time RD to T	1	20	-1		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



^{* :} All typical values are at V_{CC}=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with D_{S1} and D_{S2} at OV, 4.5V applied to T after RD has been set from OV to 4.5V.

DESCRIPTION

The M74LS165AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input — serial output shift register function.

FEATURES

- Parallel-to-serial data conversion
- Complementary output $(Q_7 \text{ and } \overline{Q_7})$
- Direct overriding load (data) input
- Clock inhibit input
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equip-

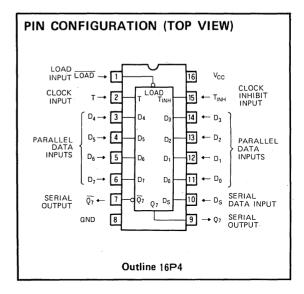
FUNCTIONAL DESCRIPTION

This device is configured from eight R-S-T flip-flop circuits and is designed to accept serial data input through D_S , or parallel data input through $D_0 \sim D_7$.

When D_S is used as the input, a clock pulse is applied to clock input T when load input \overline{LOAD} is high-level and the clock inhibit input T_{INH} is low-level.

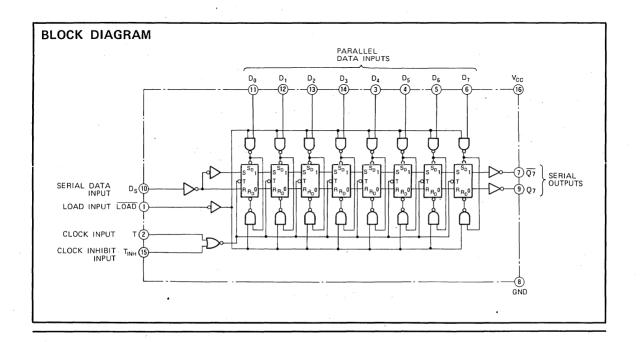
Shift operations are initiated upon T transiting from low to high, and the data present at D_S appears as an output pulse from Q_7 , \overline{Q}_7 of the 8th flip-flop circuit. The output at \overline{Q}_7 is always an inverted value of that present at Q_7 .

When $D_0 \sim D_7$ is used as the input, \overline{LOAD} is active-low. Since $D_0 \sim D_7$ are entered at the direct-set, direct-reset input of each flip-flop, read is executed regardless of the status of other inputs.



Care should be exercised to prevent the recording of erroneous data caused by a change in the value of $D_0 \sim D_7$ when \overline{LOAD} switches from low to high-value. Also, when T_{INH} is high, a shift operation will not be effected with clock pulse input. When T is low-level, and T_{INH} transits from low to high, a 1-bit shift operation will be executed.

M74LS165AP is an enhanced-performance version of M74LS165P having modified switching characteristics.



FUNCTION TABLE (Note 1)

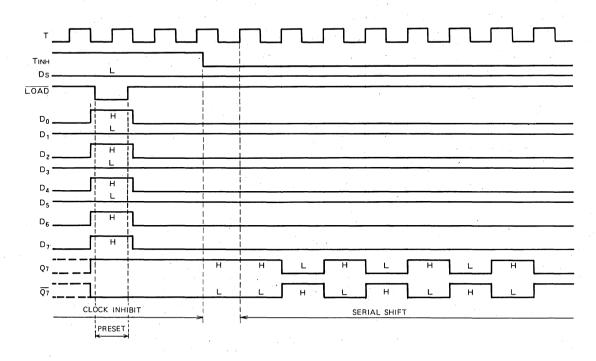
r	7	Inputs		T	Internal	Internal Outputs		
LOAD	TINH	Т	Ds	D ₀ ···D ₇	Q ₀	Q ₁	Q ₇	
L	х	Х	×	D ₀ D ₇	D.0	D ₁	D ₇	
, н	L	L	Х	×	Q ₀ 0	Q1 ⁰	Q7 ⁰	
н .	L	1	Н	х	Н	Q ₀ 0	Q ₆ 0	
Н	L	1	L	×	L	Q ₀ 0	Q ₆ 0	
Н	Н	X	` X	×	Q ₀ 0	Q1 ⁰	Q7 ⁰	

Note 1. X : Irrelevant

1: Transition from low to high (positive edge trigger)

Q0: Status of output before 1 of T

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions .	Limits	Unit
Vcc	Supply voltage		-0.5 ~ +7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Limits				
Symbol	Paramet	Talalite (Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
		V _{OL} ≤0.4V	0		4	mA		
lor	Low-level output current	V _{OL} ≤0.5V	. 0		8	mΑ		

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Combal	Parameter		Test conditions		Limits		
Symbol	rarameter	lest condi			Тур*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	Vcc=4.75V, lic=-	Vcc=4.75V, lic=-18mA			-1.5	٧
Vari	High-level output voltage	Vcc=4.75V, Vi=0.	8V	2.7			V
Vон	High-level output voltage,	VI=2V, IOH=-400	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.5		V
1/	Low-level output voltage	Vcc=4.75V	IoL=4mA		0.25	0.4	V
VoL	Low-level output voltage	Vi=0.8V , Vi=2V	IoL=8mA		0.35	0.5	· V
	High level input oursent	V _{CC} =5.25V, V _I =2.	7 V			20	μА
HII	High-level input current	$V_{CC} = 5.25 V$, $V_{I} = 10$	$V_{CC} = 5.25 \text{V}, V_{I} = 10 \text{V}$			0.1	mA
liL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 3)	V _{CC} =5.25V, V _O =0\	V _{CC} =5.25V, V _O =0V			- 100	mA
lcc	Supply current	Vcc=5.25V (Note 4)			18	30	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

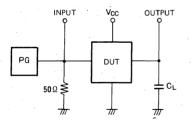
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the LOAD input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

Promise at	Parameter	Test conditions			Unit	
Symbol	· Talameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		25	38		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			17	35	ns
t PHL	time, from input \overline{LOAD} to outputs Q_7 and $\overline{Q_7}$			20	. 35	ns
t PLH	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF ·		14	25	ns
t PHL	time, from input T to outputs Q_7 and $\overline{Q_7}$	(Note 4)		13	25	ns
t PLH	Low-to-high-level, high-to-low-level output propagation	(Note 4)		9	25	ns
t PHL	time, from input D ₇ to output Q ₇			20	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			16	30	ns
t _{PHL}	time, from input D_7 to output $\overline{Q_7}$			12	25	ns

Note 4. Measurement Circuit

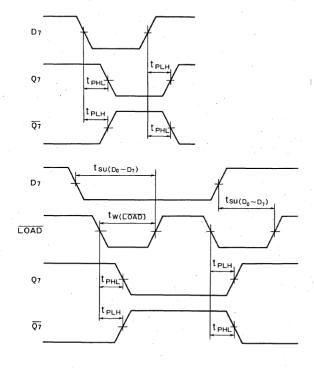


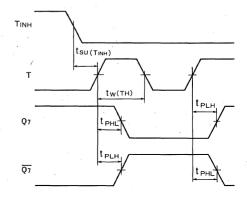
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50 Ω .
- (2) C_L includes probe and jig capacitance.

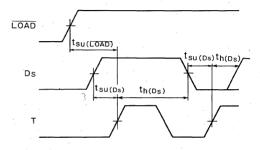
TIMING REQUIREMENTS (Voc=5V, Ta=25°C, unless otherwise noted)

0	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Oille
tw(T)	Clock pulse width		25	13		ns
tw (LOAD)	LOAD low-level pulse width] :	15	12		ns
tsu(T _{INH})	Setup time T _{INH} to T	<u> </u>	30	13		ns
tsu (D ₀ ~D ₇)	Setup time D ₀ ~ D ₇ to LOAD	1	10	9		ns
t _{su (Ds)}	Setup time D _S to T		20	8		ns
t _{Su (LOAD)}	Setup time LOAD to T		45	0		ns
th	Hold time	1	0	0		ns

TIMING DIAGRAM (Reference level = 1.3V)







MT4LS166AP

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS166AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input — serial output shift register function.

FEATURES

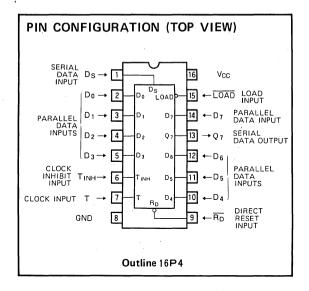
- Parallel-to-serial conversion
- Clock inhibit input
- Direct overriding reset
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

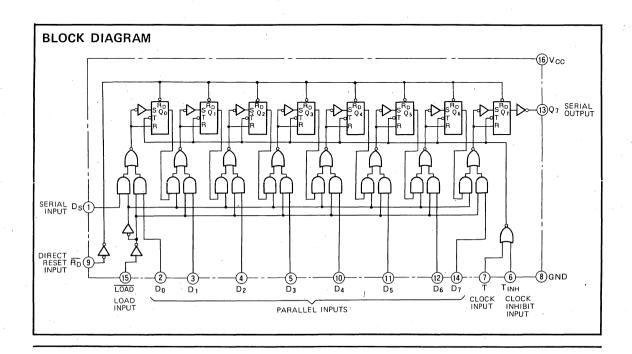
FUNCTIONAL DESCRIPTION

Parallel or serial input mode is selected via the load input $\overline{\text{LOAD}}$ signal. When $\overline{\text{LOAD}}$ is high-level, serial input enables the serial data input and couples the eight flip-flop for serial shifting with each clock pulse. Conversely, when $\overline{\text{LOAD}}$ is low-level, parallel data inputs $D_0{\sim}D_7$ are enabled and synchronous loading occurs on the next clock pulse. While during parallel loading, serial data flow in inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enable the clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other



clock input. The clock-inhibit input should be change to the high level only while $\frac{\text{the}}{R_D}$ clock input is high. The buffered, direct reset input $\frac{1}{R_D}$ overrides all other inputs, including the clock, and sets all flip-flop to zero.

M74LS166AP has been improved to resolve timing problems on LOAD input signal switching that occurred in the M74LS166P. Serial output Q7 has also been provided with a buffer to reduce noise, resulting in a change in specifications.



8-BIT SHIFT REGISTER

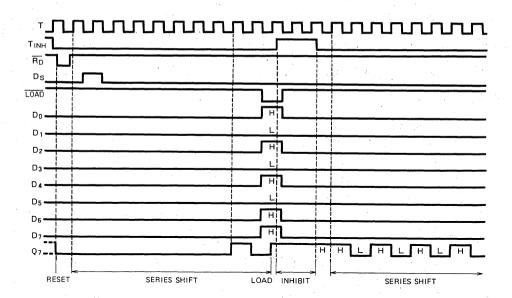
FUNCTION TABLE (Note 1)

		tr	1				t _{n+1}		
RD	1015	_	-		Parallel Inputs	Internal	outputs	0:	
n _D	LOAD	Tinh		Ds	D ₀ ···D ₇	Q ₀	Q ₁	Q ₇	
L	X	×	×	×	×	L	L	L	
Н	×	L	·L	Х .	×	Q ₀₀	Q ₁₀	Q70	
Н	L	L	1	×	D ₀ D ₇	D ₀	. D ₁	D ₇	
н	Н	L.	1	. н	×	Н	Qon	Q _{6n}	
H	Н	L	1	L	×	L	Qon	Q _{6n}	
н	X	Н	· 1	×	X	Q ₀₀	Q _{1n}	Q70	

Note 1. X : Irrelevant $\begin{array}{ccc} \uparrow : & \text{Transition from low to high (positive edge trigger)} \\ & Q_0 \sim D_7 : & \text{Indicates status prior to clock pulse at input D_0 thru D_7.} \\ & Q_0 \ldots Q_{70} : & \text{Indicates initial status of output Q_0 thru Q_7.} \\ & Q_0 \ldots Q_{7n} : & \text{Indicates initial status of Q_0 thru Q_7 immediately prior to clock input} \\ \end{array}$

Bit time after one clocking transition.

TIMING DIAGRAM



8-BIT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level output	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		11-14			
39111001	Farameter	, arameter			Max	Unit
Voc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
1	Low-level output current	V _{0L} ≤0.4V	0		4	mA
IOL		V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Tost condition				Unit	
Symbol	r al anietei	rest condition	Test conditions			Max	Omt
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.8\	/	2.7			V
Voн	· · · · · · · · · · · · · · · · · · ·	$V_1 = 2V$, $I_{OH} = -400 \mu A$	v •	2.7	3.5		٧ .
\/ -	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	High level in the second	V _{CC} =5.25V, V _I =2.7V	,			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
TIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V	1		1	-0.4	mA,
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 20		-100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			20	32	mA

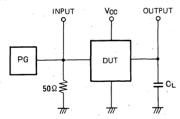
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	r al ame ter	rest conditions	Min	Тур	Max	Oiiit
f _{max}	Maximum clock frequency	C _L = 15pF (Note 5)	25	38		MHz
t _{PHL}	High-to-low-level output propagation time, from input $\overline{\mathrm{H}_D}$ to output Q_7			18	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	20	ns
t _{PHL}	time, from input T to output Q ₇			12	25	ns

 ^{*} I All typical values are at V_{CC} = 5V, T_a = 25°C.
 Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.
 3. With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

8-BIT SHIFT REGISTER

Note 4. Measurement circuit

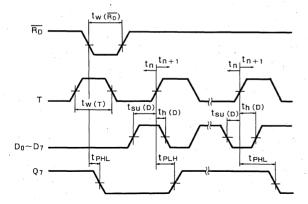


- (1) The pulse generator (PG) has the following (1) The pulse generator (PC) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P,P}, Z_O = 50Ω.
 (2) C_L includes jig and probe capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			11-3
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
tw _(T)	Clock pulse width		20	14		ns
tw(RD)	Reset pulse width		20	8		ns
tsu (D)	Setup time D _S , D ₀ ~D ₇ to T	 ·	20	12		ns
tsu(LOAD)	Setup time LOAD to T		30	12		ns
t _h	Hold time all inputs to T		. 0	-10		ns

TIMING DIAGRAM (Reference level = 1.3V)



TEST CONDITION TABLE

Data input for test	LOAD	Output tested	Bit time
D ₇	0∨	Q ₇	t _{n+1}
Ds	4.5V	Q ₇	t _{n+8}

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS170P is a semiconductor integrated circuit containing a 4-word by 4-bit register file function with open collector outputs.

FFATURES

- Separate read and write addresses for simultaneous data
- Read and write enable inputs provided
- Easy expansion of memory capacity using enable inputs
- Usable in AND-Tie connection (open collector outputs)
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

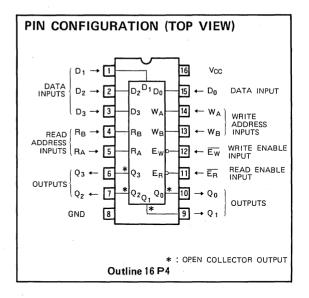
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 16 D-type latches as memory elements. Separate read and write inputs, both address and enable, allow simultaneous read and write operation, thereby enabling readout of other word contents during writing and writing into other words during readout resulting in increased speed. Open collector outputs make it possible to

The open collector outputs permit wire-AND connections for 256 outputs and expansion up to 1024 words.

M74LS170P has the same functions and pin connections as M74LS670P but the latter is provided with 3-state outputs.

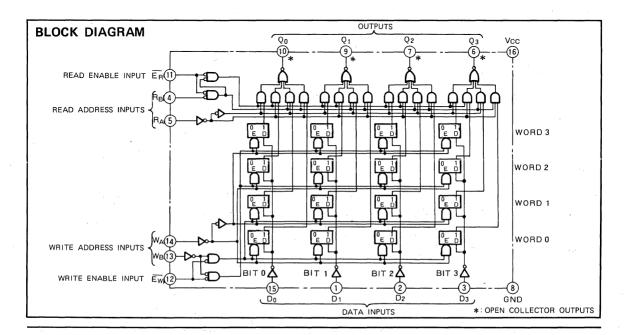


Writing Method

Writing into the bits is performed by specifying the words with address inputs W_A and W_B and by applying the data to data inputs D_0 , D_1 , D_2 and D_3 . The write enable input $\overline{E_W}$ is set low. No writing is performed when $\overline{E_W}$ is set high.

Readout Method

When the words are specified by read address inputs R_A and R_B , the contents of the stored bits appear in outputs Q_0 , Q_1 , Q_2 and Q_3 . Read enable input $\overline{E_B}$ is set low. When $\overline{E_B}$ is set high, all the outputs are set high.



4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

Writing Method

\	14/-	Ew		Word			
WA	WB	⊏w	0	1	2	3	
×	X	Н	Q ₀	Q0	Q ₀	Q0	
L	L	L	Q=D	Q0	Q ⁰	Q ⁰	
Н	L	L	Q ⁰	Q=D	Q ⁰	Qo	
L	Н	L	Q ⁰	Q0	Q=D	Q0	
Н	Н	L'	Q ⁰	δò	Q ⁰	Q=D	

Readout Method

RA	RB	ĒR	Q ₀	Q ₁	Q ₂	Q ₃
X	Х	Η	н	Н	Н	Н
L	L	الد	W ₀ B ₀	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃
Н	L	L	W ₁ B ₀	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃
L	Н	L	W ₂ B ₀	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃
Н	Н	L	W ₃ B ₀	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃

Note 1 Q⁰: No change in word contents.

Q=D: Data input contents are written into specified word.

W_XB_Y: Indicates word X and bit Y contents

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Únit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	٧
V ₀	Output voltage	High-level state	-0.5~+7	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Unit			
Symbol	rarameter		Min	Тур	Max	Jill
Vcc	Supply voltage		4.75	5	5.25	· V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	·or	Test condit	tions		Limits		Unit
Symbol	raramet	er	rest condit	tions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA	1.		-1.5	V
I _{OH}	High-level output current		V _{CC} =4.75V, V _I =0.8V V _I =2V, V _O =5.5V				100	μА
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VOL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$ $I_{OL} = 8mA$			0.35	0.5	V
		ER, Ew	V _{CC} =5.25V, V _I =2.7				40	
I _{IH}	High-level input current	Other inputs	VCC=5.25V, V ₁ =2.7	V			20	μΑ
.10	The state of the s	ER, EW	\/ F 25\/ \/ _ 10\	,			0.2	
	Othe	Other inputs	$V_{CC} = 5.25V, V_{I} = 10V$,			0.1	mΑ
hi.	Low-level input current	ER, Ew	V _{CC} =5.25V, V _I =0.4V				-0.8	-0.8
· · · · · · · · · · · · · · · · · · ·		Other inputs .					-0.4	mA
Icc	Supply current		V _{CC} =5.25V (Note 2)			25	40	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

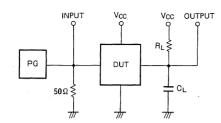
Note 2: I_{CC} is measured with W_A , W_B , R_A and R_B at 0V and with $D_0 \sim D_4$, $\overline{E_R}$ and $\overline{E_W}$ at 4.5V.

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	rest conditions	Min .	Тур	Max	Sint
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			13	30	ns
t _{PHL}	time, from input $\overline{E_R}$ to outputs Q ₀ , Q ₁ , Q ₂ , Q ₃			11	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			16	40	ns
t _{PHL}	time, from inputs R _A , R _B to outputs Q ₀ , Q ₁ , Q ₂ , Q ₃	$R_{L} = 2 k\Omega$		15	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 3)		16	45	ns
t _{PHL}	time, from input $\overline{E_W}$ to outputs Q_0 , Q_1 , Q_2 , Q_3			16	40	٠ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time			15	45	ns
tpHL	from inputs D_0 , D_1 , D_2 , D_3 to outputs Q_0 , Q_1 , Q_2 , Q_3			15	35	ns

Note 3: Measurement circuit



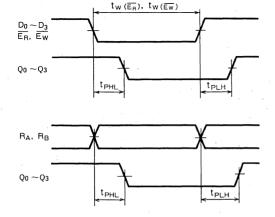
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

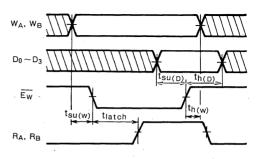
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Combal	D	Test conditions		Limits		
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
tw(ER)	Read enable input E _R pulse width		25	9		ns
tw(Ew)	Wright enable input E _W pulse width		25	9		ns
t _{su(D)}	D ₀ ~ D ₃ setup time with respect to $\overline{E_W}$		10	5		ns
t _{su(W)}	WA, WB setup time with respect to EW		15	– 2		ns
th(D)	D ₀ ~ D ₃ hold time with respect to E _W		15	0		ns
th(W)	WA, WB hold time with respect to EW		5	– 2		ns
tlatch	D ₀ ~ D ₃ latch time (note 4)		25	5		ns

Note 4: t_{LATCH} is the time required for storage when data is changed.

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS173AP

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS173AP is a semiconductor integrated circuit containing a 4-bit register with 3-state outputs.

FEATURES

- Data can be held irrespective of number of clock pulses
- Data are non-destructible with 3-state outputs
- Positive edge-triggering
- Direct reset input provided
- Easy bit expansion
- Wide operating temperature range (T_a = −20 ~ +75°C)

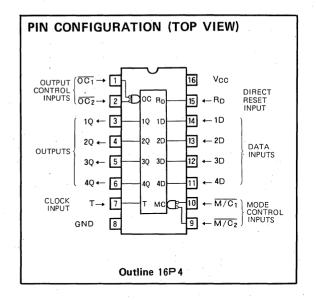
APPLICATION

General purpose, for use in industrial and consumer equipment.

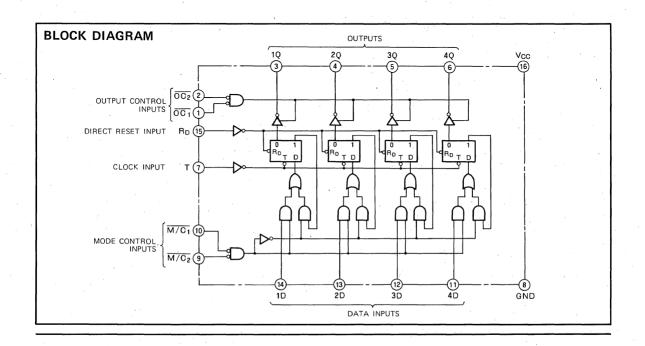
FUNCTIONAL DESCRIPTION

This device contains 4 edge-triggered D-type flip-flop circuits and direct reset input R_D and clock input T common to all circuits. When T changes from low to high, the information of data inputs 1D \sim 4D immediately before the change appears in outputs $1Q\sim4Q$ respectively in accordance with the function table.

When R_D is set high with mode control inputs $\overline{M/C_1}$ and $\overline{M/C_2}$ low, all the flip-flop outputs are low irrespective of the other inputs. When $\overline{M/C_1}$ or $\overline{M/C_2}$ is high, $10 \sim 40$



hold the status established when $\overline{M/C_1}$ and $\overline{M/C_2}$ are low, irrespective of the other signals. When $\overline{OC_1}$ or $\overline{OC_2}$ is high, $10 \sim 40$ are all put in the high-impedance state. In this case, the internal flip-flop status does not change because of the $\overline{OC_1}$ and $\overline{OC_2}$ input change. For use as a D-type flip-flop, set $\overline{M/C_1}$, $\overline{M/C_2}$, $\overline{OC_1}$ and $\overline{OC_2}$ all low.



4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

R _D	Т	M/C ₁	M/C ₂	D	0
- '''	<u> </u>	111701	, 52		
Н	X	×	X	X	· L
. г	L	X	×	×	Q ⁰
L	1	, н	×	X	Q ⁰
L	1	Х	Н	Х	Q ⁰
L	1	L	L	L	٦
L	1	L	L	Н	н

Note 1 High-impedance state when \overline{OC}_1 and/or \overline{OC}_2 are high.

† : Transition from low to high (positive edge trigger)

X : Irrelevant

Q⁰: Level of Q before the indicated steady-state input conditions were established

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Unit				
Symbol	Faianetei		Min	Тур	Max	Unit	
Voc	Supply voltage	}	4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≥2.4V	0		-2.6	mΑ	
	I _{OL} Low-level output current	V ₀ L≦0.4V	0		12	mA	
IOL .		V _{OL} ≤0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (T_a = -20~+75°C, unless otherwise noted)

C b l	Description	T	liai		Limits		Unit
Symbol	Parameter	Test conditions		Min	Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage	-				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.	8V	2.4	2.1		
VoH	righ-level output voltage	V ₁ =2V , I _{OH} =-2.6n	nA	2.4	3.1		·V
	Level autout valtage	V _{CC} = 4.75 V	I _{OL} = 12mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V	'. V ₀ =2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} 5.25V, V _I =2V	, V ₀ =0.4V			- 20	μА
	I link in all in a second	V _{CC} =5.25V, V _I =2.	7V			· 20	μА
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
1 _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4 V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-30	•	- 130	mA
loc	Supply current	V _{CC} =5.25V (Note 3)		17	30	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured after $\overline{M/C_1}$, $\overline{M/C_2}$, 1D 4D and $\overline{OC_2}$ have been set to OV, T and $\overline{OC_1}$ to 4.5V and R_D from OV to 4.5V.

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

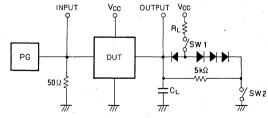
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

	Parameter	Test conditions			Limits		Unit
Symbol	Parameter	lest conditions		Min	Тур	Max	Unit
fmax	Maximum clock frequency ,			-30	35		MHz
t _{PHL}	High-to-low-level output propagation time, from input R_D to output Q	C _L =45pF	(Note 4)		21	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				20	25	ns
t _{PHL}	time from input T to output				26	30	ns
t _{PZH}	Output enable time to high-level	O45-5 B6670	(Nines 4)		14	23	ns
t _{PZL}	Output enable time to low-level	$C_L=45pF, R_L=667\Omega$	(Note 4)		15	27	ns
t _{PHZ}	Output disable time from high-level	C _L =5pF, R _L =667Ω	(Note 4)		11	17	ns
t _{PLZ}	Output disable time from low-level		(Note 4)		9	17	ns

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

6	Parameter	Total and distance		Unit		
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input T pulse width		20	4		ns
t _{su (D)}	Setup time 1D ~ 4D to T		17	3		ns
t _{h (D)}	Hold time 1D ~ 4D to T		6	3		ns
t _{su(M/C)}	Setup time M/C ₁ , M/C ₂ to T		35	20		ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T	,	0	- 12		ns
tw(RD)	Direct reset R _D pulse width		20	10		ns
trec	Recovery time R _D to T		. 15	12		ns

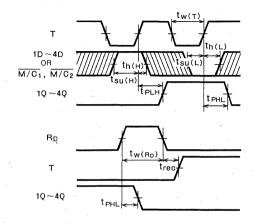
Note 4: Measurement circuit

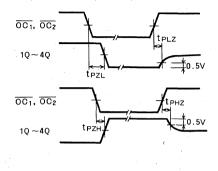


Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t PHZ	Closed	Closed
	t _{PZH} t _{PZL}	t PZH Open t PZL Closed t PLZ Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
- $V_P = 3V_{P.P}, Z_0 = 50\Omega.$
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$.
- (3) C_Lincludes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

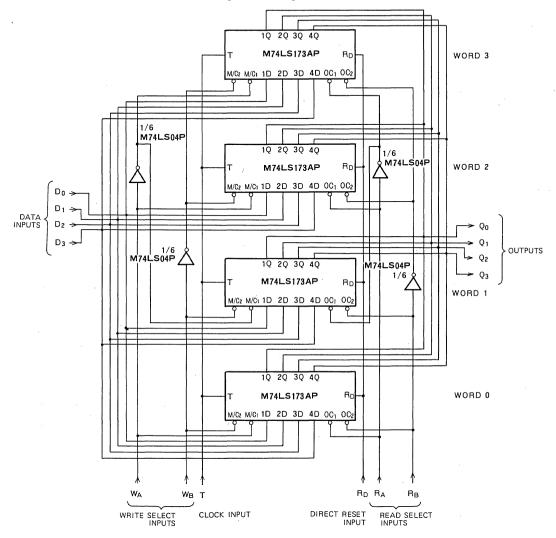




4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

APPLICATION EXAMPLE

Shown below is a schematic of a 4-bit x 4-word register file using the M74LS173AP.



Writing method

14/-	\w/.		WC	RD	
WB	WA	0	. 1	2	3
L	L	Q = D	Q ⁰	Ó ₀	Q ⁰
L .	Н	Q ⁰	Q = D	Ó ₀	Q ⁰
Н	L	Ó ₀	Q ⁰	Q = D	Q ⁰
Н	Н	Q ⁰	Q ⁰	O ₀	Q = D

Readout method

Rв	RA	Qo	Q ₁	02	Q ₃
L	· L	W ₀ D ₀	W ₀ D ₁	W ₀ D ₂	W ₀ D ₃
L	H .	W ₁ D ₀	W ₁ D ₁	W ₁ D ₂	W_1D_3
Н	L	W ₂ D ₀	W ₂ D ₁	W ₂ D ₂	W ₂ D ₃
Н	Н	W ₃ D ₀	W ₃ D ₁	W ₃ D ₂	W ₃ D ₃

HEX D-TYPE FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS174P is a semiconductor integrated circuit containing 6 D-type edge-triggered flip-flop circuits with common clock input T and direct reset input $\overline{R_D}$ as well as discrete data input D.

FEATURES

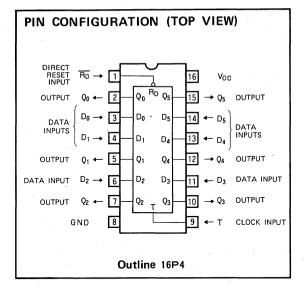
- Positive edge-triggering
- Common clock and direct reset inputs for all 6 circuits
- O and O outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change appears in the output Q in accordance with the function table. When $\overline{R_D}$ is low, all Q are low, regardless of the status of the other input signals. For use as a D-type flip-flop, keep $\overline{R_D}$ high.



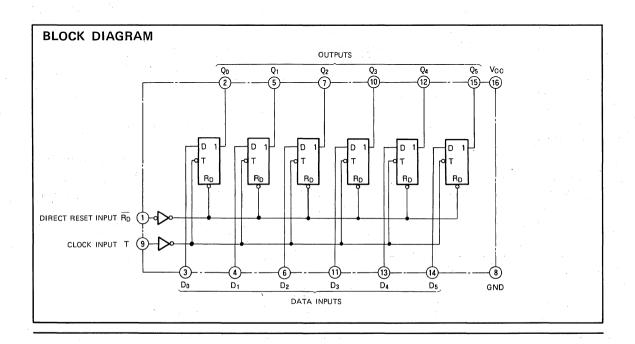
FUNCTION TABLE (Note 1)

			A
RD	Т	D	Q
·L	X	X	L
Н	. 1	H	Н
Н	1	L	L
Н	L.	Х	Q ⁰

Note 1: †: transition from low to high level

Q⁰: level of Q before the indicated steady-state input conditions were established

X : irrelevant



HEX D-TYPE FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧,	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	. V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

C	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА		
	Low-level output current	V ₀ L≦0.4V	0		4	mA		
ToL Low-level output current	V _{OL} ≦0.5V	0		. 8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 ^{\circ}$), unless otherwise noted)

					Limits		Unit
Symbol	Parameter	Test condi	tions	Min	Тур*	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	V _{CC} =4.75V, I _{IC} =-18mA			- 1.5	V
.,	High lovel autout valtage	V _{CC} =4.75V, V _I =0.8	/	2.7 3.4			V
Vон	High-level output voltage	$V_1 = 2 V, I_{OH} = -400 A$	ıΑ				. v
		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
	High level in put a second	V _{CC} =5.25V, V _I =2.7	/			20	μΑ
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V .			-0.4	mA
los	Short-circuit output current Note 2	V _{CC} =5.25V, V _O = 0 \	,	-20		— 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			16	26	mA

^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25°C.

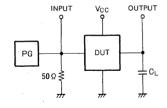
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with D, $\overline{R_D}$ inputs at 4.5V and a momentary ground, then 4.5V, applied to T input

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_a = 25 ^{\circ}\text{C}$, unless otherwise noted)

Combal	Danasasas	Total	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30	47		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	30	ns
t _{PHL}	time, from input T to output Q	C _L = 15pF (Note 4)		10	30	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q			11	35	ns

Note 4: Measurement circuit



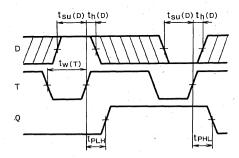
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance,

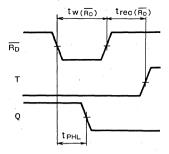
HEX D-TYPE FLIP FLOPS WITH RESET

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25 °C, unless otherwise noted)

	Symbol Parameter	7		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input T pulse width		20	4		ns
tw (RD)	Reset input RD pulse width		20	6		ns
t _{su(D)}	Setup time D to T	•	20	2		ns
th(D)	Hold time D to T		5	.0		ns
trec(RD)	Recovery time RD to T		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

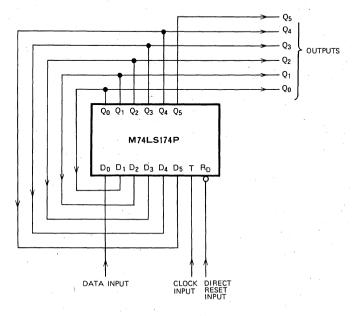




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

6-bit shift register



M74LS175P

QUADRUPLE D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS175P is a semiconductor integrated circuit containing 4 positive edge-triggered D-type flip-flops with common clock input T and direct reset input \overline{R}_D and discrete data inputs D.

FEATURES

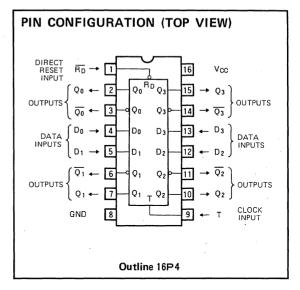
- Positive edge-triggering
- Clock and direct reset inputs common to 4 circuits
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and \overline{Q} in accordance with the function table. By setting $\overline{R_D}$ low, all the Q and \overline{Q} outputs are set low and high, respectively, irrespective of the status of the other inputs signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

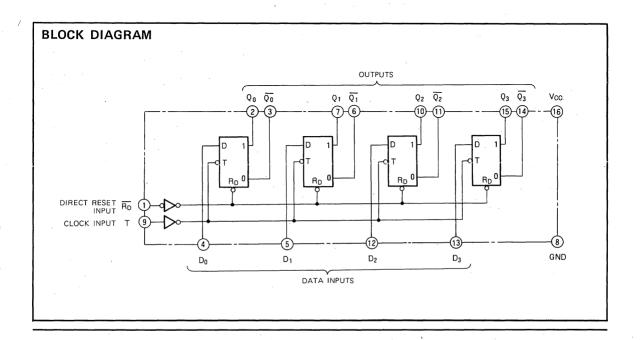


FUNCTION : TABLE (Note 1)

			0	
R _D	1	D	Ų	Ų
Ļ	X	Х	L	Н
Н	1	Н	Н	L
Н	1	L	L	Н
Н	L	X	Qo	Q0

Note 1 X : Irrelevant

- †: Transition from low to high level (positive edge trigger)
- Q0: Level of Q before the indicated steady-state input conditions were established.



QUADRUPLE D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Limits		Unit	
Symbol	ratanieter		Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

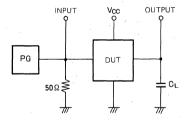
Symbol	Parameter	T	*!		Limíts		Unit	
Symbol	rarameter	Test condi	tions	Min	Typ *	Max	Onit	
ViH	High-level input voltage						V :	
VIL	Low-level input voltage			1		0.8	V	
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	. V	
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.	8V	2.7	2.4		V	
V _{OH}	High-level output voltage	V _I =2V, I _{OH} =-400,	$V_1 = 2V \cdot I_{OH} = -400 \mu A$		3.4		V	
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧	
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧	
		V _{CC} =5.25V, V _I =2.	7 V			20	μА	
Чн	High-level input current	V _{CC} =5.25V, V _I =10	V .			0.1	mA	
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	.mA	
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0\	/	- 20		-100	mA	
Icc	Supply current	V _{CC} =5.25V (Note 3)		1	. 11	18	· mA	

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS ($V_{CO}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			
Symbol	1 didiffeter	rest conditions	Min	Min Typ Max		Unit	
f _{max}	Maximum clock frequency	•	30	50		ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	$C_1 = 15 pF$ (Note 4)		10	25	ns	
t _{PHL}	time, from T to Q, Q	CL 15pr (Note 4)		12	25	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	30	ns	
t _{PHL}	time, from $\overline{R_D}$ to Q. \overline{Q}			19	30	ns	

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

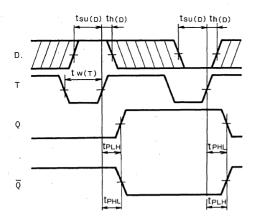
Note 3: I_{CC} is measured with 4.5V applied to D and $\overline{R_D}$ after T is set to 0V.

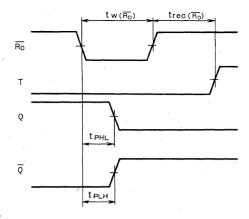
QUADRUPLE D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	7 al allietei	rest conditions	Min	Тур	Max	Oiiit
tw(T)	Clock input T pulse width		20	4		ns
tw(RD)	Direct reset input pulse width		20	7		ns
t _{SU(D)}	Setup time high to T		20	2		ns
t _h (D)	Hold time high to T		. 5	0		ns
trec(RD)	Recovery time for direct reset input		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

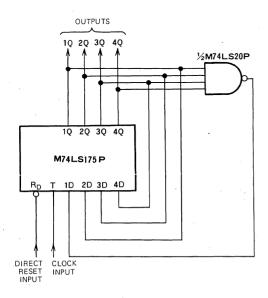


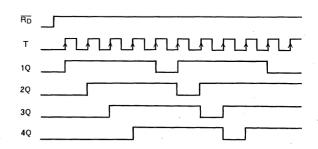


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Timing pulse generator





M74LS190P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS190P is a semiconductor integrated circuit containing a decade up/down counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control input
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (fmax = 38MHz typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

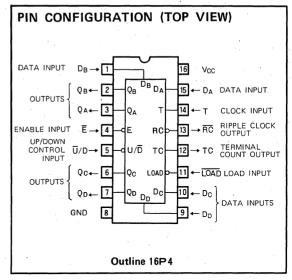
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

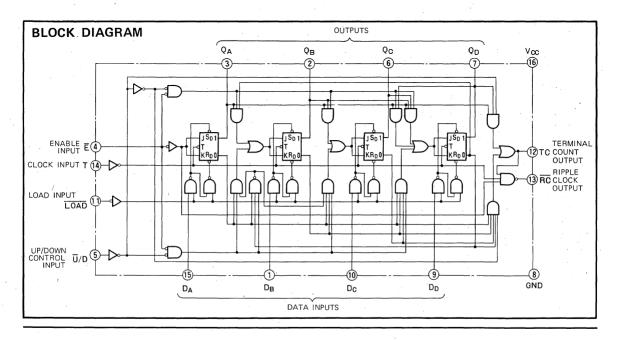
When enable input \overline{E} is low, load input \overline{LOAD} is high and the count pulses are applied to clock input T, the number of count pulses appear as a BCD code in the outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses. When the up/down control input \overline{U}/D is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs DA, DB, DC and DD and by setting \overline{LOAD} low, the DA, DB, DC and DD signals appear in outputs QA, QB, QC and QD irrespective of the status of the other inputs and the count can be preset. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10_2 or higher,



High appears in the terminal count output TC during count-up while 9_2 appears in Q_A , Q_B , Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output \overline{RC} only when \overline{E} and T are low and 9_2 appears in outputs Q_A , Q_B , Q_C and Q_D during count-up or Q_D appears in the outputs during count-down. \overline{E} , TC and \overline{RC} are used when cascade-connecting the counter. (Refer to application examples.)

 \overline{E} can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for \overline{U}/D when T is high.



SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

LOAD	Ē	Ū/D	T	QA	Q _B	Q _C	QD	
L	×	Х	X	DA	DB	Dc	D _D	
Н	L	L	1	Count-up				
н	L	н	1	Count-down				
Н	Н	Х	X	Inhibit				

Note 1. ↑: Transition from low to high x : Irrelevant

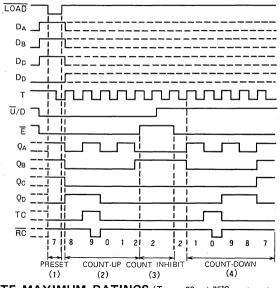
Ē	TC(1)	Т	RC
L	I	L	L
L	Н	Н	н
Н	Х	. X	Н
X	L	Х	Н

TC is the output but the signal generated internally by

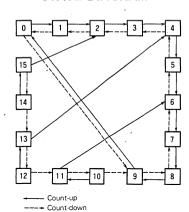
the following logical expression.

TC = $\overline{Q}_{A} \cdot \overline{Q}_{B} \cdot \overline{Q}_{C} \cdot \overline{Q}_{D} \cdot \overline{(U/D)}$ Count-up TC = $\overline{Q}_{A} \cdot \overline{Q}_{B} \cdot \overline{Q}_{C} \cdot \overline{Q}_{D} \cdot \overline{(U/D)}$ Count-down

OPERATION TIMING DIAGRAM



STATE DIAGRAM



Details of timing diagram

(1) Preset to 13

(2) Count-up 8, 9, 0, 1, 2

(3) Count inhibit

(4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage	·	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range	-	-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	0.5		Limits		Unit
Symbol	raidiley		Min	Тур	Typ Max	
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
I _{OL} Low-level outp	Low-level output current	V _{OL} ≤0.5V	0		8	mA

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

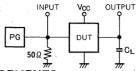
ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Constant	Dane	meter	Tost condit	ione	Limits			Unit
Symbol	Parar	neter	Test conditions		Min.	Typ *	Max	Unit
ViH	High-level input voltage				2			٧
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8 mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-400μ		2.7	3.4		٧
Vol	Low-level output voltage	,	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
	, , , , , , , , , , , , , , , , , , , ,		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =2.7V	v .	-		20 60	μΑ
ΙΗ	High-level input current	T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =10V				0.1	mA
hL.	Low-level input current	T, LOAD, U/D, Da~DD	V _{CC} =5.25V, V _I =0.4V	·			0.3 - 0.4	
		Ē		· · · · · · · · · · · · · · · · · · ·			-1.2	///A
los	Short-circuit output curre	nt (Note 2)	$V_{CC}=5.25V, V_0=0V$		-20		- 100	mΑ
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	35	mA

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Combal	Parameter	Test conditions	i i	Limits		Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit _
f _{max}	Maximum clock frequency		20	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			19	33	ns
tpHL	time, input LOAD to outputs QA, QB, QC, QD			25	50	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			11	32	ns
tpHL	time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD			25	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		11	20	ns
t _{PHL}	time, from input T to output RC			11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	· · ·		12	24	ns
t _{PHL}	time, from input T to outputs QA, QB, QC, QD			14	36	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·	!	20	42	ns
t _{PHL}	time, from input T to output TC			24	52	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation		,	22	45	ns
tehL	time, from input U/D to output RC			20	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		15	33	ns
t _{PHL}	time, from input $\overline{\mathbf{U}}/\mathbf{D}$ to output \mathbf{TC}			15	33	ns
tpLH	Low-to-high-level, high-to-low-level output propagation]		10	33	ns
tpHL	time, from input $\overline{\mathbf{E}}$ to output $\overline{\mathbf{RC}}$			11	33	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

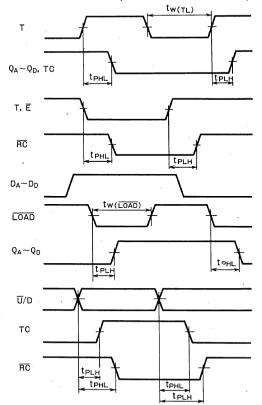
Symbol	Parameter	Test conditions	Limits			
	rarameter	rest conditions	Min	Тур	Max	Unit
tw(TL)	Clock input T low pulse width		25	9		ns
tw(LOAD)	Load LOAD pulse width		35	10		ns
tr	Clock pulse rise time			2000	100	ns
t _{SU(D)}	Setup time DA~DD to LOAD		20	9		ns
t _{SU(ĒL)}	Setup time E low to T	1	40	24		ns
th(D)	Hold time D _A ∼D _D to LOAD		5	.0		ns
th(EL)	Hold time E low to T	1	5	2		ns
trec(LOAD)	Recovery time LOAD to T		20	16		ns

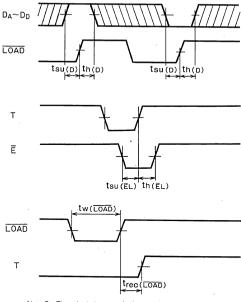
^{* :} All typical values are at V_{CC} = 5V , T_0 = 25°C. Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. Icc is measured with all the inputs at OV.

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

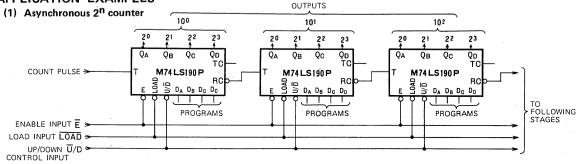
TIMING DIAGRAM (Reference level = 1.3V)

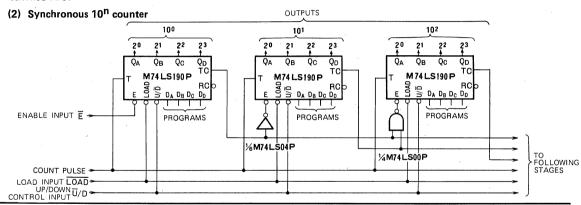




- Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.
- Note 6. The shaded area with the arrows indicate the direction of when the input is permitted to change.

APPLICATION EXAMPLES





M74LS191P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS191P is a semiconductor integrated circuit containing a synchronous 4-bit binary (hexadecimal) counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control inputs
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (fmax = 40MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

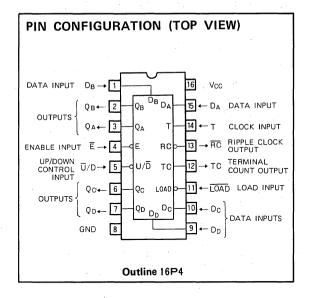
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

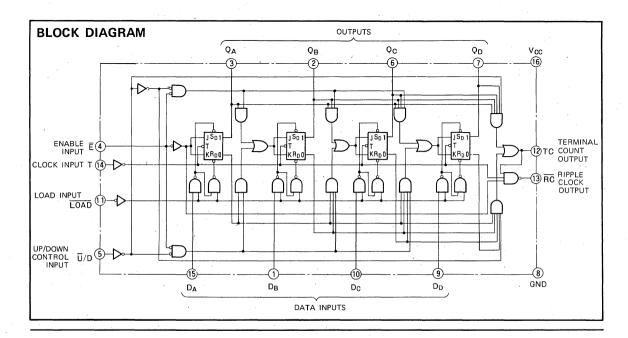
When enable input E is low, load input \overline{LOAD} is high and the count pulses are applied to clock input T, the number of count pulses appears as 4-bit pure binary code in the outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses. When the up/down control input \overline{U}/D is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} low, the D_A , D_B , D_C and D_D signals appear in outputs Q_A , Q_B , Q_C and Q_D irrespective of the status of the other inputs and the counter can be preset.



High appears in the terminal count output TC during count-up while 15_2 appears in Q_A , Q_B , Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output \overline{RC} only when \overline{E} and T are low and 15_2 appears in outputs Q_A , Q_B , Q_C and Q_D during count-up or Q_2 appears in the outputs during count-down. \overline{E} , TC and \overline{RC} are used when cascade-connecting the counter. (Refer to application example.)

 \overline{E} can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for \overline{U}/D when T is high.



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

LOAD	Ē	Ū/D	Т	QΑ	Qв	Qc	QD		
L	Х	Х	Х	DA	DB	Dc	DD		
Н	L	L	1	Count-up					
Н	L	Н	1	Count-down					
Н	Н	X	Х	Inhibit	t				

Note 1 ↑: Transition from low to high level

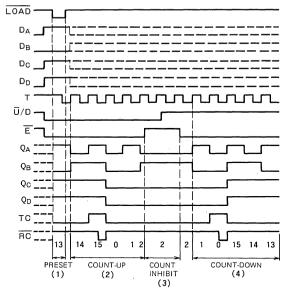
X: Irrelevant

Ē	TC ⁽¹⁾	Т	RC
L	. Н	L	١
L	Н	н	I
Н	Х	Х	Н
Х	L	Х	H

(1) TC is the output but the signal generated internally by the following logical expression.;

TC = $\overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{U}/D)$ Count-up TC = $\overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{U}/D)$ Count-down

OPERATION TIMING DIAGRAM



Details of timing diagram

- (1) Preset to 13 (3) Count inhibit
- (2) Count-up 14, 15, 0, 1, 2
- (4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	D			Limits		Unit			
Symbol	Paramete	er	Min	Тур	Max	·			
Vcc	Supply voltage		. 4.75	5	5.25	V			
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μА			
	Low-level output current	V ₀ L≦0.4V	0		4	mA			
TOL	Low-level datpat current	V _{0L} ≤0.5V	0		8	mA			

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS (Ta = −20~+75°C, unless otherwise noted)

0	,		T		-	Limits		- Unit
Symbol		Parameter	Test condit	ions	Min	Typ *	Max	
VIH .	High-level input vo	ltage			2	,		V
VIL	Low-level input vo	Itage		1		: .	0.8	V
Vic	Input clamp voltag	je .	V _{CC} =4.75V, I _{IC} =-18	8mA	i		-1.5	V
Voн	High-level output	output voltage $ \begin{array}{c} V_{CC}{=}4.75 \text{V, } V_{I}{=}0.8 \text{V} \\ V_{I}{=}2 \text{ V, } I_{OH}{=}-400 \mu \text{A} \end{array} $		2.7	3.4		٧	
V _{OL}	Low-level output	voltage	V _{CC} =4.75V			0.25	0.4	
	High-level	$T, \overline{LOAD}, \overline{U}/D, D_A \sim D_D$ \overline{E}	V _{CC} =5.25V, V _I =2.7V	1	· · · · · ·		20 60	μА
l _{IH} .	input current	T, TOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =10V	•			0.1	. mA
l _{IL}	Low-level input current	T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =0.4V				-0.4 -1.2	mΑ
los	Short-circuit outp	ut current (Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	35	mA

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

Symbol	Para meter	Test conditions		Limits		Unit
·	Talameter	i est conditions		Тур	Max	Oill
fmax	Maximum clock frequency		20	40		MHz
t pl H	Low-to-high-level, high-to-low-level output propagation			19	33	ns
t PH L	time, from input LOAD to outputs QA, QB, QC, QD	•		25	50	ns
t PL H	Low-to-high-level, high-to-low-level output propagation			11	32	ns
t _{PHL}	time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD	•		25	40	ns
t _{PL} H	Low-to-high-level, high-to-low-level output propagation			11	20	ns
tphL	time, from input T to output RC			11	24	ns
t _{PL} H	Low-to-high-level, high-to-low-level output propagation			12	24	ns
tphL	time, from input T to outputs QA, QB, QC, QD	C _L = 15pF (Note 4)		14	36	ns
t _{PL H}	Low-to-high-output, high-to-low-level output propagation			20	42	ns
tphL	time, from input T to output TC			24	52	ns
t _{PL H}	Low-to-high-level, high-to-low-level output propagation	•		22	45	ns
tPHL	time, from input U/D to output RC			20	45	ns .
t _{PL H}	Low-to-high-level, high-to-low-level output propagation			15	33	ns
tphL	time, from input U/D to output TC			15	33	ns
t _{PL H}	Low-to-high-level, high-to-low-level output propagation			10	33	ns
tphL	time, from input E to output RC			11	33	ns

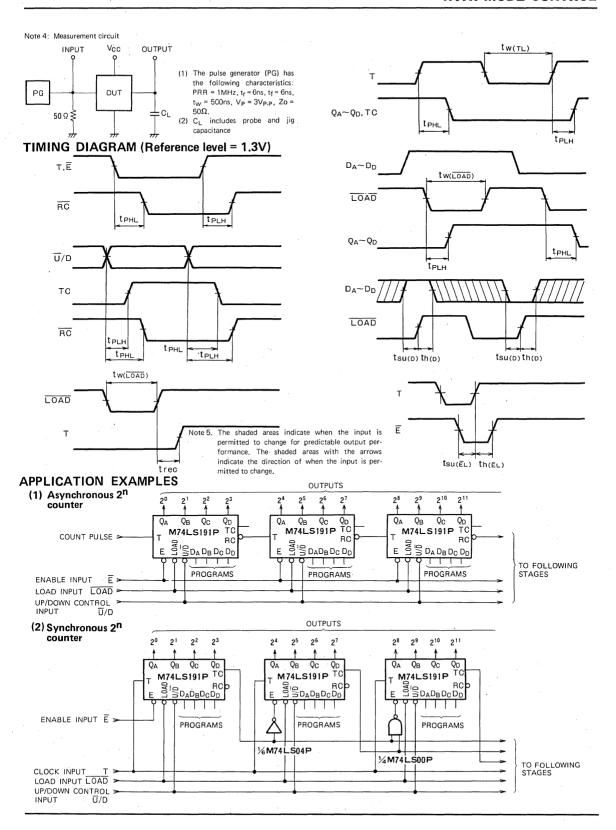
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
34111001	raiameter	. Test conditions	Min	Тур	Max	Unit
tw(TL)	Clock input T low pulse width		25	9		ns
tw(LOAD)	Load LOAD pulse width		35	10		ns
tr	Clock pulse rise time			2000	100	ns
t _{SU(D)}	Setup time DA~DD to LOAD		20	9		ns
t _{SU(ĒL)}	Setup time E low to T		40	24		ns
th(D)	Hold time DA~DD to LOAD	·	5	0		ns
th(EL)	Hold time E low to T		5	2		ns
trec(LOAD)	Recovery time LOAD to T		20	16		ns

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C. Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CC} is measured with all the inputs at OV.

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL



M74LS192P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS192P is a semiconductor integrated circuit containing a synchronous decade up/down counter function with direct reset and preset inputs.

FEATURES

- Special up count, down count clock inputs
- Asynchronous preset input provided
- Direct reset input provided
- Easy cascade connection possible
- High-speed counting (fmax = 38MHz typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

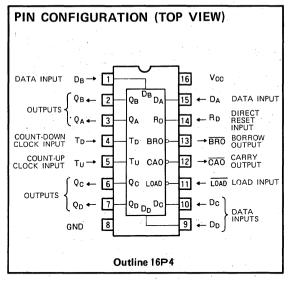
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the number of count pulses appears as a BCD code in outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses by setting load input \overline{LOAD} and T_D high, applying the count pulses to T_U while for count-down, \overline{LOAD} and T_U are set high and the count pulses are applied to T_D . Counting is performed when T_U or T_D changes from low to high.

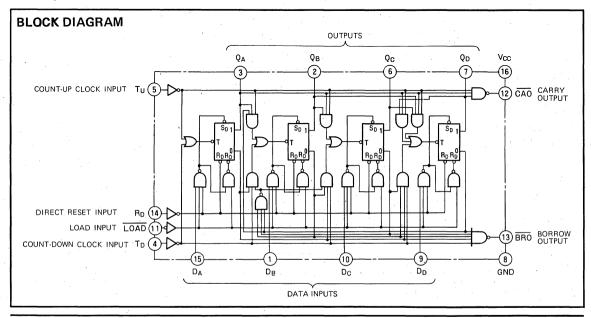
Presetting is performed independently of the count pulse. When data are applied to data inputs D_A , D_B , D_C and D_D and \overline{LOAD} is set low, the D_A , D_B , D_C and D_D signals appear in the O_A , O_B , O_C and O_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter. Counting proceeds as per the status



transition diagram with presetting to a numerical value of 10 or more.

Reset can be performed by setting the direct reset input R_D high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears in the carry output \overline{CAO} during count-up when 9 appears in Q_A , Q_B , Q_C and Q_D and when T_U is low while low appears in output \overline{BRO} when 0 appears in the outputs \overline{CAO} and \overline{BRO} should be connected to the next stage T_U and T_D for counter cascade connection. (Refer to the application examples.)



SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

FUNCTION TABLE (Note 1)

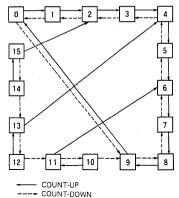
R _D	LOAD	Τυ	TD	QΑ	QB	Q _C	Q _D	CAO	BRO
Н	Х	Х	Х	L	L	L	L	Н	н*
L	L	X	×	DA	DB	Dc	D _D	н*	Н*
L	Н	Н	Н		Inhibit				н*
Ľ	Н	1	Н		Count-up			н*	Н*
L	Н	Н	1	Count-down			н*	Н*	

Note 1. ↑: Transition from low to high

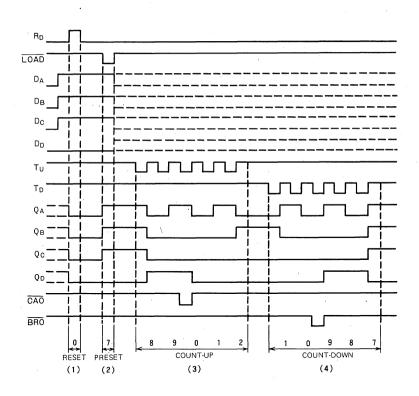
Normally high but low appears in accordance with the following logical expressions:

X : Irrelevant

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram

(1) Reset

(2) Preset to 7

(3) Count-up 8, 9, 0, 1, 2 (4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Ųι	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65 ~ + 150	°C -

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramete		Limits				
Syllibol	raiamete		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА	
loL		V ₀ L≦0.4V	0		4	mA	
	Low-level output current	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C	D	T	- diel	Limits			Unit
Symbol	Parameter	l lest co	Test conditions		Тур *	Max	J Silit
ViH	High-level input voltage			. 2			V
VIL	Low-level input voltage	7	1			0.8	V
V _{IC}	Input clamp voltage	V _{CC} = 4.75V, I _{IC} = -	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_1 = 0.8V$ $V_1 = 2V$, $I_{OH} = -400\mu A$		3.4		٧
.,	Low-level output voltage	V _{CC} = 4.75 V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.	V _{CC} =5.25V, V _I =2.7V			20	μА
Iн	righ-lever hipot corrent	V _{CC} = 5.25V, V _I = 10	V _{CC} = 5.25V, V _I = 10V			0.1	mA
l _{IL}	Low-level input current	V _{CC} = 5.25V, V _I = 0.	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V _{CC} =5.25V, V _O =0V			- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)		19	34	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

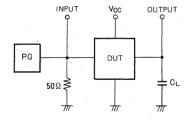
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CC} is measured with R_D and $\overline{\text{LOAD}}$ at 0V and T_U, T_D, D_A~D_D at 4.5V

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зуппьот	r arameter	lest conditions	Min	Тур	Max] 01111
f _{max}	Maximum clock frequency		25	38		MHz
t _{PLH}	Low-to-high-level , high-to-low-level output propagation	*		7	26	ns
tenl	time, from input Tu to output GAO			14	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input Tp to output BRO			7	24	ns
tpHL		O. — 15 = 5 (Note 4)		19	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input Tu. Tp to outputs	C _L =15pF (Note 4)		20	38	ns
t _{PHL}	QA, QB, QC, QD			17	47	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		24	40	ns
t _{PHL}	time, from input LOAD to outputs QA, QB, QC, QD			20	40	ns
t _{PHL}	High-to-low-level output propagation time, from input RD to outputs QA, QB, QC, QD			12	35	ns

Note 4. Measurement circuit



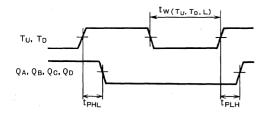
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_W = 500ns$, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance

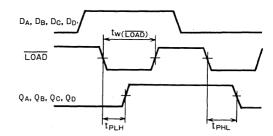
SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

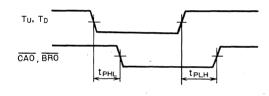
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

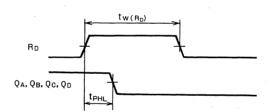
		T		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max]
tw(TuL)	Clock input Tu low pulse width		· 20	14		ns
tw(TDL)	Clock input T _D low pulse width		20	18		ns
tw(LOAD)	Load LOAD pulse width		20	11		ns
tw(RD)	Direct reset R _D pulse width		20	4		ns
t _{SU (D)}	Setup time DA~DD to LOAD		20	4		ns
t _{h(D)}	Hold time DA~DD to LOAD		5	– 3		ns

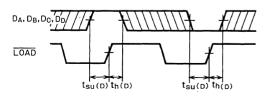
TIMING DIAGRAM (Reference level = 1.3V)







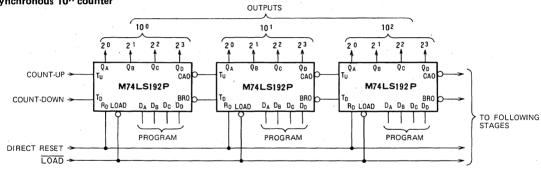




Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 10ⁿ counter



M74LS193P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS193P is a semiconductor integrated circuit containing a synchronous hexadecimal (4-bit binary) up/down counter with direct reset and preset.

FFATURES

- Special clock for up count, down count
- Asynchronous preset input provided
- Direct reset input provided
- Cascade connection easily made
- High-speed counting (f_{max}=38MHz typical)
- Wide operating temperature range (T_a=-20~+75°C)

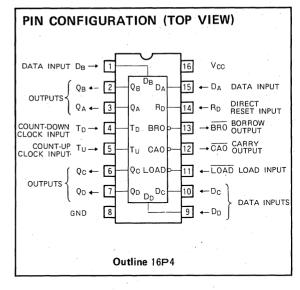
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the count pulse number appears as a 4-bit pure binary code in outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses by setting load input \overline{LOAD} and T_D to high, applying the count pulses to T_U while for count-down, \overline{LOAD} and T_U are set high and the count pulses are applied to T_D . Counting is performed when T_U or T_D changes from low to high.

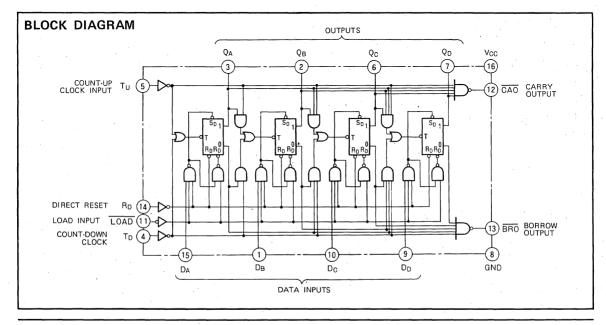
Presetting is performed regardlessly of the count pulse. When data are applied to data inputs D_A , D_B , D_C and D_D and \overline{LOAD} is set low, the D_A , D_B , D_C and D_D signals



appear in the Q_A , Q_B , Q_C , and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter.

Reset can be performed by setting the direct reset input RD high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears is the carry output \overline{CAO} during count-up when 15 appears in Q_A , Q_B , Q_C and Q_D and when T_U is low, while low appears in output \overline{BRO} when 0 appears in the outputs and when T_D is low. \overline{CAO} and \overline{BRO} should be connected to T_U and T_D of the next stage for cascade connection. (Refer to the application example.)



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

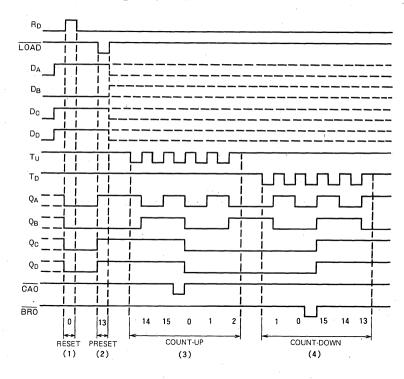
FUNCTION TABLE (Note 1)

R_{D}	LOAD	Tυ	TD	Q_{A}	QB	Qc	QD	CAO	BRO
Н	- X	Х	Х	L	L	L	L	Н	Н*
L	L	X	Χı	DA	DB	Dc	D _D	н*	н*
L	Н	Н	Н		Inh	н*	H*		
L	Н	1	Н		Count-up				Н*
L	Н	Н	1	Count-down			н*	Н*	

Note 1 1: Transition from low to high

X : Irrelevant

OPERATION TIMING DIAGRAM



Details of timing diagram

(1) Reset

(2) Preset to 13

(3) Count-up 14, 15, 0, 1, 2

(4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Limits				
Symbol	Farameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
ЮН	High-level output current	V _{0H} ≥2.7V	0		-400	μА	
loL	Low-level output current	V _{OL} ≦0.4V	0		4	mΑ	
	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0 1 1					Limits		
Symbol	Parameter	lest cond	Test conditions		Typ *	Max	Unit
VIH	High-level input voltage						. V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage	1	$V_{CC} = 4.75V$, $V_1 = 0.8V$ $V_1 = 2V$, $I_{OH} = -400\mu A$		3.4		٧
VoL	Low-level output voltage	V _{CC} = 4.75 V	I _{OL} = 4mA		0.25	0.4	·V
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧
1	High-level input current	V _{CC} =5.25V. V _I =2.7	V .			20	μΑ
ІН	riigh-lever input current	V _{CC} =5.25V, V _I =10\	<i>i</i>			0.1	mA
l _{IL}	Low-level input current	V _{CC} = 5.25V, V _I = 0.4	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	V _{CC} =5.25V, V _O =0V			- 100	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 3)		Ι,	19	34	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

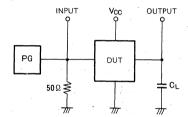
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with R_D and LOAD at 0V and T_U, T_D, D_A~D_D at 4.5V

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit	
- Cymbol		l rest conditions	Min	Тур	Max	Unit	
f _{max}	Maximum clock frequency		25	38		MHz	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	26	ns	
tpHL	time, from input T _U to output CAO			14	24	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	24	ns	
t _{PHL}	time, from input TD to output BRO	0 15-5 0		19	24	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		20	38	ns	
t _{PHL}	time, from inputs T_U , T_D to outputs Q_A , Q_B , Q_C , Q_D			17	47	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			24	40	ns	
t _{PHL}	time, from input LOAD to outputs QA, QB, QC, QD			20	40	ns	
t _{PHL}	High-to-low-level output propagation time, from input R_D to outputs $Q_A,\ Q_B,\ Q_C,\ Q_D$			12	35	ns	

Note 4: Measurement circuit



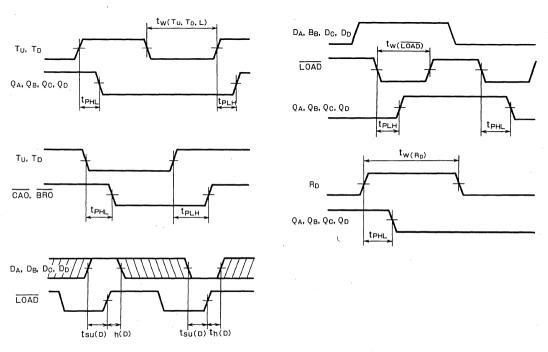
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Omt
tw(TuL)	Clock input Tu low pulse width		20	14		ns
tw(TDL)	Clock input T _D low pulse width		20	18		ns
tw(LOAD)	Load LOAD pulse width		20	11		ns
tw(RD)	Direct reset R _D pulse width].	20	4		ns
t _{SU} (D).	Setup time DA~DD to LOAD		20	4		ns
t _h (D)	Hold time DA~DD to LOAD	1	5	- 3		ns

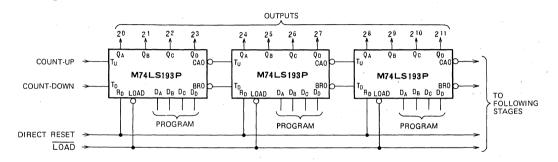
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 2ⁿ counter



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS194AP is a semiconductor integrated circuit with a 4-bit bidirectional serial/parallel input-serial/parallel output shift register functions.

FEATURES

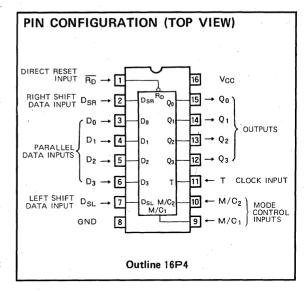
- Synchronous serial/parallel input-serial/parallel/output
- Right shift and left shift functions
- Mode control input provided
- Direct reset input provided
- Hold mode function
- Wide operating temperature range (T_a= -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

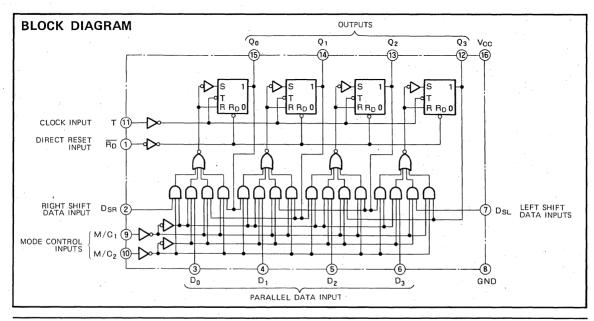
FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the modes control inputs M/C₁ and M/C₂. When M/C₁ is kept in high and M/C2 in low, the serial data are applied to right shift data input DSR and the clock pulse is applied to clock input T, the serial data are shifted sequentially to outputs $Q_0 \sim Q_3$ in synchronization with the clock pulse. When M/C₁ is kept in low and M/C₂ in high the serial data are applied to left shift data input D_{SL} and clock pulse is applied to clock input T, the serial data are shifted sequentially in synchronization with the clock pulse. The $D_0 \sim D_3$ signal appears in $Q_0 \sim Q_3$ by keeping M/C₁ and M/C₂ in high, applying the parallel data to parallel data inputs D₀~D₃ and applying a 1-bit clock pulse to clock input T. When both M/C₁ and M/C₂ are kept in low, the status of the flip-flops does not change even if the clock



pulse is applied to the clock input T.

When T changes from low to high, the right shift, left shift or parallel data are read in. $O_0 \sim O_3$ are set low by setting direct reset input $\overline{R_D}$ low irrespective of the status of the other input signals.



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operational mode	RD	M/C ₁	M/C ₂	Т	D _{SR}	D _{SL}	$D_0 \sim D_3$	Q ₀	Q ₁	Q ₂	Q ₃
Direct reset	L	X	Х	Х	Х	Х	Х	L	L	L	٦
5	Н	Н	L	1	L	Х	Х	L	Q ₀ 0	Q ₁ 0	Q ₂ 0
Right shift	Н	Н	L	1	Н	Х	×	. н	Q ₀ 0	Q1 ⁰	Q ₂ 0
1.6.1%	Н	L'	Н	1	×	L	×	Q 1 ⁰	Q ₂ 0	Q ₃ 0	L
Left shift	Н	L	Н	1	X	Н	Х	Q1 ⁰	Q ₂ 0	Q ₃ 0	Н
Parallel read	Н	Н	н	1	Х	×	D ₀ ~D ₃	D ₀	D ₁	D ₂	· D ₃
Clock inhibit	Н	L	L.	Х	Х	Х	Х	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₃ 0

Note 1. ↑: Transition from low to high (positive edge trigger)

Q0: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	C
Tstg	Storage temperature range		−65∼ + 150	ొ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	S		Limits				
Symbol	ymbol Parameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μА	
	I OL Low-level output current	V _O ∟≦0.4V	0		4.	mA	
TOL		V _{OL} ≦0.5V	0		. 8	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits		
Symbol	rarameter	lest conditi	ions	Min	Тур 🛊	Max	Unit
ViH	High-level input voltage			. 2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	· V
Vон	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		3.4		٧
V _{OL}	Low-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	$I_{OL} = 4mA$ $I_{OL} = 8mA$		0.25	0.4	V
lin	High-level input current	V _{CC} =5.25V, V _I = 2.7				20	μΑ
			$V_{CC} = 5.25V, V_I = 10V$			0.1	mA
lıL.	Low-level input current	V _{CC} =5.25V, V _I =0.4	$V_{CC}=5.25V, V_{I}=0.4V$			-0.4	mA
los	Short-circuit output current (Note 2)	$V_{CC}=5.25V, V_{O}=0$	V _{CC} =5.25V, V _O = 0 V			— 100	mΑ
lcc	Supply current	V _{CC} =5.25V (Note 3)			15	23	mΑ

* : All typical values are at $V_{CC} = 5V$, Ta = 25° C.

Note 2: All measurements must be done quickly and not more than one output should be shorted at a time.

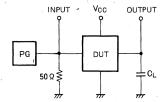
Note 3: I_{CC} is measured after $D_0 \sim D_3$ have been set to OV, D_{SR} , D_{SL} , M/C_1 , M/C_2 and $\overline{R_D}$ to 4.5V and T to 4.5V from OV.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

		Tara and distance		Limits			
Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit	
fmax	Maximum clock frequency		25	45		MHz	
tpLH	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs $Q_0 \sim Q_3$			10	22	ns	
t _{PHL}		C _L =15pF (Note 4)		12	26	ns	
tphL	High-to-low-level output propagation time, from input \overline{R}_D to outputs $Q_0 \sim Q_3$			8	30	ns	

Note 4: Measurement circuit

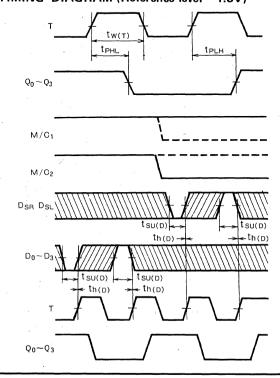


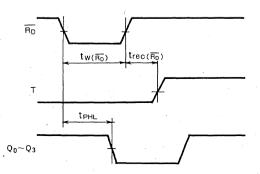
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

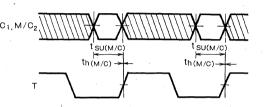
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Complete	D	Take and distance			Unit	
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input Thigh pulse width		20	5		ns
tw(RD)	Direct reset input RD pulse width		20	6		ns
tsu(D)	Setup time D to T		20	7		ns
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		30	12		ns
th(D)	Hold time D to T		0	- 3		ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T		0	- 6		ns
trec(RD)	Recovery time to direct reset		25	3		ns

TIMING DIAGRAM (Reference level = 1.3V)







Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance. The broken liners for M/C_1 and M/C_2 indicate three timings for left shifting. Setup time D_{SR} is for Q_0 only; setup time D_{SL} is for Q_3 only

M74LS195AP

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS195AP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function with a direct reset input.

FEATURES

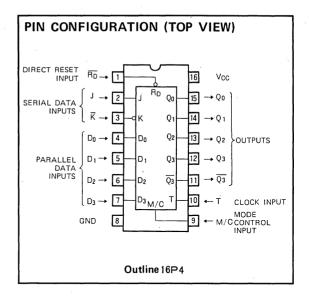
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Serial inputs J and K provided
- Direct reset input provided
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

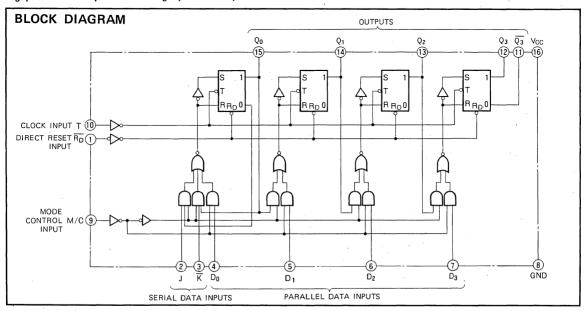
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in high, the serial data are applied to serial data inputs J and \overline{K} and the clock pulse is applied to clock input T, the serial data are shifted sequentially into outputs $O_0 \sim \overline{O_3}$ in synchronization with the clock pulse. The first stage flip-flop with J and \overline{K} functions as a J-K flip-flop. When serial data are applied from line 1, J and \overline{K} are mutually connected and used as serial input pins. When M/C is kept in low, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and a 1-bit clock pulse is applied to T, the $D_0 \sim D_3$ signals appears in $O_0 \sim \overline{O_3}$. When T changes from low to high, the shift or parallel reading operation is performed.



The last stage flip-flop output has mutually complementary outputs Q_3 and $\overline{Q_3}$, $Q_0{\sim}Q_3$ are reset low and $\overline{Q_3}$ high by setting direct reset input $\overline{R_D}$ low irrespective of all the other input signals.



4.RIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operational mode	Т	RD	M/C	J	K	D ₀ ~D ₃	Q ₀	Q ₁	Q ₂	Q 3	Q ₃
Direct reset	Х	L	X	X	×	Χ .	L	L	L	L	Н
	· 1	Н	Н	Н	Н	X	Н	Q ₀ 0	Q ₁ 0	Q ₂ 0	$\overline{Q_2^0}$
	1	Н	Н	L	L	X	L	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₂ 0
Right shift	1 .	Н	н	Н	L	X	$\overline{Q_0}$	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q ₂ 0
	1	н	Н	L	Н	X	Q ₀ 0	Q ₀ ⁰	Q ₁ 0	Q ₂ 0	$\overline{Q_2^0}$
Parallel read	1	Н	L	X	X	D ₀ ~D ₃	D ₀	D ₁	D ₂	D ₃	D ₃

Note 1. ↑: Transition from low to high (positive edge triggering)

Q0: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~'+7	V
Vı	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level output	-0.5~Vcc	٧
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits				
Symbol	raiametei	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА	
1	Low-level output current	V ₀ L≦0.4V	0		4	mΑ	
lor	Low-level output current	.V ₀ L≦0.5V	. 0	٠.	8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0		Parameter Test conditions			Limits		l lada
Symbol	Parameter	l est cond	lest conditions		Тур*	Max	Unit-
V _{IH} .	High-level input voltage						V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.	.75V, V _I =0.8V	2.7	2.4		V
V _{OH}	High-level output voltage	$V_1 = 2V$, $I_{OH} = -400 \mu A$		2.7	3.4		. V
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	High level in the surround	V _{CC} =5.25V, V _I =2.	7 V			20	μА
Iн	High-level input current	V _{CC} =5,25V, V _I =10	V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V _{CC} =5.25V, V _O =0V			- 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			14	21	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

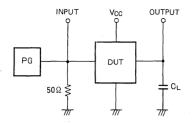
Note 3: I_{CC} is measured with M/C at 0V, J, \overline{K} and $D_0 \sim D_3$ at 4.5V, with $\overline{R_D}$ kept at 4.5V after changing from 0V and after changing T from 0V to 4.5V.

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Combal	Parameter	Test conditions		Limits	,	Unit
Symbol	Parameter	l rest conditions	Min	Тур	Max	Onit
f _{max}	Maximum clock frequency		30	60		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	22	ns
t _{PHL}	time, from input T to outputs $Q_0 \sim Q_3$, $\overline{Q_3}$			12	26	ns .
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to output $Q_0 \sim Q_3$	C _L =15pF (Note 4)		14	30	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q_3}$			12	30	ns

Note 4: Measurement circuit

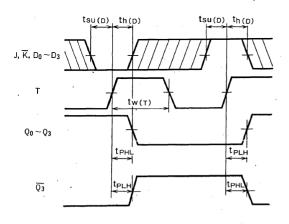


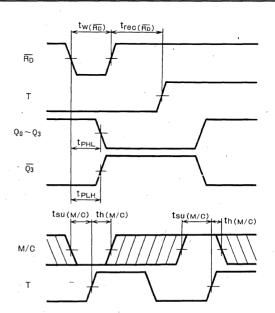
- (1) The pulse generator has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Combal	B	Task conditions		11-14		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{W(T)}	Clock input T high pulse width		16	10		ns
tw(RD)	Direct reset RD pulse width		12	6		ns
t _{SU} (D)	Setup time input data to T		15	3		ns
t _{SU(M/C)}	Setup time M/C to T		25	10		ns
t _h (D)	Hold time input data to T		3	- 1		ns
th (M/C)	M/C hold time to T		0	-7		ns
trec(RD)	Direct reset recovery time to T	• .	25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

DESCRIPTION

The M74LS196P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset input and preset input.

FEATURES

- Direct reset input and asynchronous preset input provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (fmax = 80MHz typical)
- Wide operating temperature range (T_a= -20~+75°C)

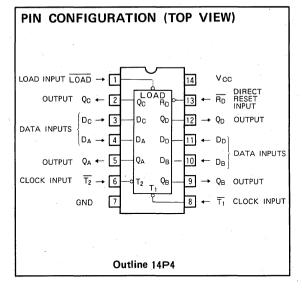
APPLICATION

General purpose, for use in industrial and consumer equipment.

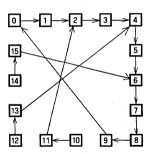
FUNCTIONAL DESCRIPTION

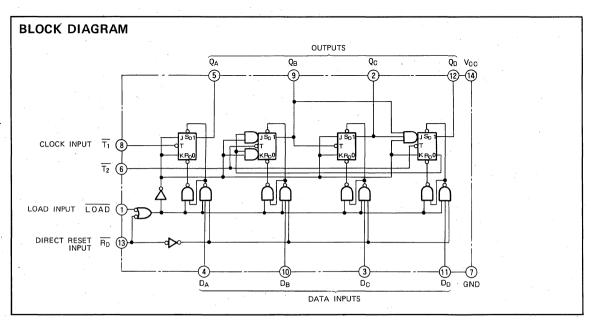
This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a BCD code appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} input low, and the D_A , D_B , D_C and D_D signals appear in Q_A , Q_B , Q_C , Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs. When preset to a numerical value of 10 or above, the count proceeds in accordance with the status transition figure.



STATE DIAGRAM





For resetting, it is possible to set $Q_A = Q_B = Q_C = Q_D =$ low by setting direct reset input R_D low irrespective of the status of the other inputs.

FUNCTION TABLE (Note 1)

T	$\overline{R_D}$	LOAD	QA	Qв	Qc	QD
×	L	Х	L	L	L	١
X	Н	L	DA	Dв	Dc	D _D
1	Н	Н		Co	unt	

Note 1 | : Transition from high to low (negative edge trigger)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS

 $(T_a = -20 \sim +75 \, ^{\circ}\mathrm{C}$, unless otherwise noted)

Count number	QA	Qв	Qc	QD
0	L	L	L	L
1	Н	L	L ·	L
2	L	Н	L	. L
3	н	Н	L	L
4	L	L	Н	L
5	н	L	н	L
6	L	н	Н	L
7	Н	Н	Ĥ	L
8	L	L	L	Н
9	н	L	L	Н

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

Symbol	Parameter	Conditions .	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
V _{CC} Supple V _I Input V _O Outpu Topr Opera	Inputs $\overline{T_1}$, $\overline{T_2}$		-0.5~+5.5		
VI	Input voltage	Inputs LOAD, RD, DA~DD	-0.5~+15	7 V	
V _O	Output voltage	High-level state	-0.5~ V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75\%$, unless otherwise noted)

Complete	5			Limits		Unit
Symbol	Param	eter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	· V
I _{OH}	High-level output current	V _{OH} ≧2.7V	0		- 400	μΑ
	Low-level output current	V _{OL} ≦ 0.4 V	0		- 400 4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

		Province	T			Limits		Unit
Symbol		Parameter	Test condt	ions	Min	Typ *	Max	Onit
ViH	High-level input vo	Itage			2			V
VIL	Low-level input vol	tage					0.8	٧
Vic	Input clamp voltag	e	V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	V
VoH	High-level output v	voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		V
.,			V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧.
VOL	Low-level output ve	ortage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA	Min Typ * 2 2.7 3.4	0.5.	V	
		LOAD, DA, DB, DC, DD					20	
		T ₁ , R _D	$V_{CC}=5.25V, V_{I}=2.7V$	/			40	μΑ
	High-level	T ₂					80	
ЦН	input current	T ₁		,			0.2	
	High-level	T ₂	V _{CC} =5.25V, V _I =5.5V			1	0.4	
		LOAD, DA, DB, DC, DD	V _{CC} =5.25V, V _I =10V				0.1	mA
		RD	V _{CC} =5.25V, V _I = 10V				0.2	
		LOAD, DA, DB, DC, DD					-0.4	
	Low-level	R _D	Vcc=5.25V. Vi=0.4V	,			-0.8	mA
IIL	input current	T ₁	VCC=5.25V, VI=U.4V	,			-2.4	IIIA
		T ₂					-2.8	
los	Short-circuit outpu	ut current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
lcc	Supply current		V _{CC} =5.25V (Note 3)			16	27	mA

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 3: I_{CC} is measured with all inputs at 0V.

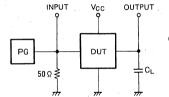


Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

		Test conditions		Limits		Unit
Symbol	Parameter	l est conditions	Min	Тур	Max	Onit
f _{max}	Maximum clock frequency, from input $\overline{\Gamma_1}$ to output Q_A		30	80		MHz
f _{max}	Maximum clock frequency, from input \overline{T}_2 to output Q_B			25		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output	•		9	15	ns
t _{PHL}	pagation time from input \overline{T}_1 to output Q_A w-to-high-level, high-to-low-level output pagation time, from input \overline{T}_2 to output Q_B w-to-high-level, high-to-low-level output	e e e e e e e e e e e e e e e e e e e		8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			10	24	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_B			10	33	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			20	57	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_C	0 45.5 (New 4)		17	62	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L = 15pF (Note 4)	13	10	18	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D	,		9	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			9	30	ns
t _{PHL}	propagation time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD			. 11	44	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			1,4	41	ns
t _{PHL}	propagation time, from input input LOAD to outputs QA, QB, QC, QD			10	45	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to outputs Q_A , Q_B , Q_C , Q_D			14	51	ns

Note 4: Measurement circuit

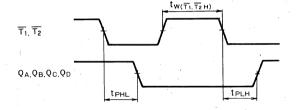


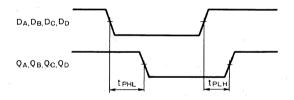
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

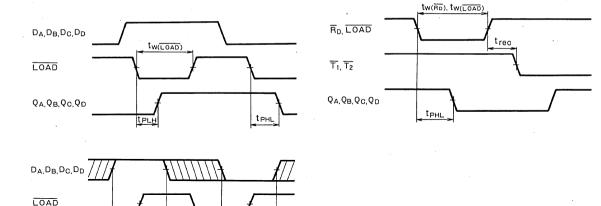
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

Symbol $t_{W(\overline{1}_1H)}$ $t_{W(\overline{1}_2H)}$			Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width		20	5		ns
tw(T₂H)	Clock input T ₂ high pulse width		30	17		ns
tw (LOAD)	Load LOAD input pulse width	1	20	8		ns
tw(RD).	Direct reset RD pulse width	1	15	4		ns
tsu(DL)	Setup time DA~DD low to LOAD		15	3		ns
t _{su(DH)}	Setup time DA~DD high to LOAD		10	0		ns
th(DL)	Hold time DA~DDlow to LOAD	1	6	0		ns
th(DH)	Hold time DA~DDhigh to LOAD	1	3	-1		ns
trec(LOAD)	. Recovery time LOAD to T		30	7		ns
trec(RD)	Recovery time RD to T		30	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





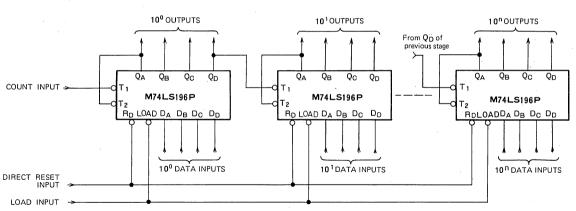


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

tsu(DL) th(D)

APPLICATION EXAMPLES

(1) Divide-by-10ⁿ presettable counter

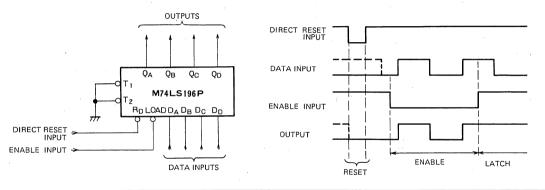


The above counter can be configured by connecting n + 1 M74LS196P devices. It operates at a high speed (60MHz typical) but since the system is synchronous, the time during which the output

changes with respect to the input is delayed in accordance with the following formula.

The delay time (typical) of each output at the Mth stage is:

(2) Use as a latch



M74LS197P

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

DESCRIPTION

The M74LS197P is a semiconductor integrated circuit containing an asynchronous hexadecimal (4-bit binary) counter function with direct reset and preset inputs.

FEATURES

- Direct reset input and asychronous preset input provided
- Usable independently as binary and octal counter
- High-speed counting (fmax = 80MHz typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ} C)$

APPLICATION

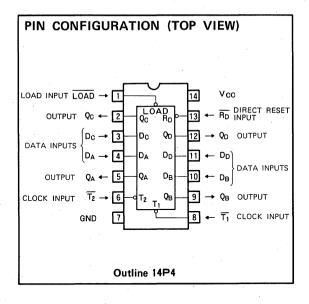
General purpose, for use in industrial and consumer equipment.

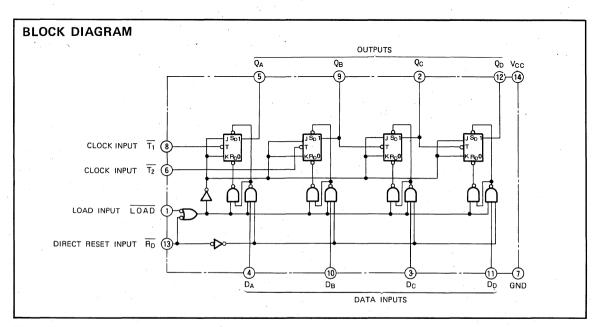
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a 4-bit pure binary code appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} input low, and the D_A , D_B , D_C and D_D signals appear in Q_A , Q_B , Q_C , Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs.

For resetting, it is possible to set $Q_A = Q_B = Q_C = Q_D =$ low by setting direct reset input \overline{R}_D low irrespective of the status of the other inputs.





PRESETTABLE 4-BIT BINARY COUNTER/LATCH

FUNCTION TABLE (Note 1)

Ť	$\overline{R_D}$	LOAD	QA	QB	Qc	Q _D
Х	L	Х	L	L	L	L
X.	Н	L	DA	D _B	Dc	D_D
\downarrow	Н	Н		Cou	ınt	

Note 1 ↓ : Transition from high to low (negative trigger)

X : Irrelevant

Count number	Q_{A}	Qв	Qc	Q _D
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	Н	L
7	Н	Н	н	L
8	L	L	L	Н
9	Н	L	L	н
10	L	Н	L	Н
11	Н	н	L	Н
12	L	L	Н	Н
.13	Н	L	Н	н
14	L	Н	н	Н
15	Н	н	н	н
15			H	

⁽¹⁾ Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
V _I Inpu	Inputs $\overline{T_1}$, $\overline{T_2}$		-0.5~+5.5		
VI	Input voltage	Inputs LOAD, RD, DA~DD	-0.5~+15	¬	
Vo	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	ဗ	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	rarameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	- V	
I _{OH}	High-level output current	V _{OH} ≥2.7V	0		-400	μА	
i la	Law level output aureant	V _{OL} ≤0.4V	0		4	mΑ	
I _{OL} .	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ	

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	T .	D			1	Limits	-	
Symbol		Parameter	l'est conditi	Test conditions		Typ *	Max	Unit
VIH	High-level input vol	tage			2			V
VIL	Low-level input volt	age					0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	٧
VoH	High-level output vo	oltage	V_{CC} =4.75V, V_{I} =0.8V V_{I} =2V, I_{OH} =-400 μ A		2.7	3.4		٧
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
	LOAD, DA, DB, DC, DD		V . 5 05V V 0 7V	V			20	
	High-level input current	$\overline{R_D}$, $\overline{T_1}$, $\overline{T_2}$	$V_{CC}=5.25V, V_1=2.7V$	•			40	μΑ
lін		$\overline{T_1}$, $\overline{T_2}$	V _{CC} =5.25V, V _I =5.5V	1		0.2		
		LOAD, DA, DB, DC, DD	Vcc=5.25V, Vi= 10V				0.1	⋅mA
	RD		7 VCC-5.25V, VI= 10V	,			0.2	
		LOAD, DA, DB, DC, DD					-0.4	
1	Low-level	RD	V _{CC} =5.25V, V _I =0.4V		-0.8			
lıL.	input current	T ₁]			-2.4	mΑ	
		T ₂	1				-1.3	
los	Short-circuit output	current (note 2)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
lcc	Supply current		V _{CC} =5.25V (Note 3)			16	27	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

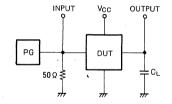
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at OV.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Зуппоп	, arameter	rest conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency $(\overline{T_1})$		30	80		MHz
fmax	Maximum clock frequency (T2)			35		MHz
tpLH	Low-to-high-level, high-to-low-level output			6	15 .	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_A		-	7	21 -	ns
t PLH	Low-to-high-level, high-to-low-level output			8	19	ns
t PHL	propagation time, from input $\overline{T_2}$ to output Q_B			8	35	ns
t PLH	Low-to-high-level, high-to-low-level output	C _L = 15pF (Note 4)		15	51	ns
t PHL	propagation time, from input $\overline{T_2}$ to output Q_C	CL— 15pF (Note 4)		15	63	ns
tpLH	Low-to-high-level, high-to-low-level output			22	78	ns
t PHL	propagation time, from input $\overline{T_2}$ to output Q_D			24	95	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			8	- 27	ns
t _{PHL}	propagation time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD			10	44	ns
tpLH	Low-to-high-level output propagation time, from			13	39	ns
t PHL	input LOAD to outputs QA, QB, QC, QD			10	45	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_A , Q_B , Q_C , Q_D			13	51	ns

Note 4: Measurement circuit



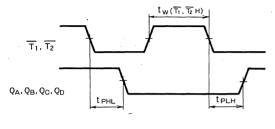
- (1) The pusle generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_t = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω .
- 2) C_L includes probe and jig capacitance

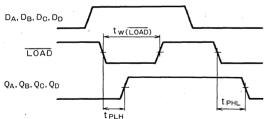
PRESETTABLE 4-BIT BINARY COUNTER/LATCH

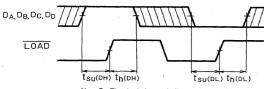
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

0	Parameter	To a live of	Limits			Unit
Symbol	rarameter	Test conditions	Min	Тур	Max	Oille
tw(TiH)	Clock input T ₁ high pulse width		20	5		ns
tw(T2H)	Clock input T ₂ high pulse width		30	14		ns
tw(LOAD)	Load LOAD input pulse width		20	8		ns
tw(RD)	Direct reset RD pulse width		15	4		ns
t _{su(DL)}	Setup time DA~DD low to LOAD	•	15	3		ns
t _{SU(DH)}	Setup time DA~DD high to LOAD		10	0		ns
th(DL)	Hold time DA~DD low to LOAD		6	0		ns
th(DH)	Hold time D _A ∼D _D high to LOAD		3	— 1		ns
trec(LOAD)	Recovery time LOAD to T		30	7		ns
trec(RD)	Recovery time RD.to T		30	7		ns

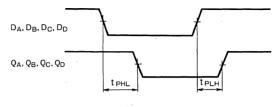
TIMING DIAGRAM (Reference level = 1.3V)

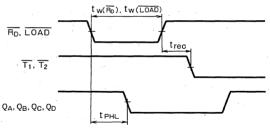






Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.





M74LS221P

DUAL MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74LS221P is a semiconductor integrated circuit containing two monostable multivibrator circuits with direct reset inputs.

FEATURES

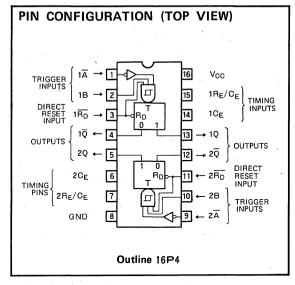
- Pulse width excellent temperature characteristics and supply voltage
- Schmidt trigger inputs (B inputs) provided
- Wide output pulse width range $(t_w = 47 \text{ns} \sim 1 \text{s})$
- Operation possible with duty cycle up to 90% $(R_T=100k\Omega)$
- Direct reset inputs provided
- A, B complementary inputs provided
- Q and Q outputs
- High input breakdown voltage (V₁≥15V)
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

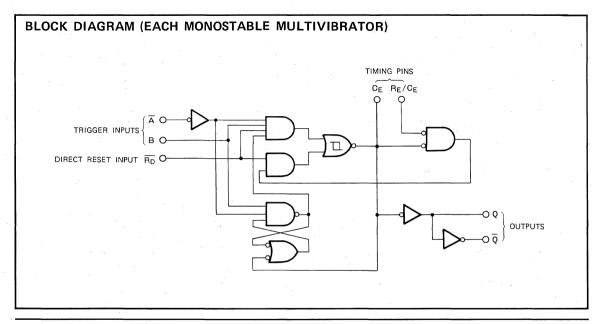
FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and electrostatic capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1, and by applying a trigger from input \overline{A} or B. The width t_w of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied. This IC is able to obtain an output pulse width with excellent supply



voltage and temperature characteristics since both its supply voltage and temperature are assured.

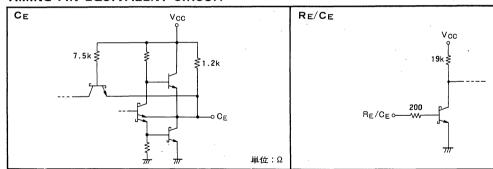
Q can be reset immediately low and \overline{Q} high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. If $\overline{R_D}$ changes from low to high when \overline{A} is low and B is high, the trigger is applied and the pulse appears in the output.



単位:Ω

DUAL MONOSTABLE MULTIVIBRATOR

TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

R _D	Ā	В	Q	Q
L	X	Х	L	Н
X	Н	. X	L	Н
Х	×	L	L	Н
Н	L	1	Л	Ъ
Н	1	Н	7.	L
1	L	Н		7.5

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and electrostatic capacitor C_T are connected to timing pins R_E/C_E and C_E . Connect the negative to the R_E/C_E side and the positive to the C_E side when using C_T with polarity.

$$\begin{array}{c} V_{CC} \\ R_T \\ + C_T \\ \end{array}$$

Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

Note 1. 1: Transition from low to high.

↓ : Transition from high to low.

☐: Positive one-shot operation.

T: Negative one-shot operation.

X : Irrelevant

2. Output pulse width tw

The output pulse width t_w is set using R_T and C_T by the following formula:

$$t_W = C_T \cdot R_T \cdot \ln 2 \text{ (ns) } X \text{ (1} \pm 0.1)$$

 $\approx 0.7 C_T \cdot R_T \text{ (ns) } X \text{ (1} \pm 0.1)$

 $R_{\rm T}$ is measured in kiloohms and $C_{\rm T}$ in picofarads. Individual fluctuations of +10% may occur in products.

Depending on the product, fluctuations in the order of 3/-10% may occur.

3. Precautions with use

In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_{T} and C_{T} wiring as short as possible and avoid signal wires which may be conducive to noise.

Connect a capacitor of $0.01{\sim}0.1\mu F$ with good high-frequency characteristics between pins V_{CC} and GND. Mount this capacitor as close as possible to the IC.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	ొ
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter			Limits				
Symbol	rara	meter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
lon.	High-level output current	V _{OH} ≥2.7V	0		-400	μΑ		
	Low-level output current	V _{OL} ≤0.4V	0		4	mΑ		
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA		
R _{T.}	External timing resistance		1.4		100	kΩ		
Ст	External timing capacitance		0		1000	μF		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

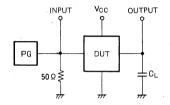
0			Tdision			Limits		Unit
Symbol	Parame	eter .	Test condition	is	Min	Тур *	Max	
ViH	High-level input voltage				2			٧
.,		Ā, B					0.8	V
VIL	Low-level input voltage RD						0.5	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	mA			- 1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.5, (0.8V	2.7	3.4		V	
Voh	High-level output voltage		$V_1 = 2V$, $I_{OH} = -400 \mu A$		2.7	3.4		<u> </u>
1/-	Law lavel autout values		V _{CC} =4.75V	I _{OL} =4mA	,	0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.5V, 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	I litely described to a consequent		$V_{CC}=5.25V, V_{I}=2.7V$				20	μΑ
Ιн	High-level input current		$V_{CC} = 5.25V, V_I = 10V$				0.1	mA
1		Ā	V _{CC} =5.25V		,		-0.4	
lıL.	Low-level input current	B, RD	V ₁ = 0.4 V				-0.8	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mΑ
	Supply current (static state)		V _{CC} =5.25V			4.7	11	mΑ
lcc	Supply current (one-shot state	e)	V _{CC} =5.25V			19	27	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25$ °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits		Unit
Symbol	ratanietei		Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level output propagation time, from input \overline{A} to output Q			٠.	27	70	ns
t _{PLH}	Low-to-high-level output propagation time, from input Bto output Q				24	55	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{A} to output $\overline{\overline{Q}}$	$C_T = 80pF$ $R_T = 2k\Omega$			30	80	ns
t _{PHL}	High-to-low-level output propagation time, from input B to output $\overline{\mathbf{Q}}$	$C_L = 15pF$	(Note 3)		26	65	ns
telh	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}				23	65	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q				18	55	ns
twQ(min)	Minimum output pulse width, from inputs \overline{A} , B to outputs Q, \overline{Q}	$C_T = 0_p F$, R $C_L = 15 pF$ (T=2kΩ Note3)	20	30	70	ns
***************************************		0 - 15-5	$C_T=80pF$, $R_T=2k\Omega$	70	120	150	ns
two	Output pulse width, from inputs \overline{A} , B to outputs Q , \overline{Q}	C _L = 15pF	$C_T = 100 pF$, $R_T = 10 k \Omega$	600	670	750	ns
		(Note 3)	$C_T = 1\mu F$, $R_T = 10k\Omega$	6	6.9	7.5	ms

Note 3: Measurement circuit



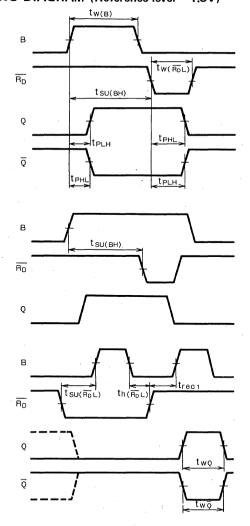
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_w =40ns, V_P =3 $V_{P,P}$, Z_O =50 Ω
- (2) C_L includes probe and jig capacitance

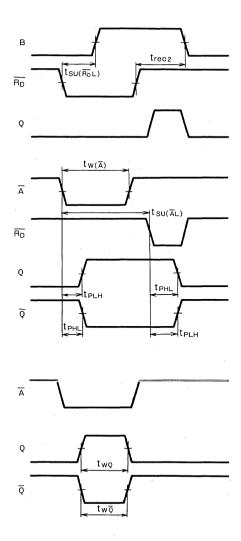
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25$ °C, unless otherwise noted)

	D			Test conditions		Limits		Unit
Symbol	Parameter			rest conditions	Min	Тур	Max	
	Maximum rise, fall voltage rate of input	mulan	Ā		1			V/μs
tr, tf	B			1			V/s	
tw(Ā)	Trigger A pulse width				40	35		ns
tw(B)	Trigger B pulse width				40	35		ns
tw(RD)	Direct reset input pulse width				40	9		ns
0.00	Output duty cycle	R _T =2k	〈 Ω				50	%
0.D.C	Output duty cycle	R _T = 10	00kΩ	(Note 3)			90	%
tsu(ĀL)	Setup time \overline{A} low to $\overline{R_D}$. 60	33		ns
tsu(BH)	Setup time B high to $\overline{R_D}$				60	25		ns
tsu(RDL)	Setup time RD low to B				50	15'		ns
trec 1	Recovery time			•	15	– 5		ns
trec 2	Recovery time (when B is superimposed of	onto R	5)		50	30		ns
th(RDL)	Hold time RD low to B				. 0	- 15		ns

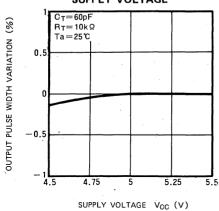
TIMING DIAGRAM (Reference level = 1.3V)



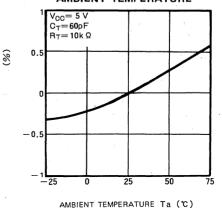




OUTPUT PULSE WIDTH VARIATION VS



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



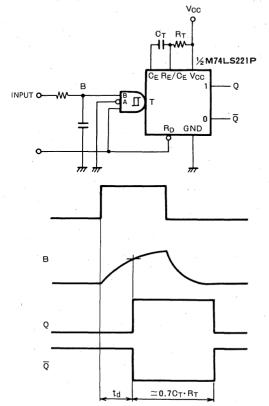
APPLICATION EXAMPLES

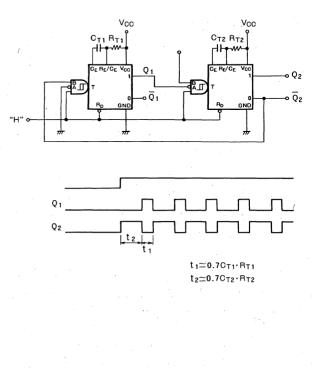
(1) Delay circuit

By connecting an integration circuit to the B input, a rectangular waveform applied to the input is changed to the waveform shown at B and delayed by time t_d . The width of the pulse output at Q and Q is determined as usual by the values of C_T , R_T connected externally to the circuit.

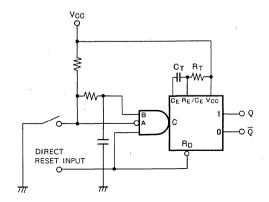
circuit (2) Pulse generator

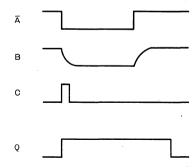
Using the fact that the output pulse width of the M74LS221P varies only slightly with changes in supply voltage and ambient temperature, a pulse generator with good supply voltage and temperature stability can be implemented. By choosing the values of externally connected components C_{T} and R_{T} , the duty cycle and frequency can be freely selected.





(3) ANTI-CHATTERING CIRCUIT





DESCRIPTION

The M74LS240P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state inverted output and common output control input for all 4 discrete circuits.

FEATURES

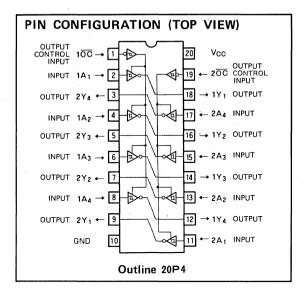
- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁≥5V)
- Output control input having same phase for 2 circuits. (1OC. 2OC)
- High fan-out, 3-state output.
 (I_{OI} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20^{\circ} + 75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and high breakdown input voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When the output control input \overline{OC} is low, high appears in the output Y if input A is low, and low appears in the Y if A is high. If, on the other hand, \overline{OC} is high, all the outputs Y_1, Y_2, Y_3 , and Y_4 are in a high-impedance state, irrespective of the status of A.



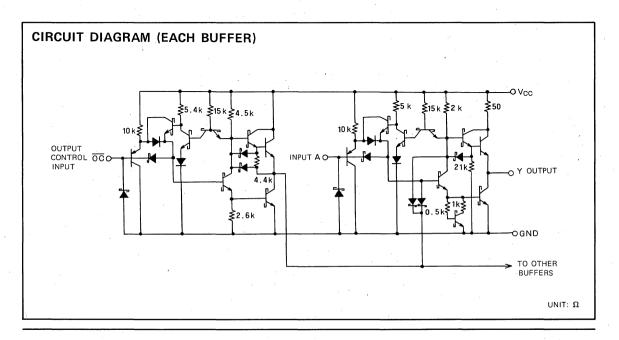
By connecting $1\overline{OC}$ with $2\overline{OC}$, it becomes possible to control the output of the 8 circuits. The output can be terminated with load resistor of 133Ω or over.

FUNCTION TABLE (Note 1)

Α	ōc	Y
L	L	Н
Н	L	L
X	Н	Z

Note 1: Z: high-impedance

X: irrelevant



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	٧ .
Vo	Output voltage	Off-state	$-0.5 \sim +5.5$	V
Topr	Operating free-air ambient temperature range	,	-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D			Limits		Unit
Symbol	Parameter		Min	Тур	Max	Onit
Vcc	CC Supply voltage	voltage	4.75	5	5.25	>
		V _{OH} ≧2.4V	0		-3	mA
Іон	High-level output current	V _{OH} ≧ 2 V	0		-15	mA
	IOL Low-level output current	V _{OL} ≤0.4V	0		12	mA
IOL		V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

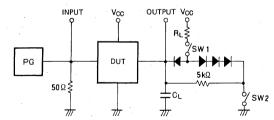
		+	+	Limits		Unit
Symbol	Parameter	Test conditions	Min	Typ*	Max	
V _{IH}	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _{T+} -V _{T-}	Hysteresis	V _{CC} =4.75V	0.2	0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
.,	High-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V$, $I_{OH} = -3$ n	nA 2.4	3.4		V
VoH	High-level output voltage	$V_1 = 2V$ $V_1 = 0.5V, I_{OH} = -15$	mA 2			V
.,	Low level output voltage	V _{CC} =4.75V I _{OL} =12m/	4	0.25	0.4	V
V _{OL} Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24m/	4	0.35	0.5	. V	
lozн	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V, V _O =0.4V			-20	μА
	High-level input current	V _{CC} =5.25V, V _I =2.7V			20	μА
liH	nigh-level input current	V _{CC} =5.25V, V _I =10V			0.1	, mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	-40		-225	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I = 0 V		17	27	mA
ICCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		26	. 44	mA
lccz	Supply current, all outputs off	V _{CC} =5.25V, V _I =4.5V		29	50	mA ·

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Description	Test conditions		Limits		Unit
	Parameter		Min	Тур	Max	Oill
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		7	14	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		15	.30	ns
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		12	18	ns

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C, Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

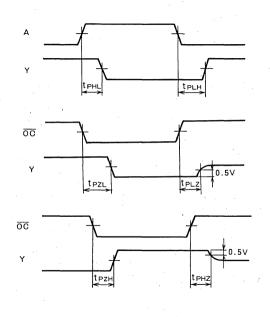
Note 3: Measurement circuit



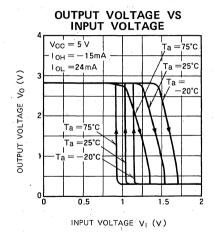
Parameter	SW 1	SW2		
t pzh	Open	Closed		
t PZL	Closed	Open		
t _{PLZ}	Closed	Closed		
t _{PHZ}	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

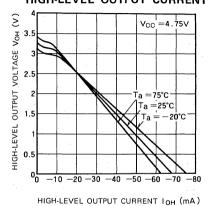
TIMING DIAGRAM (Reference level = 1.3V)



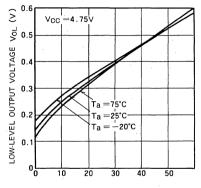
TYPICAL CHARACTERISITCS



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT CURRENT IOL (mA)

DESCRIPTION

The M74LS241P is a semiconductor integrated circuit containing 2 buffer blocks with 3-state non-inverted outputs and is provided with output control inputs which are common to 4 circuits and which are independent.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage (V₁ ≥ 15V)
- Complementary output control inputs (100, 200)
- High fan-out 3-state outputs
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range (T_a=-20~+75°C)

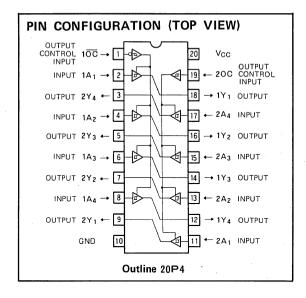
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

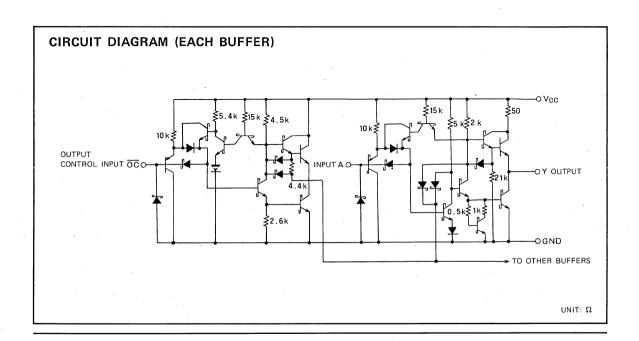
Since pnp transistors are used for the input circuits, the input load factor is small and a high breakdown input voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $1\overline{OC}$ is low, low appears in output Y if input 1A is low, and high appears in Y if 1A is high. When 2OC is high, low appears in output 2Y if input 2A is low and high



appears in 2Y if 2A is high. All the outputs are put in a high-impedance state when $1\overline{OC}$ and 2OC are high and low, respectively.

The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y and also 2A and 1Y. The outputs can be terminated with load resistors of not less than 133 ohms.



FUNCTION TABLE (Note 1)

1A	100	1Y
L	L	L
Н	L	Н
×	н	Z

2A	20C	2Y
L	Н	L,
Н	Н	·H
X	L.	Z

Note 1 Z : High-impedance

X : irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~ + 150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

	Description			Limits			
Symbol Parameter		· arameter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
	Lifet Island and American	V _{0H} ≧2.4V	0		-3	mA	
Гон	High-level output current	V _{0H} ≧ 2 V	0		—15	mA	
1	t and a state of a state of	V _{OL} ≤0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

0	Developed	Total condition		Limits		Unit
Symbol	Parameter	Test conditions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage		2	(V
V _{IL}	Low-level input voltage				0.8	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V	0.2	0.4		٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
.,	High-level output voltage	$V_{CC} = 4.75V$ $V_I = 0.8V$, $I_{OH} = -3m$	A 2.4	3.1		V
VoH	High-level output vortage	$V_1 = 2V$ $V_1 = 0.5V$, $I_{OH} = -15r$	nA 2			V
.,	I am land a standard a land	V _{CC} =4.75V I _{OL} =12mA	١	0.25	0.4	٧
V _{OL}	Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24mA	4	0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V, V _O =0.4V			_20	μА
	High Invalidance and an arrange	V _{CC} =5.25V, V _I =2.7V			20	. μА
ин	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0V	40		-225	mA
Госн	Supply current, all outputs high	$V_{CC}=5.25V, V_{I}=0V, V_{I}=4.5V$		17	27	mA
ICCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		27	46	mA
locz	Supply current, all outputs disabled	V _{CC} =5.25V, V _I =0V, V _I =4.5V		32	. 54	mA

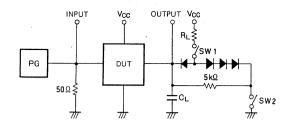
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = \overline{25^{\circ}C}$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Combat	Parameter	Test conditions	8 18			
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		8	18	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	30	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)		12	18	ns

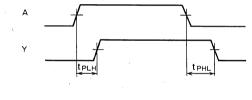
Note 3: Measurement circuit

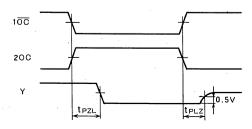


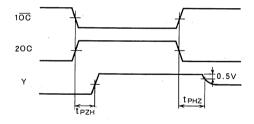
Symbol	SW-1	SW2		
t pzh	Open	Closed		
t PZL	Closed	Open		
tpLZ	Closed	Closed		
t _{PHZ}	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P \stackrel{?}{=} 3V_{P,P}, Z_0 = 50\Omega.$ (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V) .

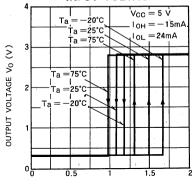






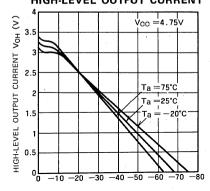
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE



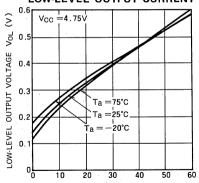
INPUT VOLTAGE VI (V)

HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



HIGH-LEVEL OUTPUT CURRENT IOH (MA)

LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT CURRENT IOL (mA)

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS242P is a semiconductor integrated circuit containing 4 bus transmitters/receivers circuit with 3-state inverted outputs.

FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High fan-out ($I_{OL} = 24mA$, $I_{OH} = -15mA$)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

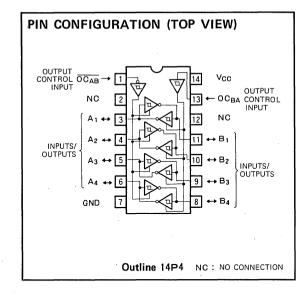
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state inverted outputs are made two-way buffers.

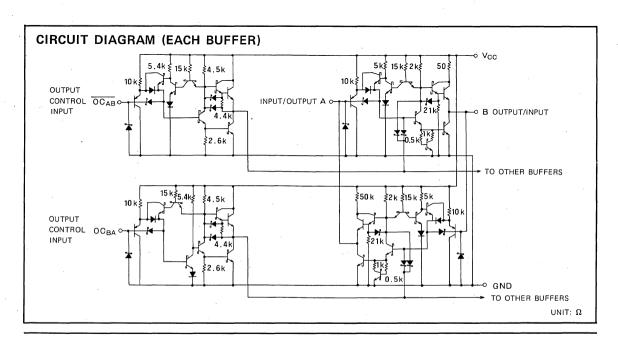
Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA} . When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is low, both A



and B are put in the high-impedance state and A and B are isolated. When $\overline{OC_{AB}}$ is low and OC_{BA} is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state must therefore be avoided. This state resulting from the $\overline{OC_{AB}}$ and OC_{BA} signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms.

Refer to M74LS240P for the typical characteristics.



QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

OCAB	OCBA	Α	В
Н	Н	ō	ı
L	Н	*	*
н	L	Z	·Z
L	L		ō

Note 1: | Input pin

O : Output pin (inverted)

Inhibited (A and B are made output pins)High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vı	Input voltage	A, B		-0.5~+5.5	V
۷Į	input voitage	OCAB, OCBA		-0.5~+15	٧.
Vo	Output voltage		Off-state	-0.5~+5.5	· V
Topr	Operating free-air ambier	nt temperature range		-20~+75	°C
Tstg	Storage temperature range	je		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			11-2-		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
1	High-level output current	V _{OH} ≧2.4V	0		-3	mA
Іон	High-level output current	V _{0H} ≧ 2 V	0		-15	mA
	Low-level output current	V _{OL} ≦0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

0 1 1	,			T			Limits		Unit
Symbol	Parameter			Test conditions -		Min	Тур *	Max	Omt
VIH	High-level input voltage					2			٧
VIL	Low-level input voltage							0.8	V
$V_{T+}-V_{T-}$	Hysteresis width		V _{CC} =4.75V			0.2	0.4		V
Vic	Input clamp voltage	,	V _{CC} =4.75V.	I _{IC} =-	18mA			-1.5	V
. ,,	Ulab laval average values)	V _{CC} =4.75V	V _I = 0	.8V, I _{OH} =-3mA	2.4	3.1		٧
Voн	High-level output voltage		V _I = 2 V	V ₁ = 0	.5V, I _{OH} = — 15mA	2	- 1		V
	Low-level output voltage		V _{CC} =4.75V		I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V, V _I =	=2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output curre	nt	V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V				40	μΑ	
lozL	Off-state low-level output curren	nt	V _{CC} =5.25V, V	/ _I =0.8V	V _I =2V, V _O =0.4V			-200	μА
		A,B	Vcc=5.25V.	V-2.7				20	μΑ
1	High-level input current	OCAB, OCBA	V _{CC} =5.25V,	V =2.7	'			20	μΑ
ин	riigii-level iliput current	A, B	V _{CC} =5.25V,	V ₁ =5.5	V			0.1	mA
		OCAB, OCBA	V _{CC} =5.25V,	V _I = 10V				0.1	IIIA
		OCAB, OCBA	V 5 05)/					-0.2	
lı_	Low-level input current	Α	$V_{CC} = 5.25V$ $V_{I} = 0.4V$	Ō	CAB = OCBA = OV			-0.2	mA
		В	VI=0.4V	. 0	CAB = OCBA=4.5V			-0.2	
los	Short-circuit output current (No	te 2)	V _{CC} =5.25V, V _O =0V		-40		-225	mA	
Гссн	Supply current, all outputs high		$V_{CC} = 5.25V, V_1 = 0V, V_1 = 4.5V$			22	38	mA	
CCL	Supply current, all outputs low		$V_{CC} = 5.25V, V_1 = 0V, V_1 = 4.5V$			29	50	mA	
Iccz	Supply current, all outputs off		V _{CC} =5.25V,	V _I =0V	, V _I =4.5V		29	50	mA

^{* :} All typical values are at V_{CC}=5V, Ta=25°C.

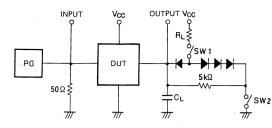
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

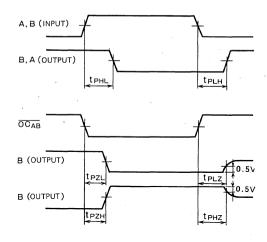
Symbol Parameter	Test conditions		Limits			
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,	C _L =45pF		7	14	ns
t _{PHL}	from inputs A, B to outputs B, A	(Note 3)		9	18	ns
t _{PZL}	Output disable time from low-level	R _L =667Ω, C _L =45pF (Note 3)		15	40	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		12	40	ns
t _{PLZ}	Output enable time to low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$ $C_L=5$ pF (Note 3)		12	18	ns

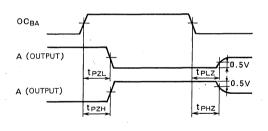
Note 3: Measurement circuit



Symbol	SW1	SW2
t pzh	Open	Closed
t pzL	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P , P_T , P_T = 50 Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) CL includes probe and jig capacitance.





QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS243P is a semiconductor integrated circuit containing 4 bus transmitters/receivers with 3-state non-inverted outputs.

FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400 mV typical)
- High fan-out ($I_{OL} = 24mA$, $I_{OH} = -15mA$)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

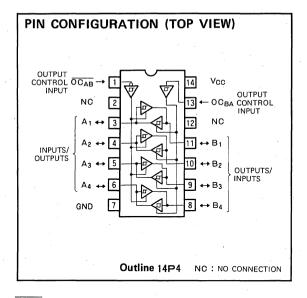
General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state non-inverted outputs are made two-way buffers.

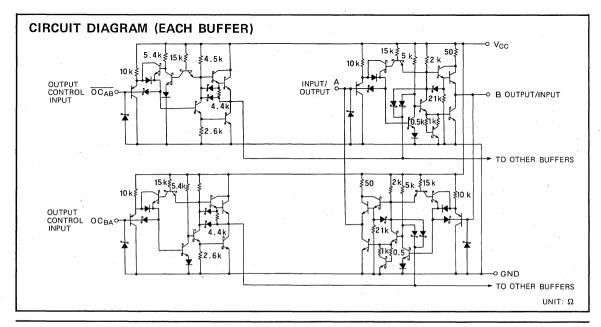
Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA} . When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is low, both A and B are put in the high-impedance state and A and B are isolated. When



 $\overline{\text{OC}_{AB}}$ is low and OC_{BA} is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state must therefore be avoided. This state resulting from the $\overline{\text{OC}_{AB}}$ and OC_{BA} signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms.

Refer to M74LS241P for the typical characteristics.



OUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

OCAB	OCBA	Α	В
H	Н	0	ı
L	н	*	*
н	L	. Z	Z
L	L	1	0

Note 1: I : Input pin

O: Output (non-inverted) pin

*: Inhibited (A and B are made output pins)

Z: High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter Conditions		Limits	Unit	
Vcc	Supply voltage			-0.5~+7	٧
Vı	Input voltage	A, B		-0.5~+5.5	V
VI	Input voltage	OCAB, OCBA		-0.5~+15	٧
Vo	Output voltage		Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambie	nt temperature range		-20~+75	°C
Tstg	Storage temperature ran	ge '		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	vmbol Parameter			Limits		Unit
Symbol	rarame	ler	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
	High-level output current	V _{OH} ≧2.4V	0		-3	mA
іон	riigii-level output corrent	V _{OH} ≧ 2 V	0		-15	mA
	Low-level output current	V _{OL} ≦0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted.)

C	Paramete	_		Test conditio			Limits		Unit		
Symbol	raramete	ır.		rest conditions		Min	Тур *	Max	Onit		
V _{IH}	High-level input voltage					2			٧		
VIL	Low-level input voltage							0.8	V		
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V			0.2	0.4		V		
Vic	Input clamp voltage		V _{CC} =4.75V,	I _{IC} = - 18	mA			-1.5	V		
	High-level output voltage		V _{CC} =4.75V	V1 = 0.8V	, I _{OH} = - 3mA	2.4	3.1		V		
Voн	riign-ievei output voitage		V ₁ =2V	V _I = 0.5V	, I _{OH} = — 15 mA	2			V ·		
.,	Low-level output voltage		V _{CC} =4.75V		I _{OL} = 12mA		0.25	. 0.4	V		
VoL	Low-level output voltage		V _I =0.8V, V _I	=2V	I _{OL} =24mA		0.35	0.5	٧		
lozh	Off-stage high-level output curr	ent	V _{CC} =5.25V,\	V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V		V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V				40	μА
lozL	Off-state low-level output curre	nt	V _{CC} =5.25V,\	/ _I =0.8V, V	I=2V, V ₀ =0.4V			-200	μА		
		A, B	Vcc=5.25V.					- 20			
	High-level input current	OCAB, OCBA	V _{CC} =5.25V,	V ₁ =2.7V				20	μ Α .		
Iн	riigii-level iriput current	A, B	V _{CC} =5.25V,	V _I =5.5V				0.1	^		
		OCAB, OCBA	V _{CC} =5.25V,	V ₁ =10V				0.1	mA		
		OCAB, OCBA	\/ E 25\/					-0.2			
li <u>L</u>	Low-level input current	Α	V _{CC} =5.25V	OCA	B=0C _{BA} =0V			-0.2	mA		
,		В	V₁=0.4V	OCA	B=0C _{BA} =4.5V			-0.2			
los	Short-circuit output current (N	lote 2)	V _{CC} =5.25V, V _O =0V		-40		- 225	mA			
Гссн	Supply current, all output high		V _{CC} =5.25V,	$V_I = 0 V$,	V _I =4.5V		22	38	mA		
ICCL	Supply current, all outputs low	,	V _{CC} =5.25V,	$V_{CC}=5.25V, V_I=0 V, V_I=4.5V$			29	50	mA		
Iccz	Supply current, all outputs off		V _{CC} =5.25V,	$V_1 = 0 V$	V ₁ = 4.5V		32	54	mA		

 $^{{\}boldsymbol *}$: All typical values are at $\,V_{CC}\!=\!5V$, $\,Ta\!=\!25^{\circ}C$.



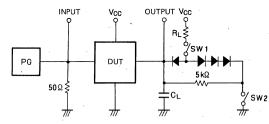
Note 2: All measurements should be done quickly and not more than one outputs should be shorted at a time.

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

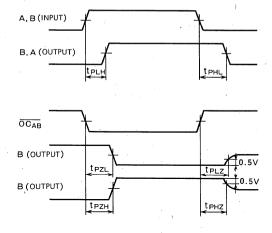
Symbol	Parameter Test conditions		Limits			Unit
Symbol	Farameter	rest conditions	Min	Тур	Max	Olife
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,	C _L =45pF		8	18	ns
t _{PHL}	ifrom inputs A, B to outputs B, A	(Note 3)		9	18	ns
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		15	40	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)		12	18	ns

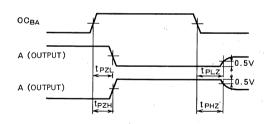
Note 3: Measurement circuit



	Symbol	SW1	SW2		
	t pzh	Open	Closed		
	t PZL	Closed	Open		
	t _{PLZ}	Closed	Closed		
j	t _{PHZ}	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- All diodes are switching diodes (t_{rr} ≤ 4ns).
- (3) CL includes probe and jig capacitance.





OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS244P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state non-inverted output and common output controlling input for all 4 discrete circuits.

FEATURES

- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁≥15V)
- Output control input having same phase for 2 circuits
- High fan-out, 3-state output
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

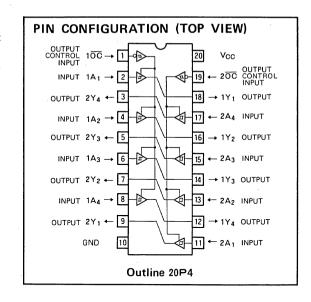
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuit has enabled the achievement of small input load factor. With hysteresis characteristics, the buffer has a 3-state noninverted output with high noise margin.

When output control input \overline{OC} is low, the output Y is low if input A is low and Y is high if A is high. When \overline{OC} is high, all of Y₁, Y₂, Y₃, and Y₄ are in the high-impedance state, irrespective of the status of A.

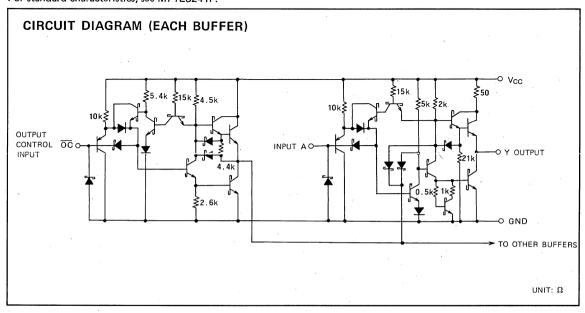
By connecting $1\overline{OC}$ with $2\overline{OC}$, it becomes possible to control the output of all 8 circuits simultaneously. Output can be terminated by a load resistor of 133Ω or over. For standard characteristics, see M74LS241P.



FUNCTION TABLE (Note 1)

Α	ōc	Y
L	L	L
Н	L	Н
X	Н	Z ·

Note 1: Z: high-impedance X: irrelevant



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		$-0.5 \sim +7$	V
· Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	Off-state	$-0.5 \sim +5.5$	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	0			Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
	High lovel cutrust current	V _{OH} ≧2.4V			- 3	mA		
Іон	High-level output current	V _{OH} ≧ 2 V			- 15	mA		
	Low-level output current	V _{OL} ≦0.4V			12	mA		
loL	Low-level output current	V _{OL} ≤0.5V			24	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Test conditions			Limits		11-14	
Symbol	Parameter	16	est condition	ıs	Min	Тур*	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage	1					0.8	V
V _{T+} -V _{T-}	Hysteresis	V _{CC} =4.75V			0.2	0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V,	I _{IC} =-18	nA		1	-1.5	V
· · ·	High-level output voltage	V _{CC} =4.75V	V _I = 0.8V	$I_{OH} = -3mA$	2.4	3.4		V
V _{OH}	High-level output voltage	V _I =2V	$V_1 = 0.5V$	$I_{OH} = -15 \text{mA}$	2			٧
.,	Low-level output voltage	V _{CC} =4.75V		$I_{OL} = 12 \text{mA}$		0.25	0.4	.V
VoL	Low-level output voltage	V ₁ =0.8V, V ₁ =	=2V	I _{OL} =24mA		0.35	0.5	٧
lozн	Off-state high-level output current	V _{CC} =5.25V,	V ₁ =2V , V	0=2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V,	V _I =2V, V	0=0.4V			-20	μΑ
	High level in the course	V _{CC} =5.25V,	V ₁ =2.7V				20	μА
lін	High-level input current	V _{CC} =5.25V,	V _I =I0V				0.1	mΑ
lıL '	Low-level input current	V _{CC} =5.25V,	V1=0.4V				-0.2	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V,	V ₀ =0V		-40		-225	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V	$V_{l} = 0 V_{r}$	V _I = 4.5V		17	27	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, \	V _{CC} =5.25V, V _I =0V			27	46	mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V	V ₁ =4.5V			32	54	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

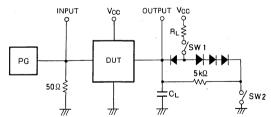
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		8	18	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		15	30	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		12	18	· ns



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

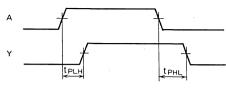
Note 3: Measurement circuit

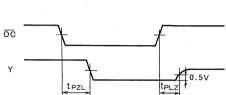


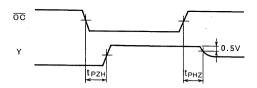
Symbol	SW 1	3W2
t _{PZH}	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$

(3) C_L includes probe and jig capacitance.







OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS245P is a semiconductor integrated circuit containing of 8 bus transmitter/receiver circuits with non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Low input load factor (pnp input)
- Input/output A and output/input B have hysteresis characteristics (Hysteresis = 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

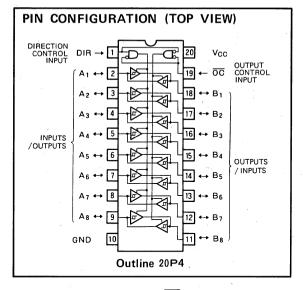
APPLICATION

General digital equipment for industrial and consumer use

FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected alternately to form a bi-directional buffer.

With hysterisis characteristics in the input section of input/output A and output/input B, noise margin is high. The use of a pnp transistor input has made the input load factor small. The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal. On the contrary, when DIR is low, B is the input terminal and A is the output terminal.



When the output control input \overline{OC} is high, both A and B, in a high-impedance state, are separated.

FUNCTION TABLE (Note 1)

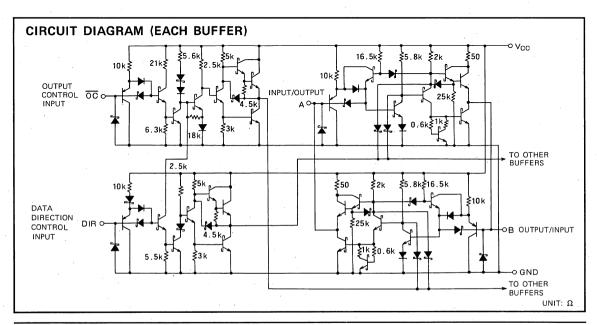
	ŌĊ	DIR .	Α	В
	L	L	0	1
	٦	н	1	0
.	Н	Χ .	Z	Z

Note 1: | : input

O: output (noninverted output)

Z: high-impedance

X: irrelevant



OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
	1	A, B		-0.5~+5.5	V
VI	V _I Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		Off-state	-0.5~+5.5	. V
Topr	Operating free-air ambient temperature range			-20~+75	rc
Tstg	Storage temperature ran	ge .		- 65~ +150	ర

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

	D			Limits			
Symbol	Parami	Parameter		Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
	18-6 1	V _{OH} ≥ 2.4 V	0		-3	mA	
Іон	High-level output current	V _{OH} ≧ 2V	0		— 15	mA	
	1	V _{OL} ≤ 0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≤ 0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

	D		Test conditions			Limits		Unit	
Symbol	rarameter		Test conditions		Parameter Test conditions	Min	Тур	Max	Ont
VIH	High-level input voltage				2			V	
· VIL	Low-level input voltage						0.8	V	
$V_{T+}-V_{T-}$	Hystersis		V _{CC} =4.75V		0.2	0.4		V	
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	V	
V	High-level output voltage		V _{CC} =4.75V	I _{OH} = - 3mA	2.4	3.4		V	
Voн	migri-rever output vortage		$V_1 = 0.8V, V_1 = 2V$	I _{OH} = - 15mA	2			V	
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12mA			0.4	V	
VoL	Low-level output voltage		$V_1 = 0.8V, V_L = 2V$	I _{OL} =24mA			0.5	V	
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_I = 0.8V,$	$V_1 = 2V, V_0 = 2.7V$			20	μΑ	
lozL	Off-state low-level output	current	V _{CC} =5.25V, V _I =0.8V,	$V_1 = 2V, V_0 = 0.4V$			-200	μΑ	
		А, В	V 5 25V V 2 3				20	μΑ	
	High-level input current	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.7$	V			20	μΑ	
Iн	riigii-ievei iriput current	А, В	V _{CC} =5.25V, V _I =5.5	V			0.1	mA	
. !		DIR, OC	V _{CC} =5.25V, V _I = 10	/			0.1	.mA	
IIL	Low-level input current		V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.2	mA	
los	Short-circuit output curre	ent (Note 2)	V _{CC} =5.25V, V _O = 0 V		- 40		-225	mA	
Гссн	Supply current, all outpu	ts high	V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5V		48	70	mA	
ICCL	Supply current, all outputs low $V_{CC}=5.25V$, $V_I=0$ V, $V_I=4.5V$		/, V _I = 4.5V		62	90	.mA		
Iccz	Supply current, all outpu	ts off	V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5V		64	95	mA	

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

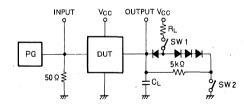
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C unless otherwise noted)

	Parameter	T	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
tpLH	· Low-to-high-level, high-to-low-level output propagation	0 : 45-5 (44 - 0)		10	. 15	ns
t _{PHL}	time, from input A, B to output B, A	C _L =45pF (Note 3)		10	.15	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		25	40	ns
t _{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		23	40	ns
tpLZ	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		15	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		14	25	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

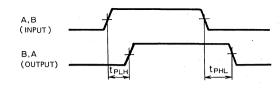
Note 3: Measurement circuit

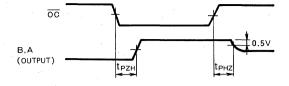


Symbol	SW1	SW2
t PZH	Open	Closed
t _{PZL}	Closed	Open
tplz	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

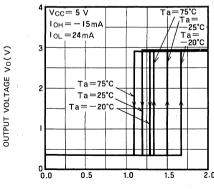




B,A (OUTPUT) tpz 10.5V

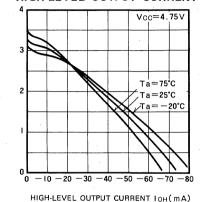
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE

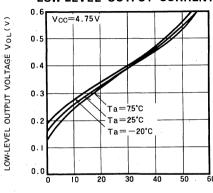


INPUT VOLTAGE VI (V)

HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT CURRENT IOL (mA)

HIGH-LEVEL OUTPUT VOLTAGE VOH(V)

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

DESCRIPTION

The M74LS247P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO outputs for zero suppression
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=-20~+75°C)

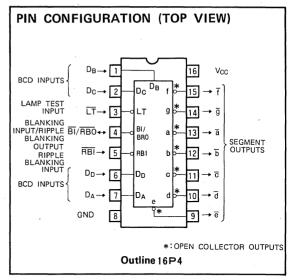
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment ouputs $\overline{a} \sim \overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a} \sim \overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, therby making it possible to drive directly a 7-segment LED for the display of anode-common numbers.

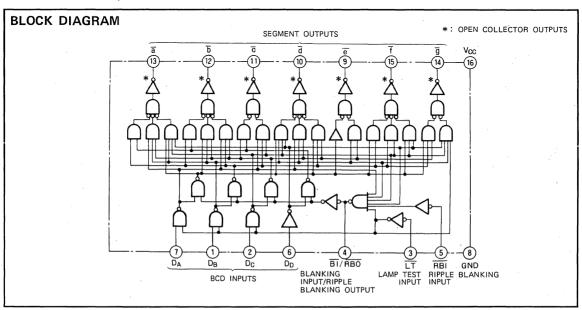
Suppression of the unnecessary high-order zeroes is possible by setting the highest order \overline{RBI} ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-level \overline{RBI} for each of the digits. Refer to the M74LS47P for the application example.



By setting blanking input $\overline{BI}/\overline{RBO}$ low, outputs $\overline{a}\sim\overline{g}$ are set high and the display element is extinguished irrespective of the status of the other inputs. Since $\overline{BI}/\overline{RBO}$ serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input \overline{LT} low, $\overline{a} \sim \overline{g}$ are set low irrespective of the status of $\overline{BI}/\overline{RBO}$, D_A , D_B , D_C and D_D , all the segments in the display element are lighted and each segment can be tested. Refer to M74LS47P for the $\overline{BI}/\overline{RBO}$ and $a\sim g$ circuits.

The only difference between the M74LS247P and M74LS47P is the configuration of the 6 and 9 numerals.



BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	ĹΤ	RBI	D _D	Dc	DB	DA	BI/F	RBO	ā	Б	ō	đ	ē	f	g	Note
0	Н	Н	L	L	L	L		Н	L	L	L	. L	L	L	Н	
. 1	Н	Χ.	L	L	L	H		Н	Н	L	L	Н	Н	Н	н	
2	Н	Х	L	L	Н	L		Н	L	L	Н	L	. L	Н	L]
3	Н	Х	L	L	Н	Н		Н	L	L	L	L	Н	Н	L	
4	Н	X	L	Н	L	L		Н	Н	L	L	Н	Н	L	L	
5	Н	×	L	Н	L	Н		Н	L	Н	L	L	Н	L	L	
6	Н	Х	L	Н	Н	L		Н	L	Н	L	L	L	L	L	1
7	Н	Х	L	Н	Н	н		Н	L	L	L	Н	Н	Н	Н	1,,
8	н	X.	Н	. L	٦	L		Н	L	L	L	L	L	L	L	(1)
9	Н	· X	Н	L	L	Н		Н	L	L	L	L	Н	L	L	
10	Н	X	Н	L	Н	L		Н	Н	Н	Н	L	L	Н	, L	
11 .	Н	Х	Н	L	Н	Н		Н	Н	Н	L	L	Н	Н	L	
12	Н	X	Н	ŀН	L	L		н	Н	L	. н	Н	Н	L	L	
13	Н	Х	Н	Н	L	Н		Н	L	Н	Н	L	н	L	L	
14	Н	Х	Н	Н	Н	L		Н	Н	Н	Н	L	L	L	L	
15	Н	Х	Н	Н	Н	Н		Н	Н	Н	Н	Н	Н	Н	Н	1
Blanking	X	Х	Х	Х	X	· X	L		Н	Н	Н	Н	Н	Н	Н	(2)
Ripple blanking	,H	L	L	L	L	L		L	Н	Н	Н	Н	н.	Н	Н	(3)
Lamp test	L	×	×	Х	Х	X		Н	L	L	L	L	L	· L	L	(4)

Note 1. (1) LT is normally kept in high.

RBI is kept open or in high with a decimal 0 output.

DEFINITION OF SEGMENTS

- (2) When BI/RBO is low, all the segment outputs are high irrespective of the status of the other inputs.
- (3) All the segment outputs are set high and $\overline{BI/RBO}$ is set low when \overline{RBI} , D_A , D_B , D_C and D_D are set low with \overline{LT} high.
- (4) When LT is low, all the segment outputs are low.
- X: Irrelevant

CHARACTERS DISPLAYED



ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parame	ter	Conditions	Limits	Unit
Vcc	Supply voltage '			-0.5~+7	V
.,	Input voltage	Input BI/RBO		-0.5~V _{CC}	V
Vı	input voltage	Other inputs	·	-0.5~+15	V
	Output voltage	Output BI/RBO	High-level state	-0.5~V _{CC}	V
Vo	Output voltage	Other outputs	Trigit-level state	-0.5~+15	V
lO(peak)	Output current		tw≤1ms, dutycycle≤10%	200	mA
10	Output current		High-level state	1	mΑ
Topr	Operating free-air ambient	temperature range	1	-20~+75	°C
Tstg	Storage temperature range			−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 - +75°C, unless otherwise noted)

0	D	Parameter				
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current, outputs $\overline{a} \sim \overline{g}$	V _{OH} = 15 V	0		250	μА
Іон	High-level output current, output BI/RBO	V _{OH} ≧2.4V	0		-50	μА
la.	Low-level output current,	V _{OL} ≦0.4V	0		12	. mA
lor .	outputs a ~ g	V _{OL} ≦0.5V	0		24	mA
	Low-level output current,	V _{OL} ≦0.4V	0		1.6	mA
loL	output BI/RBO	V _{OL} ≦0.5V	0	•	3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

ELECTRICAL CHARACTERISTICS (Ta = -20 - +70°C, unless otherwise noted)

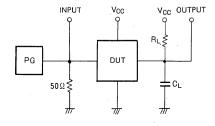
	D		Tost condi			Limits		11
Symbol	Parameter		Test condi	lions	Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
VoH	High-level output voltage, output	ıt BI/RBO	$V_{CC} = 4.75V$ $I_{OH} = -50\mu A$		2.4	4.2		V
Гон	High-level output current, output	ıts ā ~ g	V _I =0.8V, V _I =2V	V ₀ =15V			250	μА
		0.44-		I _{OL} =12mA		0.25	0.4	V
.,	Low-level output voltage	Outputs $\overline{a} \sim \overline{g}$	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	V
VoL	Low-level output voltage	Output BI/RBO	V ₁ =0.8V, V ₁ =2V	I _{OL} =1.6mA		0.25	0.4	V
		Corbot BIN NBO		I _{OL} =3.2mA		0.35	0.5	V
	High-level input voltage, except	input DI/DDO	V _{CC} =5.25V, V _I =2.7	v			20	μА
Ιн	High-level hipat voltage, except	Input BI/ RBO	V _{CC} =5.25V, V _I =10V	/			0.1	mA
1	Low-level input current	Input BI/RBO	V E 25V V 0 4	V			-1.2	mA
l _{IL}	Low-level input current	Other inputs	$V_{CC} = 5.25V, V_{I} = 0.4$	V			-0.4	mA
los	Short-circuit output current, ou	tput BI/RBO	V _{CC} =5.25V, V ₀ =0V	1	-0.3		-2	mA
loc	Supply current		V _{CC} = 5.25V (Note 2)			7	13	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

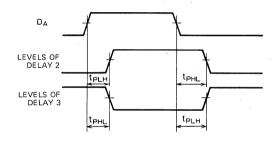
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

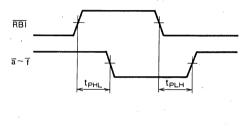
Symbol	Parameter	Test conditions		Limits	Unit	
,Symbol		rest conditions	М	in Typ	Max	Oilit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	D cor o		35	100	ns
t _{PHL}	time, from input D_{A} to outputs $\overline{a} \sim \overline{g}$	$R_L = 665 \Omega$ $C_L = 15 pF$		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 3)		50	100	ns .
tpHL	time, from input \overline{RBI} to outputs $\overline{a} \sim \overline{f}$			45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





Note 2. I_{CC} is measured with all inputs at 4.5V.

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

DESCRIPTION

The M74LS248P is a semiconductor integrated circuit provided with a BCD-to-7-segment decoder/driver function and 2kohm (typ) pull-up resistor outputs.

FEATURES

- Suitable for lighting 7-segment display element
- RBI input and BI/RBO output for zero suppression
- LT input for lamp testing
- BI/RBO input for blanking all segments
- NPN transistor can be externally mounted for highcurrent drive.
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

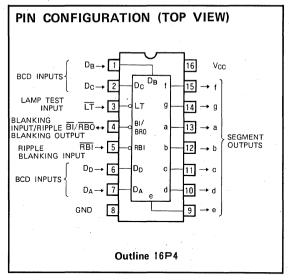
FUNCTIONAL DESCRIPTION

This IC is a version of the M74LS247P without the output transistors. When numbers are specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs a~g are set high in accordance with those numbers. These outputs have built-in $2k\Omega$ pull-up resistors suited to driving common-cathode LEDs. High-current display elements can be driven by connecting NPN transistors to the outputs.

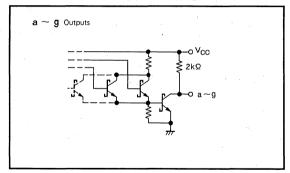
The ripple blanking, blanking and lamp test functions are the same as those for the M74LS247P.

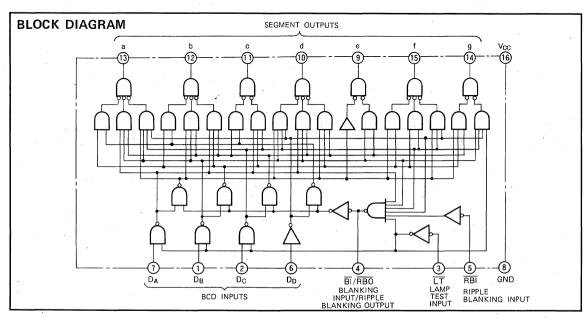
Refer to the M74LS47P for the application example.

The only difference from the M74LS48P is the configuration of the 6 and 9 numerals.



OUTPUT CIRCUIT SCHEMATIC





BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	D _D	Dc	DB	DA	BI/F	RBO	а	b	С	d	е	f	g	Note
. 0	Н	Н	L	L	L	L		Н	Н	Н	Н	Н	Н	Н	L	
1	Н	Х	L	L	L	Н		Н	L	Н	Н	L	L	L	L	1
2	Н	Х	L	L	Н	L		Н	Н	Н	L	Н	Н	L	Н	
3	Н	Х	L	L	Н	Н		Н	Н	Н	Н	Н	L	L	Н	
4	Н	Х	L	Н	L	L		Н	L	н	Н	L	L	Н	Н] -
5	Н	X	L	Н	L	Н		Н	Н	L	Н	Н	L	Н	Н	1
6	Н	X	L	Н	Н	L		Н	Н	L	Н	Н	Н	Н	Н	1
7	н	Х	L	Н	Н	Н		Н	Н	Н	Н	L	L	L	L	(1)
8	Н	X	. Н	L	L	L		Н	Н	Н	Н	Н	Н	Н	Н	(1)
9	н	Х	н	L	L	Н		Н	Н	Н	Н	Н	L	Н	Н]
10	Н	X	Н	L	Н	L		Н	L	L	L	Н	Н	L	Н]
. 11	Н	X	Н	L	H	Н		Н	L	L	Н	Н	L	L	Н	1
12	Н	Х	Н	Н	L	L		Н	L	Н	L	L	L	Н	Н	1
13	Н	X	Н	Н	٦	Н		Н	Н	L	L	Н	L	Н	Н]
14	Н	Х	Н	Н	Н	L		Н	L	L	L	Н	Н	Н	Н	1
15	Н	X	Н	Н	Н	Н		Н	L	L	L	L	L	L	L	1
Blanking	Х	Х	Х	Х	X	Х	L		L	L	L	L	L	L	L	(2)
Ripple blanking	н	L	L	L	L	L		L	L	L	L	L	L	L	L	(3)
Lamp test	L	Х	Х	Х	Х	Х		Н	Н	Н	Н	Н	Н	Н	Н	(4)

Note 1. (1) LT is normally kept in high.

RBI is kept open or in high in case of a decimal 0 output.

DEFINITION OF SEGMENTS

- (2) When BI/RBO is low, all the segment outputs are low irrespective of the status of the other inputs.
- (3) All the segment outputs are set low and $\overline{BI/RBO}$ is set low when \overline{RBI} , D_A , D_B , D_C and D_D are set low with \overline{LT} high.
- (4) When \overline{LT} is low, all the segment outputs are high.

X: Irrelevant



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5 .	6	7	8	9	10	11	12	13	14	15
Character	\Box		U	3	. 4	5	σı	7	8	9	U	٦	U	_	٤	

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage		·	-0.5~+7	V
Vı	Input voltage	Input BI/RBO		-0.5~Vcc	V
VI	input voltage	Other inputs		- 0.5 ~ + 15	V
\/-	Output voltage	Output BI /RBO	High-level state	-0.5~Vcc	V
Vo	Output voltage	Other outputs	inginevel state	-0.5~Vcc	V
Topr	Operating free-air ambient temp	perature range		−20 ~ +75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	Parameter			Limits		
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current, outputs a∼g	V _{OH} ≧2.4V	0		- 100	μА
Іон	High-level output current, output BI/RBO	V _{OH} ≧2.4V	0		- 50	μА
		V _{0L} ≤0.4V	0		2	mA
loL	Low-level output current, outputs, a∼g	V _{QL} ≦0.5V	0		6	mΑ
	Low-level output current, output BI/RBO	V _{OL} ≤0.4V	0		1.6	mA
loL	Low-level output current, output BI7RBO	V _{OL} ≦0.5V	0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70^{\circ}C$, unless otherwise noted)

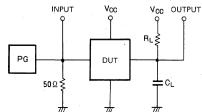
Cumbal	Paramete		Took one did			Limits		Unit
Symbol	Paramete		Test condit	ions	Min	Typ *	Max	Unit
VIH	High-level input voltage				2			V .
VIL	Low-level input voltage						0.8	>
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	>
.,	High-level output voltage	Outputs a∼g	V _{CC} = 4.75V	$I_{OH} = -100 \mu A$	2.4	4.2		>
Voн	High-level output voltage	Output BI/RBO	$V_1 = 0.8V, V_1 = 2V$	$I_{OH} = -50 \mu \text{ A}$	2.4	4.2		V
Іон	High-level output current	Outputs a ~ g	Vcc=4.75V, Vi=0.8V,	$V_1 = 2V, V_0 = 0.85V$	-1.3	-2		mA
		0		I _{OL} =2mA		0.25	0.4	٧
	Low-level output voltage	Outputs a ~ g	V _{CC} =4.75V	I _{OL} =6mA		0.35	0.5	V
VoL	Low-level output voltage	Output BI/RBO	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =1.6mA		0.25	0.4	V
		Output BI/RBO		I _{OL} =3.2mA	-	0.35	0.5	٧
	I that is not a second	5 57./556	V _{CC} =5.25V, V _I =2.7	v .			20	μА
Ιн	High-level input current	Except input BI/RBO	V _{CC} =,5.25V, V _I =10V				0.1	mA
, ,	Lauriandian di	Input BI/RBO					-1.2	mA
lıL.	Low-level input current '	Other inputs	$V_{CC} = 5.25V \cdot V_I = 0.4$	v			-0.4	mA
los	Short-circuit output current	Output BI/RBO	V _{CC} =5.25V, V _O =0V		-0.3		· -2	· mA
loc	Supply current		V _{CC} = 5.25V (Note 2)			25	38	mΑ

f * : All typical values are at V_{CC}= 5V, T_a= 25°C. Note 2. I_{CC} is measured with all inputs at 4.5V.

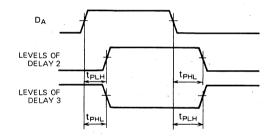
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

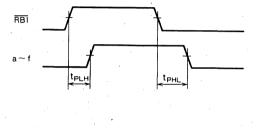
Symbol	Parameter	Test conditions		Unit		
Symbol	ratameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =4kΩ		30	100	ns
tpHL	time, from input $D_{\mathbf{A}}$ to outputs a \sim g	C _L =15pF (Note 3)		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =6kΩ		40	100	ns
t _{PHL}	time, from input RBI to outputs a ~ f	C _L =15pF (Note 3)		45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





M74LS251P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER
WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS251P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function and 3-state outputs.

FEATURES

- 3-state outputs
- Complementary output provided
- Wide operating temperature range (T_a=-20~+75°C)

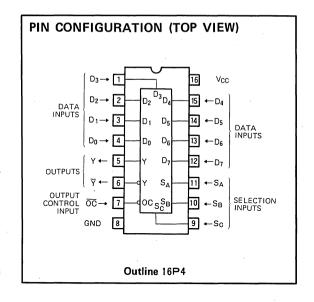
APPLICATION

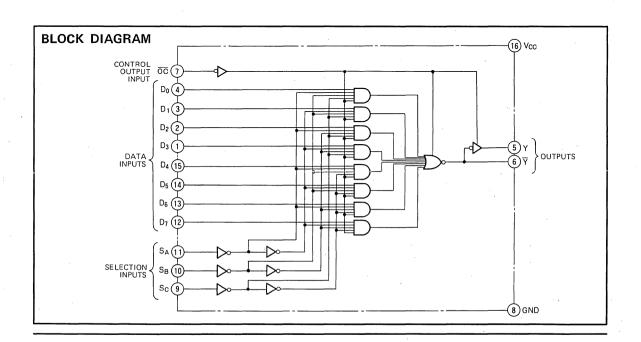
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and using a multiplexer function which converts the 8-bit parallel data into serial data by time-sharing. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A , S_B and S_C , the input signal is at output Y and the inverted signal from output \overline{Y} . When output control input \overline{OC} is set high, Y and \overline{Y} are put in the high-impedance state and the outputs are completely isolated.

M74LS251P has the same functions and pin connections as M74LS151P but the latter is provided with active pull-up resistor outputs.





8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

Sc	SB	SA	ōc	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Υ	Y
×	×	×	Н	×	×	×	×	×	×	×	×	· Z	Z
L	L	L	L	L	×	×	×	х	x	×	×	L	Н
L	· L	L	L	Н	X .	×	Χ .	×	×	×	×	н	L
L	L	н .	L	×	L	×	×	×	×	×	×	L	н
L	L	Н	L	×	Н	×	×	×	X	×	×	н	L
L	н	L	L	×	×	L	×	×	×	×	x	L	Н
L	Н.	L	Ļ	×	×	Н	×	×	×	×	×	н	L
L	н	н	L	×	×	×	L	×	X	×	×	L	Н.
L	Н	н	L	×	×	. x	н	. ×	×	X	×	Н	L,
Н	L	L	L	×	×	×	×	L	×	×	· x	L.	Н
Н	L	L	L	×	×	×	×	н	×	×	×	н	L
Н	L	Н	L	×	×	×	×	×	L	×	×	L	н
Н	L.	н	L	X	×	×	×	×	н	×	×	Н	, L
Н	н	. L	L	X .	×	×	X	×	×	Ŀ	×	\ L '	н
H	н	L	L	×	×	×	×	×	×	Н .	×	Н	L
Н.	н	н	L	×	×	×	×	×	×	×	L	L	н
Н	Н	Н	L '	×	×	×	×	×	×	×	Н	Н	L

Note 1 X : Irrelevant

Z: High-impedance state

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
VI -	Input voltage		-0.5~+15	٧
Vo	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		<u>−65∼+150</u>	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits		Unit
Symbol	Parameter		Min	Тур	Max	Ont
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mA
		V _O L≦0.4V	0		4	mA `
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Combal	Parameter	Tost and	isiana		Limits		01-24
Symbol	rarameter	l est cond	Test conditions			Max	Unit
V _{IH}	High-level input voltage						V
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	– 18 mA			-1.5	V
V _{OH}	High-level output voltage	1	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-2.6mA$		3.1		٧
VoL	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I = 2 V			0.25	0.4	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V	V, V ₀ =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V	V, V ₀ =0.4V			-20	μА
	I Balance I and a second a second and a second a second and a second a second and a	V _{CC} =5.25V, V _I =2.	.7V			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10	V _{CC} =5.25V, V _I =10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-30		130	mA
Icc	Supply current	V _{CC} =5.25V (Note 3	V _{CC} =5.25V (Note 3)		6.1	10	mA
Iccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4	1)		7.1	12	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Took on a division of		Limits		
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			22	45	ns
t _{PHL}	time, from inputs S_A , S_B , S_C to output Y			18	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	33	ns
t _{PHL}	time, from inputs S_A , S_B , S_C to output \overline{Y}	C ₁ = 15 pF (Note 5)		15	33	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL 13pr (Note 5)		15	28	ns
t _{PHL}	time, from inputs D ₀ ~D ₇ to output Y	·		14	28	ns
t _{PLH}	Low-to-high-level, nigh-to-low-level output propagation			7	15	ns
t _{PHL}	time, from inputs $D_0 \sim D_7$ to output \overline{Y}			7	15	ns
t _{PZH}	High-level output enable time, from input OC to output Y	5 00 0 45 5 111 71		11	45	ns
t _{PZL}	Low-level output enable time, from input OC to output Y	$R_L=2k\Omega$, $C_L=15$ pF (Note 5)		16	40	ns
t _{PZH}	High-level output enable time, from input \overline{OC} to output \overline{Y}	$R_1 = 2k\Omega$. $C_1 = 15pF$ (Note 5)		11	27	ns
t _{PZL}	Low-level output enable time, from input \overline{OC} to output \overline{Y}	HL=2KY, GL=15pr (Note 5)		13	40	ns
t _{PHZ}	High-level outpout disable time, from input OC to output Y			16	45	ns
t _{PLZ}	Low-level output disable time, from input \overline{OC} to output Y	$R_L=2k\Omega$, $C_L=5$ pF (Note 5)		8	25	ns
t _{PHZ}	High-level output disable time, from input \overline{OC} to output \overline{Y}	5 50 5 5 10 45		18	55	ns
t _{PLZ}	Low-level output disable time, from input \overline{QC} to output \overline{Y}	$R_{\perp}=2k\Omega$, $C_{\perp}=5$ pF (Note 5)		9	25	ns

^{*:} All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly.

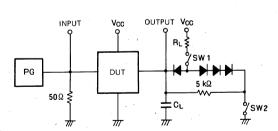
Note 3: I_{CC} is measured with OC at 0V and all other inputs at 4.5V

Note 4: I_{CCZ} is measured with all inputs at 4.5V.

M74LS251P

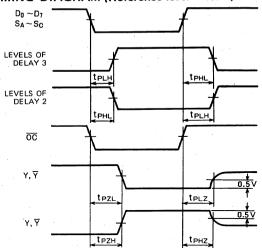
8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

Note 5: Measurement circuit



- The pulse generator (PG) has the following characteristics:
 PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_P, Z_O=50Ω.
- (2) All diodes are switching diodes. (trr ≤ 4ns)
- (3) C₁ includes probe and jig capacitance

Symbol	SW 1	SW2
t pzņ	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t phz	Closed	Closed



M74LS253P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS253P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Selection inputs common to both circuits
- Output control inputs separate for each circuit
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

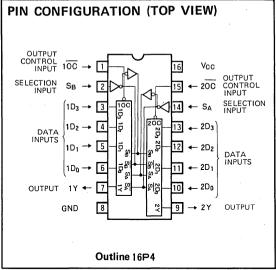
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data by time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 , and 1 data is specifed from among the data input by selection inputs S_A and S_B , the input signal is output at Y. By applying 4-bit parallel data to data inputs D_0 , D_1 , D_2 and D_3 and by connecting the output of a synchronous divide-by-four counter to S_A and S_B , data D_0 , D_1 , D_2 and D_3 appear in the order of D_0 , D_1 , D_2 and D_3 , synchronized with the clock pulse. S_A and S_B are common to both circuits while output control inputs $1\overline{OC}$ and $2\overline{OC}$ are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, 1Y and 2Y are put in the high-impedance state ("Z") irrespective of the status of the inputs.

M74LS253P has the same functions and pin connections as M74LS153P but the latter is provided with active pull-up resistor outputs.

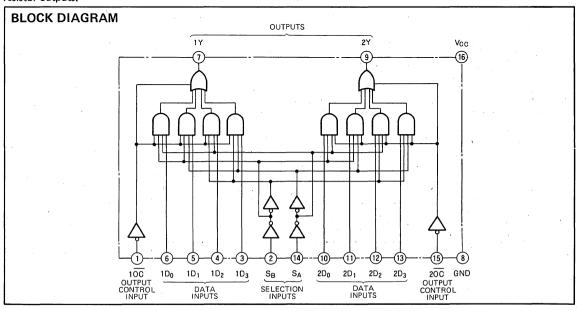


FUNCTION TABLE (Note 1)

S _B	SA	D ₀	D ₁	D ₂	D ₃	ŌC	Υ
X	Х	X	×	×	Х	Н	z
L	L	L	Х	×	х	Γ.	L
L	L	Н	Х	×	X	L	н
L	Н	х	L	×	×	Γ	L
L	Н	×	Н	×	X	L	Н
Η	L	X	X	L	×	L	Ľ
Н.	L	×	×	Н	X	L	Н
Н	н	×	Х	×	L	L	L
Н	н	Х	Х	×	Н	L	Н

Note 1 X : Irrelevant

Z: High-impedance state



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = $-20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage		V	-0.5~+7	٧
٧ı	Input voltage			-0.5~+15	٧
V ₀	Output voltage	Off-state		-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range			-20~+75	°C
Tsta	Storage temperature range	-		-65~+150	ъ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Complete				Limits		Unit
Symbol	Parame	ter	Min	Тур	Max	Onit
. Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA
loL Lo	Low-level output current	V ₀ L≦0.4V	0		4	mA
	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol		Test condition	<u> </u>		Limits		Unit
Symbol	Parameter	Test condition	ons ·	Min	Typ ★	Max	Unit
VIH	High-level input voltage						٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18	mA .			-1.5	٧
Voн	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-2.6m_{P}$	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-2.6mA$		3.1		٧
V _{OL}	Low-level output voltage	$V_{CC}=4.75V$ $V_{I}=0.8V, V_{I}=2V$	I _{OL} = 4 mA I _{OL} = 8 mA		0.25	0.4 0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I = 2 V,	V ₀ =2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I = 2 V,	V _O =0.4V			-20	μА
	High level in the second	V _{CC} =5.25V, V _I =2.7V				20	μА
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA ·
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V	V _{CC} =5.25V, V _O = 0 V			— 130	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V (Note 3)	V _{CC} =5.25V (Note 3)		7	12	mA
locz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)			8.5	14	mA

 $[\]star$: All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: ICCL is measured with all inputs at OV.

Note 4: I_{CCZ} is measured with $1\overline{OC}$ and $2\overline{OC}$ at 4.5V and all other inputs at OV.

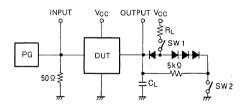
SWITCHING CHARACTERISTICS (Vcc= 5 V, Ta=25°C, unless otherwise noted)

		Test conditions		Limits		11.2
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	25	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output Y	C ₁ = 15pF (Note 5)		12	20	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	CL= 15pF (Note 5)		12	45	ns
t _{PHL}	time, from inputs SA, SB to output Y			12	32	ns
t _{PZH}	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		11	28	ns
t _{PZL}	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		12	23	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		15	41	ns
t _{PLZ}	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		9	27	ns

M74LS253P

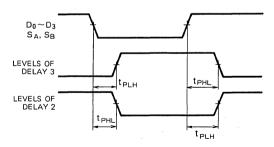
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

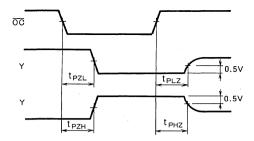
Note 5: Measurement circuit



Symbol	SW1	SW2
tpzh	Open	Closed
tpzL	Closed	Open
tpLZ	Closed	Closed
tphz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR-1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω . All diodes are switching diodes. ($t_{rr} \le 4$ ns)
- C_L includes probe and jig capacitance.





DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS256P is a semiconductor integrated circuit containing a dual demultiplexer circuit configured into a 4-bit latch addressable in 2-bit binary code.

FEATURES

- Easily expandable
- May be used as a 2-bit binary-to-quaternary decoder/ demultiplexer
- Active low common reset
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

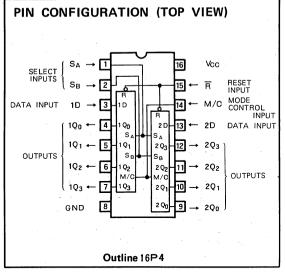
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device is configured from two circuits providing the capability to function as a 2- bit binary-to-quaternary demultiplexer or as a 4-bit latch. The operational modes listed below are selectable using mode control input M/C (common to both circuits) and reset input \overline{R} in combination.

- (1) 2-bit binary-to-quaternary decoder/demultiplexer
- (2) Addressable latch
- (3) Data input inhibit
- (4) Reset

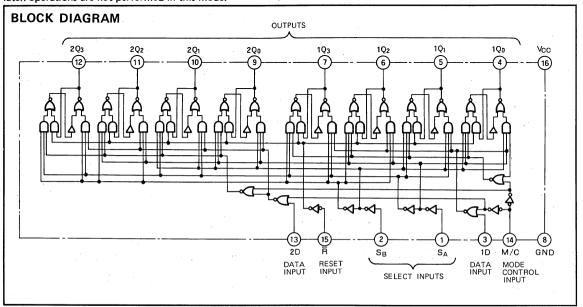
When used as a 2-bit binary-to-quaternary decoder/demultiplexer and a 2-bit binary number is applied to select inputs S_A and S_B , one of the $Q_0 \sim Q_3$ outputs will correspond to that number, and the signal appearing at its output will be the same as the one present at data input D. All other outputs will remain low-level at this time; and latch operations are not performed in this mode.



When used as an addressable latch, S_A and S_B will be recified as in the above operation, with the corresponding tch being selected. The signal present at data input D will then appear at output. When M/C transits from low to high (data inhibit mode), the information present at D immediately prior to that event will be latched. When M/C is low-level, changing the signal at D will also change the signal present at Q.

During the data input inhibit mode, changes applied to D will not affect $O_0 \sim O_3$, and the status prior to M/C transiting high will be held.

Direct reset is activated by all outputs at low-level, regardless of the status of D, S_A , and S_B .



DUAL 4-BIT ADDRESSABLE LATCH

FUNCTION TABLE (Note 1)

Operational mode	R	M/C	D	SA	SB	Q ₀	Q1	Q ₂	Q ₃
Reset	L	Н	Χ.	Х	Х	L	L	L	L
	L	L	, L	L	L	L	L	L	٦
	L	L	Η	L	L.	Η	L	Г	٦
	L	L	L	Н	L	L	L		L
Active high 4-channel	L	٦.	Н	Н	L	L	Н	با	L
demultiplexers	L	L	L	L	Н	L	L	L	Г
	L	L	Н	L	н	L	L	Η	L
	L	L	L	Н	Н	L	L	L	Γ
	L	L	Н	н	Н	L	L	٦	Н
Memory	Н	Н	×	×	Х	Q ₀ ⁰	Q1 ⁰	Q2 ⁰	Q ₃ ⁰
	н	L	L	L	L	L	Q1 ⁰	Q2 ⁰	Q3 ⁰
	Н	L	н	L	L	Н	Q 1 ⁰	Q2 ⁰	Q3 ⁰
	Н	L	L	Н	L	Q ₀ ⁰	L	Q2 ⁰	Q ₃ ⁰
Addressable latch	Н	L	Н	Н	L	Qo ⁰	Н	Q2 ⁰	Q3 ⁰
Addressable latch	Н	L	L	L	Н	Q ₀ ⁰	Q1 ⁰	L	Q ₃ ⁰
	Н	L	Н	, L	Н	Q ₀ ⁰	Q 1 ⁰	Н	Q3 ⁰
	Н	, L	L	Н	н	Qo ⁰	Q 1 ⁰	Q2 ⁰	L
	Н	L	Н	Н	Н	Q ₀ ⁰	Q1 ⁰	Q2 ⁰	Н

Note 1. X : Irrelevant

Q 0: Indicates output status prior to input conditions being set.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted.)

Symbol	Barrana	Parameter		Limits			
Syllibol	raramete	er	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≧2.7V	0		- 4 00	μА	
1		V ₀ L≤0.4V	0		4	mΑ	
loL	Low-level output current	V ₀ ∟≦0.5V	0		8	mA	

DUAL 4-BIT ADDRESSABLE LATCH

ELECTRICAL CHARACTERISTICS (T_a = −20~+75 °C, unless otherwise noted)

0	Parameter.		T	• • • • • • • • • • • • • • • • • • • •		Limits		Unit	
Symbol	Parameter		lest condi	Test conditions		Min Typ ★ Max		7 "	
VIH	High-level input voltage				2			. V	
VIL	Low-level input voltage		-				0.8	٧	
V _{IC}	Input clamp voltage		V _{CC} =4.75V.I _{IC} =-	18mA			-1.5	٧	
	Literal entered unlane		V _{CC} =4.75V. V _I =0.8	3V	2.7	3.4			
VoH	High-level output voltage		Vi=2V. IOH=-400/	Α	2.1	3.4		V	
			V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$ $I_{OL} = 8mA$		0.3		0.5	V	
		M/C	V 5 25V V 2 3				40	μA	
l	History is an annual an	Exclusive of M/C	V _{CC} =5.25V, V _I =2.7	V			20	μА	
Ιн	High-level input current M/C V _{CC} =5,25V, V _L =10V	,			0.2	mA			
		Exclusive of M/C	VCC=5.25V, V[=100	,			0.1		
		M/C					-0.8	4	
hL.	Low-level input current	Exclusive of M/C	V _{CC} =5.25V, V _I =0.4V				-0.4	mA	
los	Short-circuit output current (No	ote 2)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA	
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	36	mA	

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

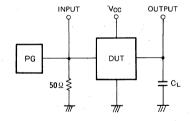
SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
- Cymbol	Tarameter	rest conditions	Min	Тур	Max	Onit
t _{PHL}	High-to-low-level output propagation time, from input \overline{R} to output $\Omega_0{\sim}\Omega_3$			9	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	32	ns
tpHL	time, from input D to output $Q_0 \sim Q_3$			11	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15 pF (Note 4)		15	38	ns
tphL	time, from input S_A , S_B to output $Q_0 \sim Q_3$			11	29	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			14	35	ns
t _{PHL}	time, from input M/C to output $Q_0 \sim Q_3$			13	24	ns

TIMING REQUIREMENTS (Vcc=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Tdisi	Limits			Unit
	rarameter	Test conditions	Min	Тур	Max	Unit
t _{su (DH)}	D high-level setup time to M/C		15	10		ns
th (DH)	D high-level hold time to M/C		5.	- 5		ns
t _{su (DL)}	D low-level setup time to M/C		15	8		ns
th(DL)	D low-level hold time to M/C		. 5	- 7		ns
t _{su(s)}	S _A , S _B setup time to M/C		15	7		ns
th(s)	S _A , S _B hold time to M/C		5	- 5		ns
tw(M/C)	M/C pulse width	1	15	8		ns
tw(R)	R pulse width		15	7		ns

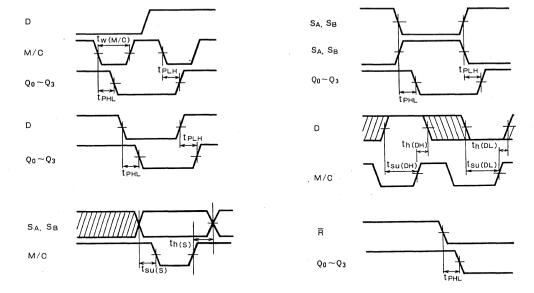
Note 4. Measurement Circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , Z_0 = 50 Ω .
- (2) C_L includes probe and jig capacitance.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} Icc is measured with all inputs at OV.



Note 5. Shaded area denotes the time period in which switching is possible.

M74LS257AP

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS257AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Output control input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

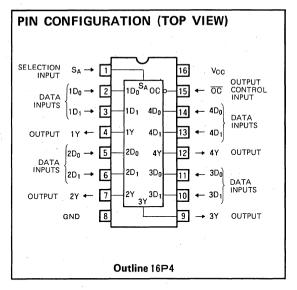
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 1-line selection of 2 input signals using four multiplexer circuits which convert the 2-bit parallel data into serial data by time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1 , and 1 data is specified from among the data input from selection input S_A , the input signal is output at Y.

 S_A and output control \overline{OC} are common to all four circuits. When \overline{OC} is set high, 1Y, 2Y, 3Y and 4Y are put in the high-impedance state irrespective of the status of the other inputs.

M74LS257AP has the same functions and pin connections as M74LS157P but the latter is provided with active pull-up resistor outputs.

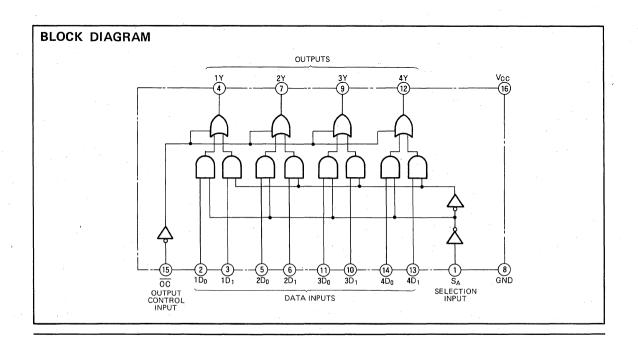


FUNCTION TABLE (Note 1)

ŌC	SA	D ₀	. D ₁	Υ
Н	X	Х	Х	Z
L	L	L	Х	L
L.	L	Н	Х	Н
L	Н	. X	L	L
L	Н	×	Н	Н

Note 1 X: Irrelevant

Z: High-impedance state



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ + 75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
٧ı	Input voltage		-0.5~+15	٧
Vo	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		-20~+75	ొ
Tstg	Storage temperature range		−65∼ + 150	ဗ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Combat	D			Limits		Unit
Symbol	raramete	Parameter		Min Typ Max		Oilit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mA
	Lawleyd arter to area	V _{OL} ≦0.4V	0		12	mÅ
IOL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

0						Limits		Unit
Symbol	Parameter		lest condit	Test conditions		Typ *	Max	Unit
VIH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	· V
V _{OH}	High-level output voltage	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-2.6mA$		3.1		V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	V
VoL	Low-level output voltage		$V_{I}=0.8V, V_{I}=2V$	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =2V, V _O =2.4V				20	μА
lozL	Off-state low-level output curre	nt	V _{CC} =5.25V, V _I =2V, V _O =0.4V				-20	μА
		D ₀ , D ₁ , OC	V _{CC} =5.25V				20	
Local	High-level input current	SA	V ₁ =2.7V				40	μΑ
Iн	riight-level hipat carrett	D ₀ , D ₁ , \overline{OC}	V _{CC} =5.25V				0.1	^
		SA	V ₁ = 10 V				0.2	mΑ
l _{IL}	Low-level input current	D_0 , D_1 , \overline{OC}	V _{CC} =5.25V				-0.4	
'IL	Low-level input current	SA	V _I =0.4V				-0.8	, mA
los	Short-circuit output current (Ne	ote 2)	V _{CC} =5.25V, V _O =0V		-30		— 130	mA
Іссн	Supply current, all outputs high	1	V _{CC} =5.25V (Note 3)			6.2	10	mA
ICCL	Supply current, all outputs low		V _{CC} =5.25V (Note 4)			10	16	mA
locz	Supply current, all outputs off		V _{CC} =5.25V (Note 5)			12	19	mA

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I CCH is measured with \overline{OC} , S_A , D_1 at 0V and D_0 at 4.5V

Note 4: I CCL is measured with all inputs at 0V.

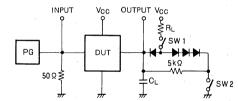
Note 5: I_{CCZ} is measured with \overline{OC} at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, Ta=25°C, unless otherwise noted)

Symbol	Parameter Test conditions			Limits		Unit		
Symbol	rarameter	rest conditions		rest conditions		Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	18	ns		
t _{PHL}	time, from inputs D ₀ , D ₁ to output Y	0		8	18	ns		
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL=45pF (Note 6)		11"	28	ns		
t _{PHL}	time, from input SA to output Y			11	35	ns		
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$ $C_L = 45pF$ (Note 6)		7	22	ns		
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 6)		9	35	ns		
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 6)		11	26	ns		
t _{PHZ}	Output disable time from high-level	R _L =667Ω, C _L =5 pF (Note 6)		. 8	35	ns		

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

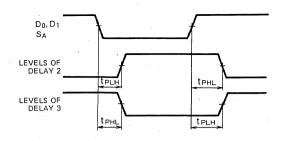
Note 6: Measurement circuit

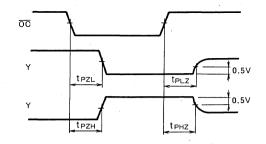


Symbol	SW1	SW2
tеzн	Open	Closed
tezu	Closed	Open
tplz	Closed	Closed
tpHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics:
 - PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$.
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C₁ includes probe and jig capacitance,

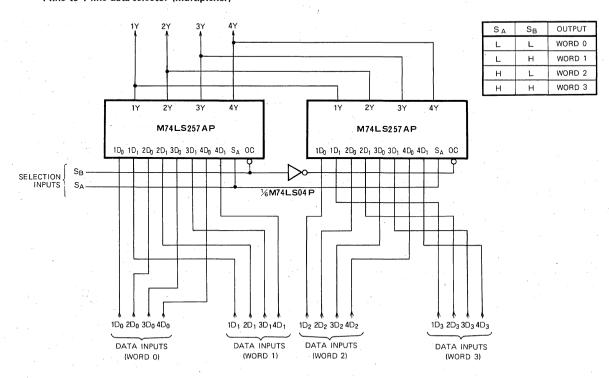
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

4-line to 1-line data selector (multiplexer)



M74LS258AP

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS258AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits with 3-stage outputs.

FEATURES

- Inverted outputs
- Output control input common to all four circuits
- Select input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

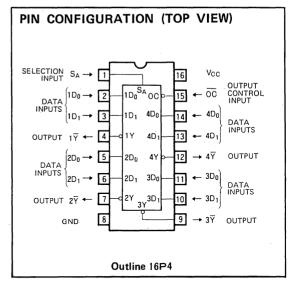
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC contains four sets of circuits which are used 1-line selection 2 input signals and as both data selectors, selecting 1-line out of 2 input signals, and multiplexers which convert the 2-bit parallel data into serial data by time-sharing. When one out of 2-line signals, which are applied to the data inputs D_0 and D_1 , is specified by select from input S_Δ , inverted signal of that appears at output \overline{Y} .

 S_A and output control \overline{OC} are common to all four circuits. When \overline{OC} is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are put in the high-impedance state irrespective of the status of the other inputs.

M74LS258AP has the same functions and pin connections as M74LS158P but the latter is provided with active pull-up resistor outputs.

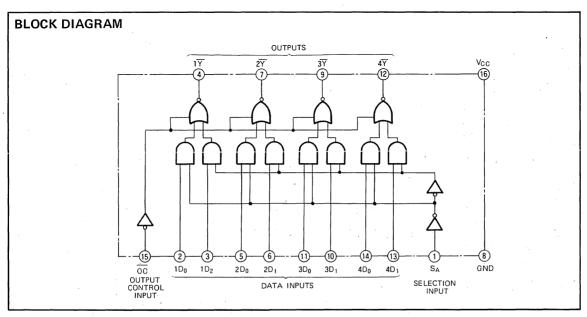


FUNCTION TABLE (Note 1)

OC	SA	D ₀	、 D ₁	Y
Н	×	X	Х	Z
L	L	L	Х	Н
L	L	Н	Х	L
L	Н	Х	L	Н
L	Н	X	н	L

Note 1 X : Irrelevant

Z: High-impedance state



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted.)

Symbol	Parameter		Conditions	Limits	Unit
V _{CC}	Supply voltage			-0.5~+7	V
Vı	Input voltage	, ,		-0.5~+15	V
V ₀	Output voltage	Off-state		-0.5~+5.5	V
Topr	Operating free-air ambient temperature range			-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}$ C, unless otherwise noted.)

	D			Unit			
Symbol	Parameter		Min	Max	- Onit		
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≧2.4V	0		-2.6	.mA	
	Low-level output current	V _{OL} ≦0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mΑ	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Combal	Parameter					Limits	1	0.6
Symbol			Test conditions		'Min	Typ *	Max	Unit
VIH	High-level input voltage			,	2			. ^
VIL	Low-level input voltage						0.8	V
V _{IC}	linput clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA	-		-1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8$ $V_{I}=2V, I_{OH}=-2.6 \text{ r}$		2.4	3. 1		, V
			V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	V
V _{OL}	Low-level output voltage		$V_i = 0.8V, V_i = 2V$	I _{OL} =24mA		0.35	0.5	· V
lozh	Off-state high-level output curr	rent	V _{CC} =5.25V, V _I =2V	, V ₀ =2.7V			20	μА
lozL	Off-state low-level output curre	ent	V _{CC} =5.25V, V _I =2V	, V _O =0.4V			-20	μА
-		D ₀ , D ₁ , OC	V _{CC} =5.25V				20	
	High-level input current	SA	V _I =2.7V				40	μΑ
I _{IH}		D ₀ , D ₁ , OC	V _{CC} =5.25V				0.1	
		SA	V _I = 10V				0.2	mA
L	Low lovel input everent	D ₀ , D ₁ , OC	V _{CC} =5.25V		-		-0.4	^
IIL ·	Low-level input current SA		V ₁ =0.4V				-0.8	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V	1	-30		— 130	mA
Госн	Supply current, all outputs high		V _{CC} =5.25V (Note 3)			4.5	. 7	mA
ICCL	Supply current, all outputs lov	v	V _{CC} =5.25V (Note 4)			8.8	14	mA
lccz	Supply current, all outputs off		V _{CC} =5.25V (Note 5)			12	,19	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			11.24
Symbol	Farameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			5	18	ns
tpHL	time, from inputs D_0 , D_1 to output \overline{Y}	C _L =45pF (Note 6)		8	18	ns
: t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	28	ns
t _{PHL}	time, from input SA to output Y			16	35	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 6)		7	22	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 6)		12	35	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 6)		11	26	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 6)		8	35	ns

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I _{CCH} is measured with all inputs at OV.

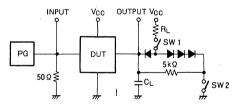
Note 4: I_{CCL} is measured with \overline{OC} , S_A and D_1 at OV and D_0 at 4.5V.

Note 5: 1 CCZ is measured with OC at 4.5V and all other inputs at OV.

M74LS258AP

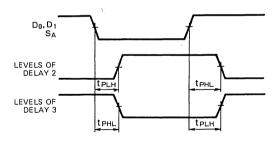
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

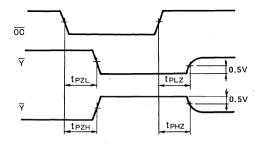
Note 6: Measurement circuit



Symbol	SW1	SW2
tpzh	Open	Closed
tpzL	Closed	Open
tpLZ	Closed	Closed
tphz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) All diodes are switching diodes.
- (3) C_L includes probe and jig capacitance





8-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS259P is a semiconductor integrated circuit containing 8 latch circuits and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- Easy bit expansion
- Usable as 3-bit binary/octal decoder/demultiplexer
- Direct reset input provided
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

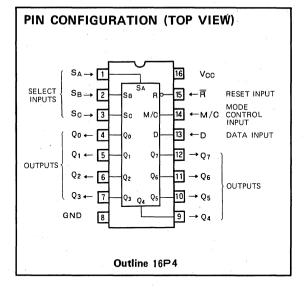
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of a 3-bit binary/octal demultiplexer and 8 latch circuits. The following operational modes can be selected by combining the mode control input M/C with the reset input \overline{R}

(1)	3-bit binary/octal	M/C: Low;
	decoder/demultiplexer	R: Low
(2)	Addressable latch	M/C: Low;
		R̄: High
(3)	Data input inhibit	M/C: High
	*	R: High
(4)	Reset	M/C: High;
		R: Low

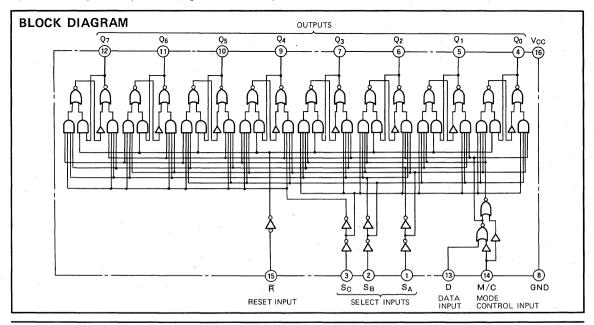
When this device is used as a 3-bit binary/octal decoder/demultiplexer and the select inputs $S_A \sim S_C$ are designated by a 3-bit binary number, the same signal as the data input



D appears in one of the outputs $Q_0 \sim Q_7$ corresponding to that number and all the other outputs are set low. There is no latch operation in this mode.

When used as an addressable latch and inptus $S_A \sim S_C$ are designated as above, the corresponding latch is selected and the same signal as D appears in the output. When M/C changes from low to high (data inhibit mode), the information from the data input D immediately before the change is latched. When M/C is low, the signal appearing in Q is also changed if the signal D is changed.

In the data input inhibit mode $Q_0 \sim Q_7$ do not change



8-BIT ADDRESSABLE LATCH

even if D is changed and the status before M/C is set high is held

With direct resetting, all the outputs are reset low irrespective of the status of D and $S_A \sim S_C$.

FUNCTION TABLE (Note 1)

Operational mode	R	M/C	D	SA	SB	Sc	Q ₀	Q1	Q2	Q ₃	Q4	Q ₅	Qб	Q ₇
Reset	L	Н	X	X	Х	Х	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L	L	L	L	L	L	L L
	L	L	Н	L	L	L	Н	L	L.	L	L	L	L	L
3-bit binary/octal	L	L	L	Н.	L	L	· L	L	L	L	L	L	L	L L L : : H Q70 Q70 Q70 Q70
decoder/demultiplexer	L	L	Н	Н	L	L	L	Н	L	L	L	L	L	
	i	:	:	:	:	:	:	:	:	÷	:	:	:	:
	L	L	L	Н	Н	Н	L	L	L	L	L	L	L	L
	L	L	Н	н	Н	Н	L	L	L	L	L	L	L	Н
Data input inhibit	Н	Н	Х	Х	Х	Х	Q ₀ 0	Q1 ⁰	Q 2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
	Н	L	L	L	L	L	L	Q ₁ 0	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
	Н	L	Н	L	L	L	н	Q1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
	Н	L	L	н	L	L	Q ₀ 0	L	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
Addressable latch	Н	L	Н	н	L	L	Q ₀ 0	Н	Q ₂ 0	Q ₃ 0	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
	:	:	:	:	:	·	:	:	:	·	:	:	:	:
	Н	L	L	Н	Н	Н	Q ₀ 0	Q1 ⁰	Q 2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	L
	Н	L	Н	н	Н	Н	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	. Q6 ⁰	Н

Note 1 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0:5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃ .
Tstg	Storage temperature range		-65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C	Parameter		Limits			1111	
Symbol	rarameter		Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
	l and land and a second	V _O L≦0.4V	0		4	mA	
IOL	Low-level output current	V _{OL} ≤0.5V	0		8		

Q0: Level of Q before the indicated steady-state input conditions were established.

8-BIT ADDRESSABLE LATCH

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C		_			Limits		
Symbol	Parameter	lest cond	Test conditions		Typ *	Max	Unit
ViH	High-level input voltage			. 2			V
VIL	Low-level input voltage					0.8	V .
Vic	Input clamp voltage	V _{CC} =4.75V.1 _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-400\mu A$		2.7	3.4		٧
VoL	Low-level output voltage	V _{CC} = 4.75 V	I _{OL} = 4mA		0.25	0.4	V
		V ₁ =0.8V, V ₁ =2V	I _{OL} =8mA		0.35	0.5	. V
Іін	High-level input current	$V_{CC} = 5.25V, V_{I} = 2.$	7V			20	μА
чн	Thigh level input current	$V_{CC} = 5.25V \cdot V_{I} = 10$	V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V. V _O =0	V	- 20		- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)		22	36	mA

^{* :} All typical values are at Voc = 5V. Ta = 25°C

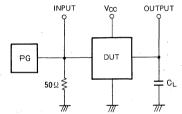
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Зуппоп	rarameter	rest conditions	Min	Тур	Max	UIII
tpHL	High-to-low-level output propagation time, from input R to outputs Q ₀ ~Q ₇			9	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	32	ns
tphL	time, from input D to outputs Q0~Q7	0 45 5		12	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF		15	38	ns
tphL	time, from inputs SA, SB, SC to outputs Q0~Q7			12	29	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			14	35	ns
t _{PHL}	time from input M/C to outputs Q ₀ ~Q ₇			13	24	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

C.:	D	Test conditions		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{su (DH)}	Setup time D high to M/C	·	15	10		ns
t _{h (DH)}	Hold time D high to M/C		5	-5		ns
t _{su (DL)}	Setup time D low to M/C		15	8		ns
th(DL)	Hold time D low to M/C		5	-7		ns
t _{su(s)}	Setup time SA, SB to M/C		15	7		ns
th(s)	Hold time SA, SB, to M/C		5	5		ns
tw(M/C)	M/C input pulse width		15	8		ns
tw(雨)	R input pulse width		15	. 7		ns

Note 4: Measurement circuit

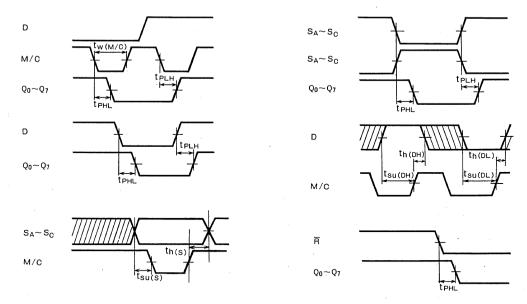


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

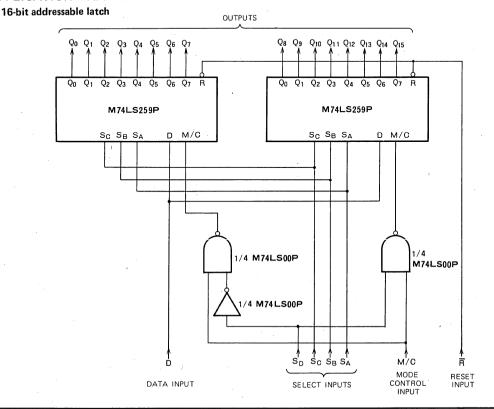
Note 3: ICC is measured with all inputs at 0V.

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE



MITSUBISHI LSTTLS M74LS266P

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS266P is a semiconductor integrated circuit containing four integral open-collector output circuits configured into dual input exclusive NOR gates.

FEATURES

- "wire-AND" capability
- Capable of gating high output voltages $(V_0 \ge 7V)$
- Low power dissipation (Pd = 40mW typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

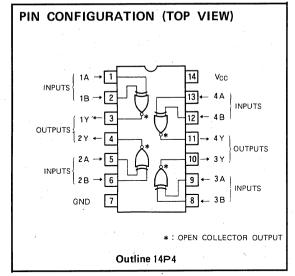
FUNCTIONAL DESCRIPTION

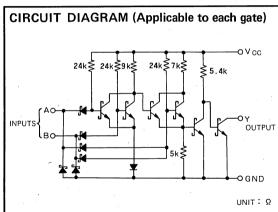
The use of open-collector output circuits in this device gives the user the option of varying high-level output impedance via an external resistance. It is thus possible to implement an AND tie which is not possible in conventional gates.

When both inputs A and B are either high or low-level, output Y goes high-level. Conversely, when A and B are high — low, or low — high with respect to each other, Y will be low-level.

FUNCTION TABLE

Α	В	Υ
L	٦	Н
Н	L	L
L	н	L
Н	н	Н





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		−20 ~ + 75	°C
Tstg	Storage temperature range		− 65 ~ + 150	°C

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet			Limits		Unit
Symbol		ei	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V ₀ =5.5V	0		100	μА
	Low-level output current	V _{OL} ≤ 0.4V	0		4	mA
IOL Low-level output current	loL	V _{OL} ≤0.5V	0		8	mA

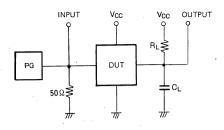
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T	Test conditions		Limits		
Symbol	rarameter	lest con			Typ.*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	· 18mA			-1.5	V
	OH High-level output current	V _{CC} =4.75V, V ₁ =0.8V				100	μА
ЮН		$V_1=2V_1$, $V_0=5.5V_2$	V ₁ =2V. V ₀ =5.5V			100	μΑ.
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	High lovel inc. 4	V _{CC} =5.25V. V _I =2.	7 V			40	μΑ
ΙН	High-level input current	V _{CC} =5.25V, V _I =10	V			0.2	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0 8	mA
Icc	Supply current	V _{CC} =5.25V (Note 1))		8	13	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

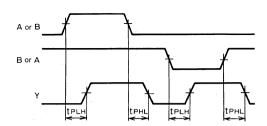
Constant	Parameter				Unit	
Symbol	rarameter			Тур	Max	Onit
tpLH		R _L = 2 kΩ		16	30	ns
tpHL	Low-to-high-level, high-to-low-level output	C _L = 15 pF Other input low-level (Note 2)		16	30	ns
tpLH	propagation time	$R_L = 2 k\Omega$		14	30	ns
· t _{PHL}		$C_L = 15 pF$ Other input high-level (Note 2)		- 14	30	ns

Note 2. Measurement Circuit



- (1) The pulse generator has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, $t_W = 500 \text{ns}, V_P = 3 V_{P,P}, Z_O = 50 \Omega.$ (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C. Note 1. I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS273P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common direct reset and clock inputs.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Direct reset and clock inputs common to all 8 circuits
- Wide operating temperature range (T₂ = -20~+75°C)

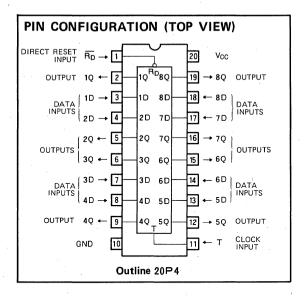
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with direct reset $\overline{R_D}$ input and clock input T common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

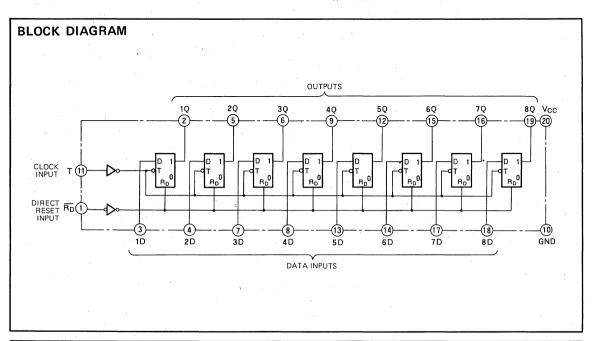
When $\overline{R_D}$ is set low, 1Q through 8Q are all set low irrespective of the status of the ID through 8D and T signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.



FUNCTION TABLE (Note 1)

R _D	T	. D	Q
L	Х	х	L
Н	↑	Н	Н
Н	↑ .	L	L
Н	· L	Х	Q 0

- Note 1 ↑: Transition from low to high (positive edge trigger)
 - Q 0: Level of Q before the indicated steady-state
 - input conditions were established.
 - X : Irrelevant



OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

Combal	Paramet			Limits		Unit
Symbol Parameter		er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0	V	-400	μÀ
1.	Low-level output current	V ₀ ∟≤0.4V	0		4	mA _.
IoL Low-level output current	V ₀ L≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

Symbol	Parameter	Test sand	*****		Limits		Unit
Зуппоот	, a anieter	Test conditions		Min	Typ ∗	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	٧
	/OH High-level output voltage	V _{CC} =4.75V, V _I =0.8V		2.7			
VOH		V _I =2V, I _{OH} =-400	$V_1 = 2V$, $I_{OH} = -400 \mu A$. 3.4	i	V
		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	History and the second	V _{CC} =5.25V, V _I =2.	7V			20	μА
l _{tH}	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
IIL .	Low-level input current	V _{CC} =5.25V, V _I =0.	4 V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-20		- 100	mA
loc	Supply current	V _{CC} =5.25V (Note 3)		17	27	mA

 $[\]boldsymbol{*}$: All typical values are at $V_{CC}\!=\!5V$, $T_{a}\!=\!25^{\circ}\!C$

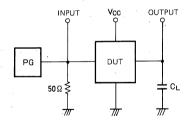
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured after 1D \sim 8D and \overline{R}_D are made 4.5V and T has been changed from 0V to 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Taraffictor .	rest conditions	Min	Тур	Max	Oiiit
f _{max}	Maximum clock frequency		30	40		MHz
t _{PLŲ}	Low-to-high-level, high-to-low-level output propagation			12	27	ns -
tpHL	time, from T to 1Q~8Q	C _L =15pF (Note 4)		13	27	ns
t _{PHL}	High-to-low-level output propagation time, from $\overline{R_D}$ to $1Q{\sim}8Q$			15	27	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .

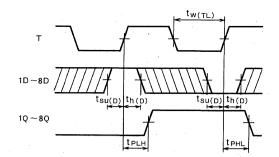
(2) C_L includes probe and jig capacitance.

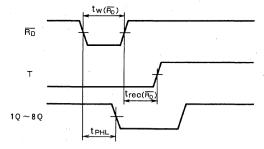
OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS (Vcc=5V, Ta=25°C, unless otherwise noted)

C b l	Symbol Parameter	Test conditions	Limits			Unit
Symbol		rest conditions	Min	Тур	Max	Oint
tw(TL)	Clock input T low pulse width		20	7.		ns
tw (RD)	Direct reset pulse width]	20	6		ns
t _{SU(D)}	Setup time 1D~8D to T		20	7		ns
t _{h(D)}	Hold time 1 D ~ 8 D to T]	5	-3		ns
trec(RD)	Recovery time RD to T	1	25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

QUADRUPLE R-S LATCH

DESCRIPTION

The M74LS279P is a semiconductor integrated circuit containing 4 R-S flip-flop circuits.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- High breakdown output voltage ($V_O \ge 7V$)
- Low power dissipation (P_d = 19mW typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

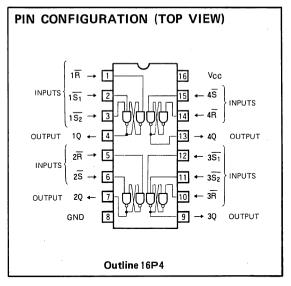
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Two of the 4 circuits have set inputs \overline{S}_1 and \overline{S}_2 and reset input \overline{R} and the other 2 circuits have \overline{S} and \overline{R} inputs.

When $\overline{S_1}$ or $\overline{S_2}$ or both are low or \overline{S} is low, high appears in output Ω , and when R is low, low appears in output Ω . When $\overline{S_1}$ or $\overline{S_2}$ or both are low and \overline{R} is low, high appears in the output but when each of the inputs is set high at the same time, the status of Ω cannot be anticipated.



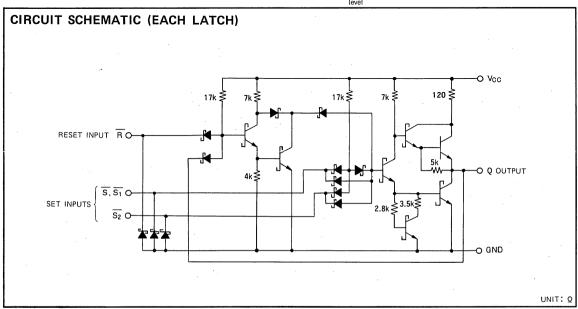
FUNCTION TABLE (Note 1)

. S ₁	S ₂	R	Q
L	Х	L	н*
Х	L	L	Н*
L	Х	Η	Н
Х	L	Н	Ι
Н	н	L	L
н	Н	Н	Q٢

Note 1 $\,\,{\rm Q}^{\,0}$: Level of Q before the indicated steady-state input conditions were established

X: Irrelevant

★: Nonstable, it will not persist when R̄, S̄₁ and S̄₂ return to their inactive (high) level



QUADRUPLE R-S LATCH

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Limits	Unit
Vác	Supply voltage		-0.5~+7	V
٧ı	Input voltage	•	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~ + 75	င
Tstg	Storage temperature range		-65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

	Parameter			Limits .			
Symbol	Parame	ralameter		Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
	Lou Low-level output current	V _{OL} ≤0.4V	0		4	mA	
OL	V _{OL} ≤0.5V		0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75℃, unless otherwise noted)

Combal	Parameter	T			Limits		
Symbol	rarameter	l est condit	Test conditions		Тур *	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{1C} =-1	8mA			-1.5	· V
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		3.4		V ,
VoL	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} =4mA		0.25	0.4	V
		V _{CC} =5.25V V _I =2.7V	1 102			20	μΑ
lih '	High-level input current	V _{CC} =5.25V V _I =10V				0.1	, mA
l _{IL}	Low-level input current	V _{CC} =5.25V V ₁ =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	V _{CC} =5.25V, V _C =0V			— 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			3.8	7	mA

^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

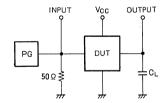
Note 3: ICC is measured with all R inputs at OV and all S inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Symbol Parameter	Test conditions	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	22	ns
t _{PHL}	time, from input S to output Q	C ₁ = 15pF (Note 4)		12	21	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{\mathbf{R}}$ to output \mathbf{Q}	OL TOPI (Note 4)		12	27	ns

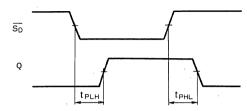
QUADRUPLE R-S LATCH

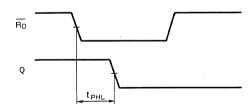
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- (2). C_L includes probe and jig capacitance

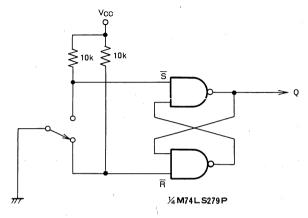
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Chattering prevention circuit



M74LS280P

9-RIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74LS280P is a semiconductor integrated circuit containing a 9-bit parity generator/checker function.

FEATURES

- Easy expansion of bits with cascade connection
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

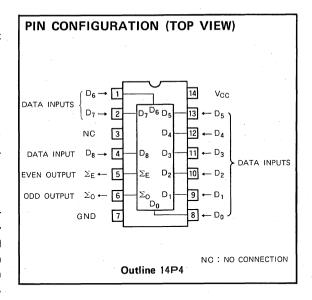
FUNCTIONAL DESCRIPTION

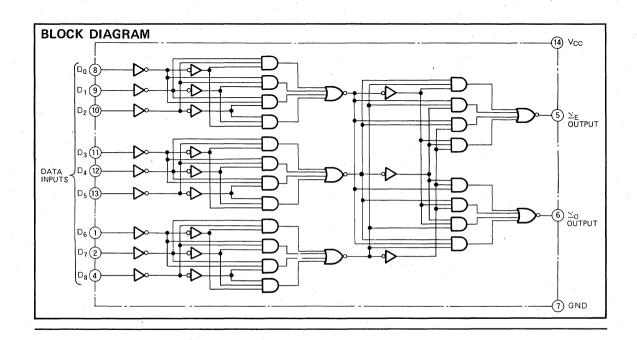
This device is provided with both a 9-bit parity generator and checker functions. For use as a parity generator, parity outputs in even output $\Sigma_{\rm E}$ and odd output $\Sigma_{\rm O}$ are obtained in accordance with the function table, depending on whether the number of high-level data in the inputs is even or odd when 9-bit data are applied to data inputs $D_{\rm O} \sim D_{\rm R}$.

For use as a parity checker, one of the 9-bit data inputs is used for the even or odd parity designation and the remaining 8 bits are used as the data.

FUNCTION TABLE

Number of high-level data in input data.	Σ_{E}	Σ_0
Even number	Н	L
Odd number	L	Н





9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		−0.5 ~ + 15	V
Vo	Output voltage	High-level state	-0.5~Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	ా
Tstg	Storage temperature range		- 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75 ℃, unless otherwise noted)

Symbol	Parameter			Unit		
			Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА
	I OL Low-level output current	V _{OL} ≤0.4V	0		4	mA
1 OL		V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

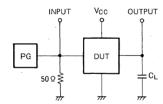
C	Parameter				Limits				
Symbol	rarameter	lest condition	Test conditions		Typ*	Max	Unit		
VIH	High-level input voltage						V		
VIL	Low-level input voltage					0.8	V		
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18	V _{CC} =4.75V, I _{IC} =-18mA			- 1.5	V		
		V _{CC} =4.75V, V _I = 0.8 V	/	2.7 3.4		2.7	2.4		V
Von.	/OH High-level output voltage	$V_1 = 2V$, $I_{OH} = -400 \mu a$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V		
		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V		
VoL	Low-level output	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V		
	High lovel input accept	V _{CC} =5.25V, V _I =2.7V	/			20	μА		
ΊΗ	High-level input current	V _{CC} =5.25V, V _I = 10V				0.1	mA		
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4\	V _{CC} =5.25V, V _I =0.4V			-0.4	mA		
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA		
loc	Supply current	V _{CC} = 5.25V (Note 2)			16	27	mΑ		

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Sumbal	Symbol Parameter	Test conditions		Unit		
Syllidi		rest conditions	Min	Тур	Max	Onit
tpLH	Low-to-high-level, high-to-low-level output propagation			22	50	ns
t _{PHL}	time, from inputs $D_0 \sim D_8$ to output Σ_E	O. — 1505 (Nov. 2)		17	45	ns
tplH	Low-to-high-level, high-to-low-level output propagation time, from inputs $D_0\sim D_8$ to output Σ_0	C _L = 15pF (Note 3)		16	35	ns
t _{PHL}				17	50	ns

Note 3: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_O =50 Ω .

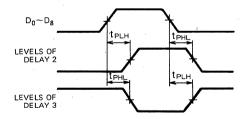
Note 1: All measurements should be done quickly.

Note 2: I_{CC} is measured with all inputs at 0V.

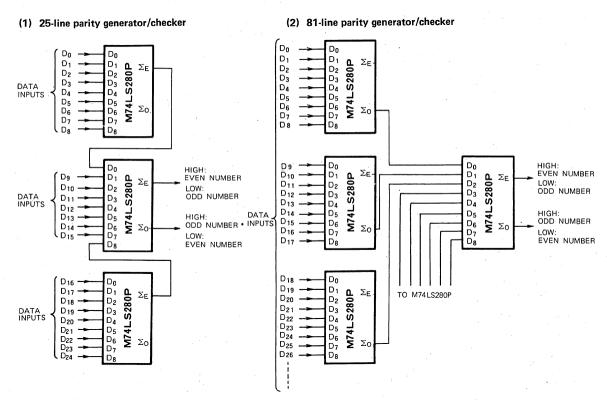
⁽²⁾ C_L includes probe and jig capacitance

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATIONS EXAMPLES



4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS283P is a semiconductor integrated circuit containing a 4-bit full adder function using the look-ahead carry method of operation.

FEATURES

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide operating temperature range (Ta = $-20 \sim +75^{\circ}$ C)

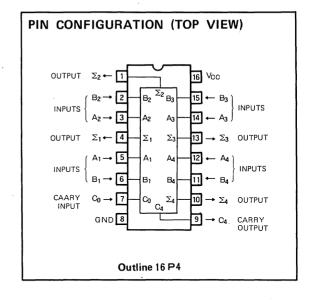
APPLICATION

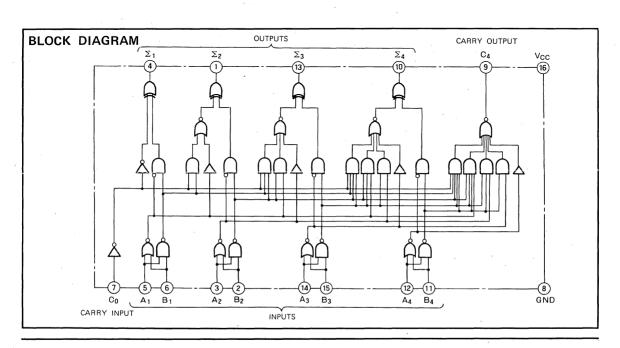
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions as a 2-group, 4-bit binary adder with full adder capability. When a 4-bit binary number is applied to input A_1 thru A_4 or B_1 thru B_4 and a carry signal from the previous column is applied to input C_0 , the sum output for the respective bits will appear at output $\Sigma_1 \sim \Sigma_4$; and carry output to the following column will appear at C_4 .

The full adder capability of this device is also complete with full look-ahead carry operations, and its high speed means that a 4-bit carry output is produced at an average rate of 8ns (typical). Thus, when N-stages are configured for parallel addition of an N-number of 4-bit inputs, a carry output can be obtained with a 8Nns delay time. (See the application example provided in the back of this specification sheet.) Also provided is the M74LS83AP with the same functions and electrical characteristics. This device differs only in its pin configuration.





4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

C _{k-1}	A _k	Bk	$\Sigma_{\mathbf{k}}$	Ck
L	L	L	L	L
L	ŀН	L	Н	L
L	L	н	Н	L
L	Н	н	L	Н
н	L	L	Н	L
Н	Н	L	L	Н
. н	L	Н	L ·	Н
Н	н	н	н	Н.

Note 1. Σ_K and C_K are the sum and carry output calculated in response to input at A_K , B_K , and C_{K-1} (carry input), derived from the following logical equation.

gical equation: $\Sigma_K = A_K \oplus B_K \oplus C_{K,1}$ $C_K = A_K \cdot B_K + (A_K + B_K) \cdot C_{K,1}$ (Where $K = 1 \sim 4$; $\oplus = \text{Exclusive OR}$; + = OR; $\cdot = \text{AND}$)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Complete			Limits			
Symbol	Parameter		Min	Тур	Max 5.25 -400	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА.
		V ₀ L≦0.4V	0		4	mΑ
loL	Low-level output current	V _{OL} ≤0.5V	0	,	8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	· or	Test condi	tions		Limits	ì	Unit
Symbol	T di dililet	,ci	l est condi	tions	Min	Typ *	Max	Offit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V. I _{IC} =-	8mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400\mu A$		2.7	. 3.4		٧
V _{OL}	Low-level output voltage		V _{CC} = 4.75V	I _{OL} =4mA		0.25	0.4	V
VOL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		Co		V 5 05V V 0 7V			20	μΑ
1.	High-level input current	V _{CC} =5.25V, V _I =2.7V				40		
Iн	High-level input current	Co	V _{CC} =5.25V, V _I =10V				0.1	mΑ
		A1~A4, B1~B4					0.2	
1	Low-level input current	Co	1/ 5 051/ 1/ 0 4				-0.4	
lıL	Low-level input current	A1~A4. B1~B4	$V_{CC} = 5.25V, V_1 = 0.4$	v			-0.8	mA
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
			V _{CC} =5.25V, V ₁ = 0	/		22	39	
Icc	Supply current		$V_{CC} = 5.25V$, $V_{I} = 0V$, $V_{I} = 4.5V$ (Note 3)			19	34	, mA
			$V_{CC} = 5.25V, V_1 = 4.$	5V		19	34	

All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

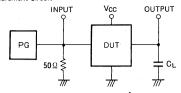
Note 3. I_{CC} is measured with $B_1 \sim B_4$ at OV and with all other inputs 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

C l	Parameter	Test and distance	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	24	ns
t _{PHL}	time, from input C_0 to outputs $\Sigma_1{\sim}\Sigma_4$			13	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	24	ns
t _{PHL}	time, from inputs $A_1 \sim A_4$ or $B_1 \sim B_4$ to outputs $\Sigma_1 \sim \Sigma_4$	C ₁ = 15 pF (Note 4)		11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL - 13 pr (Note 4)		8	17	ns
t _{PHL}	time, from inputs C ₀ to output C ₄			8	22	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	17	ns
tpHL	time, from inputs A ₁ ~A ₄ or B ₁ ~B ₄ to output C ₄			8	17	ns

Note 4 . Measurement Circuit



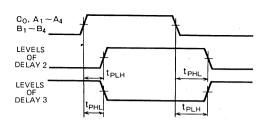
- The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
- (2) C_L includes probe and jig capacitance.

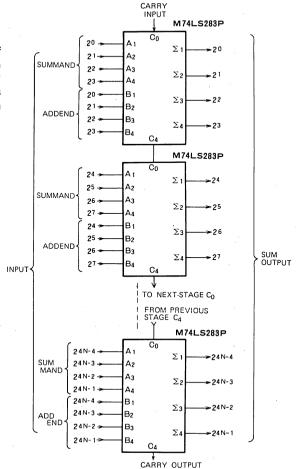
APPLICATION EXAMPLE

The accompanying diagram shows an N-number of M74LS283P devices connected in parallel for addition of an N-number of 4-bit inputs. Typical delay times for carry output in this circuit configuration are listed below. This figures indicates the suitability of this device for use in a high-speed adder employing the ripple-carry method.

N=1 (4 bits) 10.5 ns N=2 (8 bits) 21ns N=3 (12 bits) 31.5 ns N=4 (16 bits) 42ns N=8 (32 bits) 84ns

TIMING DIAGRAM (Reference level = 1.3V)





DECADE COUNTER

DESCRIPTION

The M74LS290P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9-set inputs provided
- Usable independently as binary and divide-by-5 counter
- High-speed counting (f_{max} = 75MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

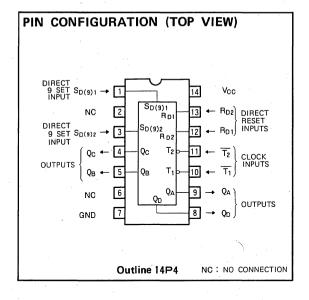
General purpose, for use in industrial and consumer equipment.

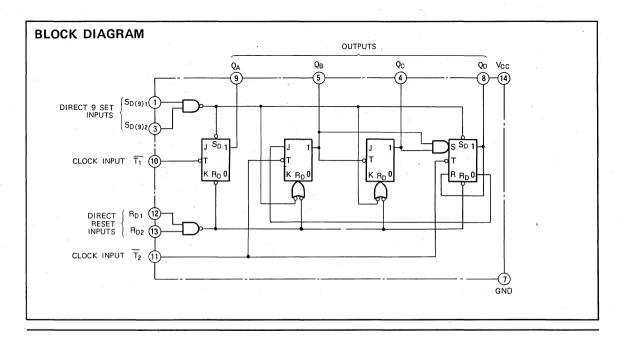
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-5 counters can be reset or set to 9 simultaneously by setting direct reset inputs $R_{D\,1}$ and $R_{D\,2}$ and direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, either $R_{D\,1}$ or $R_{D\,2}$, or both, and $S_{D(9)1}$ or $S_{D(9)2}$, or both, are set low.

Also provided is the M74LS90P with the same functions and electrical characteristics. This device differs only in its pin configuration.





FUNCTION TABLE (Note 1)

T	R _{D1}	RD2	S _{D(9)1}	S _{D(9)2}	QΑ	QB	Qc	QD
×	Н	Н	L	Х	٦	L	L	L
×	Н	Н	Х	L	L	L	L	L
Х	Х	Х	Н	Н	Н	L	L.	Н
↓	L	Х	L	Х		Co	unt .	
1	Х	L.	Х	L		Co	unt	
1	L	Х	Х	L	Count			
1	×	L	L	Х	Count			

Note 1: 1: Transition from high to low

X : Irrelevant

Count number	QA	Qв	Q _C	QD
0	L	L	L	L
1	н	L	L	L
2	L	Н	L	L
3	Н	н	L	L
4	L	L	н	L
5	н	L	н	L
6	L	Н	н	L
7	Н	н	н	L
8.	L	L	L	Н
9	Н	L	L	Н

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless other wise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	V _I Input voltae	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5	J ,,
VI.	Input voltae	Inputs R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	-0.5~+15	7 '
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range	•	-20~+75	င
Tstg	Storage temperature range		−65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, \text{C}$, unless otherwise noted)

				Limits		11-14
Symbol	Parame	eter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	- 5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА
		V _{OL} ≦0.4V	0		4	mA
IOL	Low-level output current	V _{0L} ≦0.5V	0		8	· mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol		Parameter	Test condi			Limits		Unit
Symbol		rarameter	i est condi	lions	Min	Typ *	Max	
VIH	High-level input vo	ltage			2			V
VIL	Low-level input vo	Itage					0.8	V
Vic	Input clamp voltag	e	V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	V
VoH	High-level output v	roltage	$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
Voi Low-level output volta		oltata	V _{CC} =4.75V	I _{OL} =4 mA (Note 2)		0.25	0.4	V
VoL	Low-level output v	Low-level output voltate		I _{OL} =8 mA (Note 2)		0.35	0.5	V
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V _{CC} =5.25V, V _I =2.7V				20	μA mA
		T ₁					40	
	High-level	T ₂					80	
ин	input current	T ₁	V _{CC} =5.25V, V _I =5.5V				0.2	
		T ₂					0.4	
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V _{CC} =5.25V, V _I =10V				0.1	mA
	l and land	R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	,				-0.4	
l _{IL}	input current	Low-level input current T ₁		√			-2.4	mA
		T ₂					-3.2	
los	Short-circuit outpu	it current (Note 3)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
lcc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

* : All typical values are at $V_{CC} = 5 \text{ V}$, $T_a = 25 ^{\circ}\text{C}$.

Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A .

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

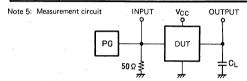
Note 4: I_{CC} is measured with $\overline{T_1}$, $\overline{T_2}$, $S_{D\{9\}1}$ and $S_{D\{9\}2}$ at OV after R_{D1} and R_{D2} have been set to OV after 4.5V.



DECADE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25°C, unless otherwise noted)

0	D	Tank and distance	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	75		MHz
fmax	$\begin{array}{c} \text{Maximum clock frequency,} \\ \text{from input \overline{T}_2 to output Q_B} \end{array}$		16	30		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input $\overline{T_1}$ to output Q_A			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	48	ns
t _{PHL}	time, from input $\overline{T_2}$ to output Q_B			16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	+		7	16	ns
t _{PHL}	time, from input $\overline{T_2}$ to output Q_C			8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O. — 15-5 (Note 5)		15	32	ns
t _{PHL}	time, from input $\overline{T_2}$ to output Q_D	C _L = 15pF (Note 5)		15	. 35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	32	ns
t _{PHL}	time, from input $\overline{T_1}$ to output Q_D			8	35	ns
t _{PHL}	Low-to-high-level output propagation time, from inputs SD(9)1. SD(9)2 to outputs QA, QD	<u>'</u> .		17	40	ns
t _{PLH}	High-to-low-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QB, QC			10	30	ns
t _{PHL}	High-to-low-level output propagation time, from inputs RD1, RD2 to outputs QA, QB, QC, QD			14	40	ns

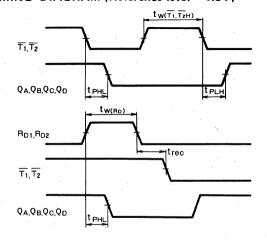


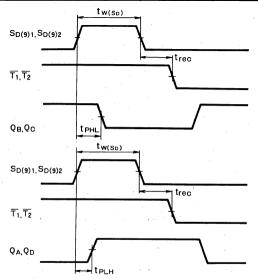
- (1) The pusle generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Tana and distance		Unit		
Зупівої	Farameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width	, .	15	6	٠.	ns
tw(T₂H)	Clock input T ₂ high pulse width		30	17		ns
tw(RD)	Direct reset RD1, RD2 pulse width		15	5		ns
tw(sp)	Direct 9 set SD(9)1, SD(9)2 pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
t _{rec (RD)}	Recovery time RD1, RD2 to T1, T2.		25	8		ns
trec(so)	Recovery time $S_D(9)_1$, $S_D(9)_2$ to \overline{T}_1 , \overline{T}_2		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI LSTTLS M74LS293P

4-BIT BINARY COUNTER

DESCRIPTION

The M74LS293P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexademical) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max} = 60MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

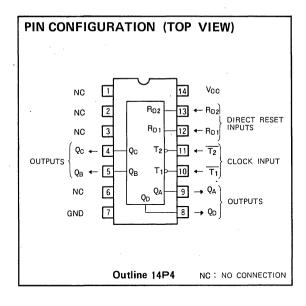
APPLICATION

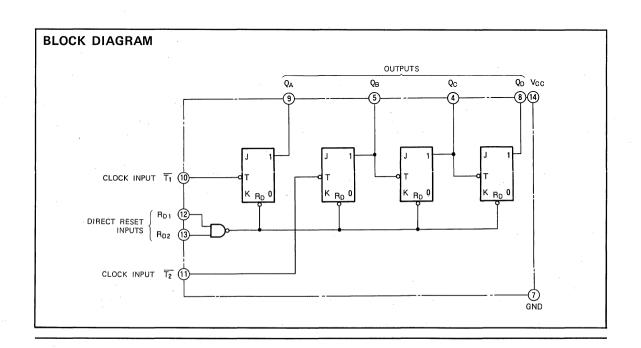
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} and R_{D2} high. For use as a counter, either R_{D1} or R_{D2} , or both, is set low. This pin has the same functions and electrical characteristics as the M74LS93P; only its pin configuration is different.





4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

Ŧ	R _{D1}	R _{D2}	Q_{A}	Q _B	Q _C	Q _D		
X	Н	Н	L	L	L	L		
1	L	Н	Count					
1	Н	L	Count					
1	L	L	Count					

Note 1 | : Transition from high to low

X : Irrelevant

Count number	QΑ	Qв	Qc	QD
0	L	L	L	L
1	Η	L	L ·	L
2	٦	Н	L	L
3	H	Н	L	L
4	L	L	Н	L `
5	H	L,	Н	L
6	L	Н	н	L
. 7	Н.	Н	Н	L
8	L	L	L	Н
9	Н	, L	L	н
10	L	Н	,L	н
11	Н	н	L	Н
12	L,	L	н	н
13	Н	L	H	Н
14	Ĺ	H.	н	н
15	Н	н	Н	н

Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

 $(T_a = -20 \sim +75 \, ^{\circ}\text{C})$, unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	٧	
	Vi Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5	,	
VI	Input voltage	Inputs R _{D1} , R _{D2}	-0.5~+15	1 V	
Vo	Output voltage	High-level state	-0.5~V _{CC}	٧	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

		Parameter			Limits				
Symbol	Paramet	ter	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	٧			
Іон	High-level output current	V _{OH} ≧2.7V	, 0		-400	μА			
		V _{OL} ≦0.4V	. 0		4	mA			
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Paramet		Test condi	itions	Limits			Unit
Symbol	raramet	er	rest contri	itions	Min	Typ *	Max	Onit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	V
Voн	High-level output voltage		$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-400\mu$		2.7	3.4	1	· V
VoL	Low-level output voltage			I _{OL} = 4mA(Note 2) I _{OL} = 8mA(Note 2)		0.25	0.4	V
		R_{D1}, R_{D2} $\overline{T_1}, \overline{T_2}$	V _{CC} =5.25V, V _I =2.7V	<i>,</i>			20 40	μΑ
Іін	High-level input current	$\overline{T_1}$, $\overline{T_2}$ R_{D1} , R_{D2}	$V_{CC}=5.25V, V_{I}=5.5V$ $V_{CC}=5.25V, V_{I}=10V$				0.2	mA
lıL ,	Low-level input current	$ \begin{array}{c} R_{D1}, R_{D2} \\ \hline \overline{T_1} \\ \hline \overline{T_2} \end{array} $	V _{CC} =5.25V, V _I =0.4V	,			-0.4 -2.4 -1.6	· mA
los	Short-circuit output current (N	lote 3)	V _{CC} =5.25V, V _O = 0 V	/	-20		- 100	mA
lcc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.



Note 2: Output Q_A should be tested with input T_2 connected to output Q_A .

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

4-BIT BINARY COUNTER

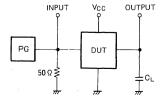
SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	i arameter	rest conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	60		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
tpLH	Low-to-high-level, high-to-low-level output			7	16	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_A			8	18	ns
tpLH	Low-to-high-level, high-to-low-level output	·		28	70	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_D			28	70	ns
tpLH	Low-to-high-level, high-to-low-level output	C. = 1505 (Note 5)		7	16	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_B	C _L =15pF (Note 5)		8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output		:	15	32	ns
t _{PHL}	propagation time, from input T_2 to output Q_C			15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	*		22	51	ns
t _{PHL}	propagation time, from input T ₂ to output Q _D			22	51	ns
t _{PHL}	High-to-low-level output propagation time, from inputs R $_{ m D1}$, R $_{ m D2}$ to outputs Q $_{ m A}$, Q $_{ m B}$, Q $_{ m C}$, Q $_{ m D}$			17	40	ns

TIMING REQUIREMENTS ($v_{CC} = 5 \text{ V}$, $T_a = 25 \text{ C}$, unless otherwise noted)

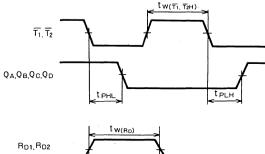
Symbol	Parameter	Test conditions		Unit		
Зупівої	raiametei	rest conditions	Min	Тур	Max] Onit
tw(TiH)	Clock input $\overline{T_1}$ high pulse width		15	6		ns
tw(T₂H)	Clock input T ₂ high pulse width		30	15		ns
tw(RD)	Direct reset RD1, RD2 pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(RD)	Recovery time $R_{D 1}$, $R_{D 2}$ to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

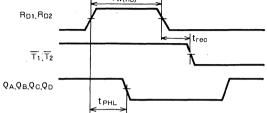
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)





M74LS295BP

4.BIT SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS295BP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input serial/parallel output shift register function.

FEATURES

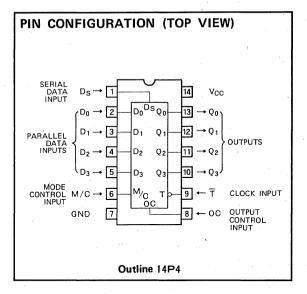
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection.
- Mode control input provided
- Output control input provided
- Usable in AND-Tie connection (3-state output provided)
- Wide operating temperature range (T_a= -20~+75°C)
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)

APPLICATION

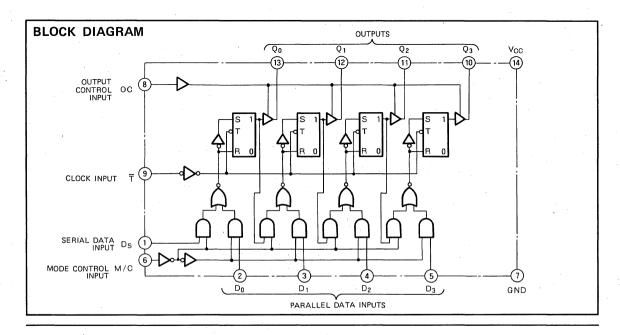
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to serial data input D_S and the clock pulse is applied to clock input \overline{T} , the serial data are shifted into outputs $Q_0 \sim Q_3$ sequentially in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and the 1-bit clock pulse is applied to clock input \overline{T} , the signals $D_0 \sim D_3$ appear in $Q_0 \sim Q_3$ respectively. When \overline{T} changes from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high.



 Q_3 is connected with D_2 , Q_2 with D_1 and Q_1 with D_0 , the serial data are applied to D_3 and the clock pulse applied to \overline{T} , the left shift operation is performed. When low is applied to output control input OC, $Q_0 \sim Q_3$ are put in the high-impedance state and AND-tie connection is enabled. Even when OC is changed, there are no effects on the shift and parallel data reading operations. When a low-level signal is applied to OC with an expansion in the bit number due to the high-impedance state and so shifting is disabled. In cases like this, the M74LS395AP with cascade output Q_3 is recommended.



4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

		Input						Output				
Function mode	M/C	〒			Parallel Data					_		
	IVI / C		Ds	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	
Output hold	Н	Н	Х	×	Х	Х	Х	Q ₀ 0	Q1 ⁰	Q ₂ 0	Q3 ⁰	
Parallel read	Н	1	Х	D ₀	D ₁	D ₂	D ₃	Do	D ₁	D ₂	D ₃	
Left shift	н	↓	Х	Q ₁ +	Q ₂ +	Q ₃ +	D ₃	Q1 ⁰	Q2 ⁰	Q ₃ 0	D ₃	
Output hold	L	Н	Х	Х	Х	Х	×	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q ₃ 0	
Right shift	L	1	н	х	Х	Х	×	н	Q ₀ 0	Q1 ⁰	Q2 ⁰	
night shift	L	1	L	Х	Х	Х	X	L	Ç ₀ 0	Q1 ⁰	Q ₂ 0	

Note 1: † : transition from low to high level (negative edge trigger)

Q0 : level of Q before the indicated steady-state input conditions were established

X : irrelevant

 $Q^{\star}~:~D_0~\text{and}~Q_1$, $D_1~\text{and}~Q_2$, and $D_2~\text{and}~Q_3~\text{are}$ connected externally and serial data are applied to D3

High-impedance state when OC is low.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	င
Tstq	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$), unless otherwise noted)

Symbol	Paramete		Limits				
Symbol	raiamete	, stantes			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	. mA	
		V _{OL} ≤0.4V	0		12	mA	
loL	Low-level output current	V _{0L} ≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted)

Complete	ъ.	-			Limits		
Symbol	Parameter	l est con	Test condotions			Max	Unit
V _{IH}	High-level input voltage						V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	-18mA			- 1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-2.6mA$		3.1	,	V
Vol	Low-level output voltage	$V_{CC}=4.75V$ $V_{I}=0.8V, V_{I}=2V$	I _{OL} = 12mA		0.25	0.4 0.5	V V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =0.	8V, V _O =2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =0.	8V, V _O =0.4V			-20	μА
	High level input ourrent	V _{CC} =5.25V, V _I =2.	V _{CC} =5.25V, V _I =2.7V			20	μА
Ін	High-level input current	V _{CC} =5.25V, V _I = 10)V .			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0	V _{CC} =5.25V, V _O = 0 V			- 130	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)		20	29	mA
Iccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)		22	33	mA

 $\boldsymbol{*}~:~$ All typical values are at VCC=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with $D_0 \sim D_3$ at 0V, D_5 , M/C and 0C at 4.5V after \overline{T} has been set from 3V to 0V.

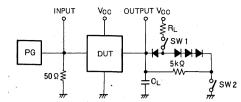
Note 4: I_{OCZ} is measured with $D_0 \sim D_3$, 0C and \overline{T} at 0V and D_S and M/C at 4.5V.

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

0	Description	Test conditions	Limits			Unit
Symbol	Parameter Parame	rest conditions	Min	Тур	Max	Omit
fmax	Maximum clock frequency		30	40		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation	C ₁ = 15pF (Note 5)		15	20	ns
t _{PHL}	time, from input \overline{T} to outputs $Q_0 \sim Q_3$	CL= 15pF (Note 5)		18	30	ns
tpzh	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		14	26	ns
tpzL	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		16	30	ns
tpHZ	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)	1	14	20	ns
tpLZ	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		14	20	ns

Note 5: Measurement circuit



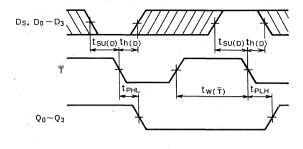
Symbol	SW1	SW2
tрzн	Open	Closed
tpzL	Closed	Open
tpLz	Closed	Closed
t _{PHZ}	Closed	Closed

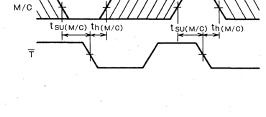
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_o = 50Ω
- (2) All diodes are switching diodes ($t_{rr} \leq 4ns$)
- (3) C_L includes probe and jig capacitance

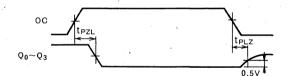
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

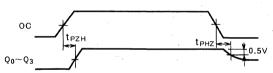
Symbol	Parameter	Test conditions		Limits		
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
tw(T)	Clock input T high pulse width		25	10		· ns
tsu(D)	Setup time D to T	1	20	3		ns
tsu(M/C)	Setup time M/C to T		40	20		ns
th(D)	Hold time D to \overline{T}		20	-1		ns
th(M/C)	M/C hold time to \overline{T}		0	-10		ns

TIMING DIAGRAM (Reference level = 1.3V)









Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.



M74LS298P

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

DESCRIPTION

The M74LS298P is a semiconductor integrated circuit which containing four 2-line to 1-line multiplexers provided with a temporary storage circuit with common selection input and clock input.

FEATURES

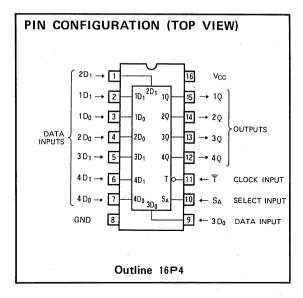
- One line data can be selected from 2-line data.
- Equipped with D-type negative edge-triggered flip-flop.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When the select input S_A is low, data input D_0 is selected, and when it is high, data input D_1 is selected. When the clock input \overline{T} changes from high to low, the selected data appears in the output Q. Since a D-type negative edge-triggered flip-flop is used as a temporary storage circuit, the status of Q does not change even if D is changed, whether \overline{T} is high or low.

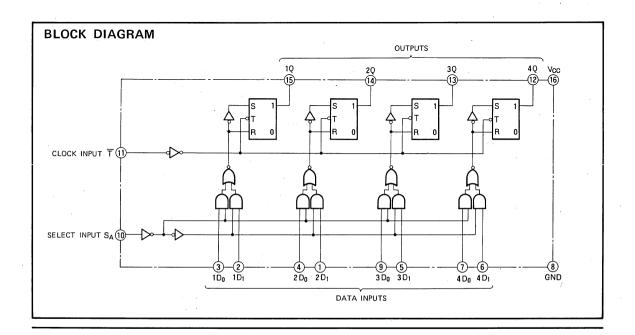


FUNCTION TABLE (Note 1)

Ŧ	. S _A	D ₀	D ₁	Ç
↓	L	L	X	· L .
↓	L	Н	Х	Н
↓	Н	Х	L	L
→	н	Х	н	Н

Note 1: 1: transition from high to low-level

X: irrelevant



OUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Limits					
Symbol	Paramete	Min	Тур	Max	Unit			
Voc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА		
	1 - 1 - 1 - 1 - 1 - 1 - 1	V ₀ L≦0.4V	0		4	mA		
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

C	Parameter	Test cor	ditions		Limits		Unit
Symbol	rarameter	lest cor	iditions	Min	Typ*	Max	Onit
ViH	High-level input voltage			2			٧ .
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	٧
V.	High-level output voltage	V _{CC} =4.75V, V ₁ =0.	.8V .	2.7	3.4		>
VoH	nigh-level output voltage	V _I =2V, I _{OH} =-400/	uΑ	2.7	3.4		٧
V	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V _{OL}	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	High level input august	V _{CC} =5.25V, V _I =2.	7V .			20	μΑ
Ιн	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA .
lı∟	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0:4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-20		- 100	mA
loc	Supply current	V _{CC} =5.25V (Note 3)			13	21	mA .

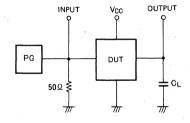
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, runless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	i di di le tei	rest conditions	Min	Тур	Max	Oiiit
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L =15pF		12	27	ns
t _{PHL}	time, from input \overline{T} to outputs $1Q\!\sim\!4Q$	(Note 4)		11	32	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
 - $V_P = 3V_{P.P}, Z_0 = 50\Omega$
- (2) C_L includes probe and jig capacitance.

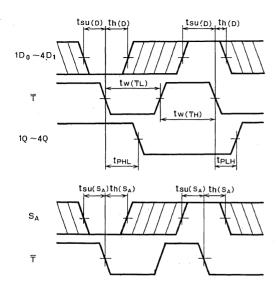
^{3:} I_{CC} is measured with S_A, 1D₀ ~ 4D₁ inputs grounded and a momentary 4.5V, then grounded, applied T input.

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Cumbal	Parameter	Test conditions		Unit		
Symbol	raiameter	rest conditions	Min	Тур	Max	Unit
t _W (〒H)	Clock input T high pulse width		20	7		ns
tw(₹L)	Clock input T low pulse width		20	4		ns
tf	Clock pulse fall time		15	0		ns
t _{SU(D)}	Setup time data input to \overline{T}		15	0		ns
tsu(s _A)	Setup time S_A to \overline{T}		25	5		ns
t _{h(D)}	Hold time data input to ₹		5	0		ns
th(SA)	Hold time SA to T		0	-2		ns

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS299P

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

DESCRIPTION

The M74LS299P is a semiconductor integrated circuit containing an 8-bit serial/parallel input-parallel output shift register function equipped with 3-state outputs and direct reset input.

FEATURES

- Synchronous serial/parallel input-serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Direct reset input
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C_1 and M/C_2 .

(1) Parallel read

M/C₁: High;

M/C₂: High

(2) Right shift

 M/C_1 : High; M/C_2 : Low

(3) Left shift

 M/C_1 : Low; M/C_2 : High

(4) Clock inhibit

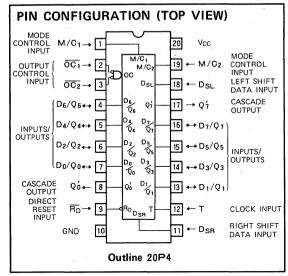
 M/C_1 : Low; M/C_2 : Low

With parallel read, the 8-bit parallel data are applied to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$ and when the clock input T changes from low to high, the data are stored in each of the

respective flip-flops.

With right shift, when the parallel data are applied to the right shift data input DSR, a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With left shift, when the parallel data are applied to the



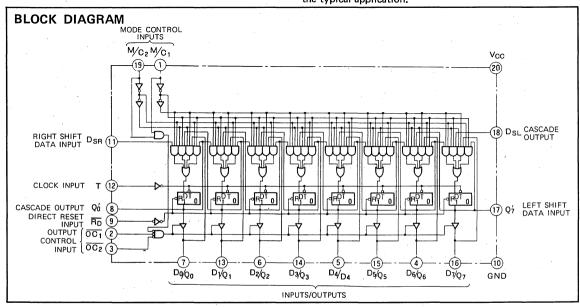
left shift data input D_{SL} , a shift is made one bit at a time from D_7/Q_7 to D_0/Q_0 every time the clock input T changes from low to high.

With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.

When $\overline{R_D}$ is set low, all the flip-flops are set low irrespective of the status of the other inputs.

Cascade outputs O_0' and O_7' are used for expansion of the respective bit numbers. Reference should be made to the typical application.



FUNCTION TABLE (Note 1)

Operational mode	RD	Т	M/C ₁	M/C ₂	DSR	D _{SL}	ŌC₁	OC ₂	D ₀ /Q ₀	D1/Q1	D ₂ /Q ₂	D ₃ /Q ₃	D4/Q4	D ₅ /Q ₅	D ₆ /Q ₆	D ₇ /Q ₇	Qó	Qź
	L	Х	L	Х	Х	Х	L	L	L	L	L	L	L	L	L	L	L	L
Direct reset	L	×	X	L	х	×	L	L	L	L	L	L	L	L	L	L	L	L
District	Н	1	Н	L	L	X	L	L	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q3 ⁰	Q ₄ ⁰	Q ₅ ⁰	Q ₆ ⁰	L	Q ₆ ⁰
Right shift	Н	1	Н	L	Н	X	L	L	Н	Q ₀ ⁰	Q10	Q_2^0	Q3 ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ ⁰	Н	Q ₆ ⁰
	Н	1	L	Н	Х	L	L	L	Q 1 ⁰	Q ₂ ⁰	Q ₃ ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Q ₇ ⁰	L	Q 1 ⁰	L
Left shift	Н	1	L	Н	х	Н	L	L	Q 1 ⁰	Q ₂ ⁰	Q3 ⁰	Q ₄ ⁰	Q4 ⁰	Q ₆ ⁰	Q7 ⁰	н	Q 1 ⁰	Н
Parallel read	Н	1	Н	н	Х	х	L	L	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₇
	н	х	L	L	Х	х	L	L	Q ₀ 0	Q 1 ⁰	Q ₂ ⁰	Q ₃ ⁰	Q4 ⁰	Q ₅ ⁰	Q ₆ ⁰	Q ₇ 0	Q ₀ ⁰	Q7 ⁰
Clock inhibit	н	L	X	х	Х	Х	L	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q ₃ ⁰	Q ₄ ⁰	Q ₅ ⁰	Q ₆ ⁰	Q ₇ ⁰	Q ₀ ⁰	Q7 ⁰
Output inhibit	×	×	×	×	Х	X	Н	L	z	Z	z	Z	Z	Z	z	z	Q ₀ ⁰	Q7 ⁰
(D ₀ /Q ₀ ~D ₇ /Q ₇ are put) in the high-impedance	×	×	×	×	×	×	Ļ	н	z	z	z	z	z	z	Z	z	Q0 ⁰	Q7 ⁰
state	х	х	х	х	X	Х	Н	н	Z	Z	Z.	z	Z	z	Z	Z	Q ₀ ⁰	Q7 ⁰

Note 1. Qn⁰: level of Q before the indicated steady-state input conditions were established

X : Irrelevant

Transition from low to high (positive edge trigger)

Dn: $D_0/Q_0 \sim D_7/Q_7$ function as inputs. Q_0' and Q_1' are set to the same status as D_0 and D_7 , respectively.

Z: High-impedance state. Status of flip-flops before $D_0/Q_0 \sim D_7/Q_7$ were put in the high-impedance mode is held.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
VI	Input voltage			-0.5~+15	V
	0	D ₀ /Q ₀ ~D ₇ /Q ₇	Off-state ·	-0.5~+5.5	V
V ₀	Output voltage	Qó, Qŕ	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient	temperature range		-20~+75	°C
Tstg	Storage temperature range			-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol		Parameter		Limits				
Symbol	·	T diameter			Тур	Max	Unit	
Vcc	Supply voltage			4.75	5	5.25	٧	
1	High-level	$D_0/Q_0 \sim D_7/Q_7$	V _{OH} ≥2.4V	0		-2.6	mA	
тон	OH output current	Qó, Qí	V _{OH} ≧2.7V	0		-400	μ А	
		D ₀ /Q ₀ ~D ₇ /Q ₇	V _{OL} ≤0.4V	0		. 12	mA	
loL	Low-level		$V_{OL} \leq 0.5V$	0		24	mΑ	
IOL	output current		0' 0'	V _{OL} ≦0.4V	0		4	mΑ
•		Q'0, Q'7	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol		Parameter	Test co	nditions		Limits		Unit
SAMPÓI		Faranietei	rest co	inditions	Min	Тур 🛊	Max	Omit
VIH	High-level input volt	age			2			V
VIL	Low-level input volta	age			-	0.8	V	
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	—18mA	-		-1.5	V
V	High-level	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =4.75V	I _{OH} = -2.6mA	2.4	3.1		V
V _{OH}	output voltage Qó, Q7		$V_l=0.8V$, $V_l=2V$	I _{OH} = -400 μA	2.7	3.4		V
		D- /0 D- /0-	\/ A 75\/	I _{OL} =12mA		0.25	0.4	V
	Low-level	$D_0/Q_0 \sim D_7/Q_7$	V _{CC} =4.75V V _I =0.8V	I _{OL} =24mA		0.35	0.5	V
VoL	output voltage	0'.0'	V _I = 0.8 V V _I = 2 V	I _{OL} = 4 mA		0.25	0.4	V
		Qó, Qớ	V = 2 V	I _{OL} = 8 mA		0.35	0.5	. V
lozh	Off-state high-level output current	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =5.25V, V _I =2			40	μΑ	
I _{ozL}	Off-state low-level output current	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =5.25V, V _I =2V, V _O =0.4V				-400	μА
		D ₀ /Q ₀ ~D ₇ /Q ₇ , M/C ₁ , M/C ₂		71/			40	μА
		Onputs other then D ₀ /Q ₀ ~D ₇ /Q ₇ , M/C ₁ , M/C ₂	$V_{CC}=5.25V, V_{I}=2$. / v			20	μΑ
Iн	High-level input current	D ₀ /Q ₀ ~D ₇ /Q ₇		V _I =5.5V			100	μА
		M/C ₁ , M/C ₂	$V_{CC} = 5.25V$				200	μА
		Onputs other then $D_0/Q_0 \sim D_7/Q_7$, M/C_1 , M/C_2		V _I =10V			100	μΑ
1	Low-level	M/C ₁ , M/C ₂	V _{CC} =5.25V				-0.8	mA
I _{IL}	input current	Onput other then M/C ₁ , M/C ₂	V _I =0.4V				-0.4	mA
1.	Short-circuit	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =5.25V		-30		— 130	mA
los	output current	Qó, Q7	$V_0 = 0V$		-20	-	— 100	mA
Icc	Supply current		V _{CC} =5.25V			33	53	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CO}= 5 V, Ta=25°C, unless otherwise noted)

				Unit		
Symbol	Parameter	Test conditions		Тур	Max	Unit
fmax	Maximum clock frequency		25	28		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0 45 5 11 11		20	33	ns
t _{PHL}	time from input T to outputs Qo, Q7	C _L =15 pF (Note 4)		20	39	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to outputs Q_0' , Q_7'			18	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			17	25	ns
t _{PHL}	time, from input T to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	C ₁ = 45 pF (Note 4)		23	39	ns
t _{PHL}	High-to-low-level output propagation time, from inputs $\overline{R_D}$ to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	OL TOPI (Hoto I)		20	40	ns
t _{PZH}	Output enable time to high-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		12	21	ns
t _{PZL}	Output enable time to low-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		15	30	ns
t _{PHZ}	Output disable time from high-level.	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns
t _{PLZ}	Output disable time from low-level	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns

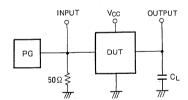
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

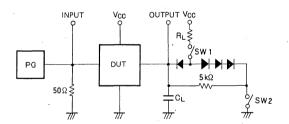
Symbol	Parameter	Test conditions		Unit		
Зуппоот	T arameter	lest conditions	Min	Тур	Max	
tw(TH)	Clock input T high pulse width		20	13		ns
tw(TL)	Clock input Talow pulse width		20	17		ns
tw(RDL)	Direct reset input low pulse width		20	7		ns
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		35	18		ns
tsu(D)	Setup time D _{SR} , D _{SL} , D ₀ /Q ₀ ~D ₇ /Q ₇ to T		20	10		ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T	` .	. 10	-12		ns
th(D)	Hold time D _{SR} , D _{SL} , D ₀ /Q ₀ ~D ₇ /Q ₇ to T	1	0	- 5		ns
trec(RD)	Recovery time RD to T		20	15		ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Iccis measured with inputs T and OC at 4,5V.

Note 4: Measurement circuit





Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t PHZ	Closed	Closed

 $\overline{R_D}$

т

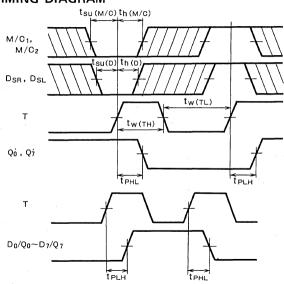
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P=3V_{P-P}, Z_O=50\Omega$
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$

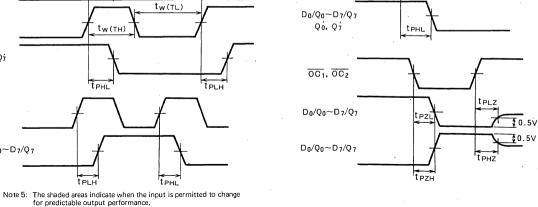
tw(RDL)

trec (RD

(3) C_L includes probe and jig capacitance

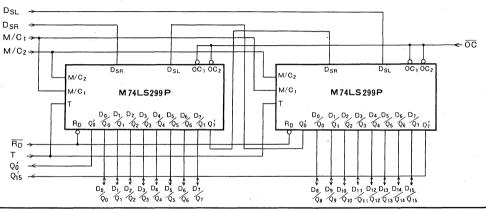
TIMING DIAGRAM





APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS299P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



M74LS323P

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

DESCRIPTION

The M74LS323P is a semiconductor integrated circuit containing an 8-bit serial/parallel input/parallel output shift register function equipped with 3-state outputs and synchronous reset input.

FEATURES

- Synchronous serial/parallel input/serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Synchronous reset input
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C_1 and M/C_2 .

(1) Parallel read

M/C₁: High;

; M/C₂: High

(2) Right shift

 M/C_1 : High; M/C_2 :

(3) Left shift

M/C₁: Low;

M/C2: High

(4) Clock inhibit

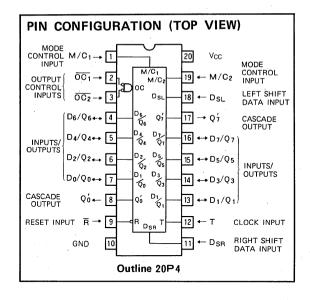
 M/C_1 : Low;

 M/C_2 : Low

Low

With parallel read, the 8-bit parallel data are applied to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$ and when the clock input T changes from low to high, the data are stored in each of the respective flip-flops.

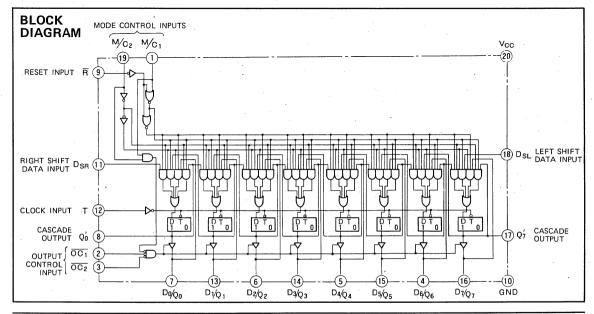
With right shift, when the parallel data are applied to the right shift data input D_{SR} , a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.



With left shift, when the parallel data are applied to the left shift data input D_{SL} , a shift is made one bit at a time from D_0/Ω_0 to D_7/Ω_7 every time the clock input T changes from low to high.

With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.



When \overline{R} is set low if \overline{T} is changed from low to high, all the flip-flops are set low.

Cascade outputs Q'0 and Q'7 are used for expansion of

the respective bit numbers. Reference should be made to the application example.

FUNCTION TABLE (Note 1)

Operational mode	R	, T	M/C ₁	M/C ₂	D _{SR}	D _{SL}	OC ₁	OC2	D ₀ /Q ₀	D ₁ /Q ₁	D ₂ /Q ₂	D ₃ /Q ₃	D4/Q4	D ₅ /Q ₅	D ₆ /Q ₆	D ₇ /Q ₇	Qó	Qí
	L	1	L	х	х	×	L	L	L	L	L	L	L	L	L	L	L	L
Reset	L	Ť	х	L	х	×	L.	L	L	L	L	L	L	L	L	L	L	L
D: 1 . 1://	Н	1	н	L	L	×	L	L	L	Q ₀ 0	Q1 ⁰	Q ₂ ⁰	Q3 ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ 0	L	Q ₆ 0
Right shift	Н	1	Н	L	Н	X	L	L	Н	Q ₀ 0	Q10	Q ₂ ⁰	Q ₃ ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ ⁰	Н	Q ₆ 0
Left shift	Н	1	L	H	Х	L	L	L	Q ₁ ⁰	Q ₂ ⁰	Q ₃ ⁰	Q ₄ ⁰	Q ₅ ⁰	Q ₆ 0	Q7 ⁰	L	Q 1 ⁰	L
Left snift	Н	1	L	Н	Х	Н	L	L	Q ₁ ⁰	Q ₂ ⁰	Q3 ⁰	Q ₄ ⁰	Q ₅ ⁰	Q ₆ ⁰	Q7 ⁰	Q	Q 1 ⁰	Н
Parallel read	Н	1	н	Н	Х	Х	L	L	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₇
Clock inhibit	Н	х	L	L	Х	Х	L	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q ₃ ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Q7 ⁰	Q ₀ ⁰	Q7 ⁰
Clock minibit	Н	L	X	Х	Х	X	L	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q3 ⁰	Q4 ⁰	Q ₅ ⁰	Q ₆ 0	Q ₇ 0	Q_0^0	Q7 ⁰
Output inhibit	Х	X	×	X ·	Х	Х	Н	L	z	Z	Z	Z	Z	Z	Z	z	Q ₀ 0	Q ₇ ⁰
(D0/Q0~D7/Q7 are put) in the high-impedance	X	Χ-	×	Х	Х	×	L	Н	z	z	z	z	z	Z	Z	Z	Q ₀ 0	Q7 ⁰
state	Х	х	X	Х	Х	Х	Н	Н	z	z	Z	z	z	z	Z	z	Q_0^0	Q ₇ 0

Note 1 $\,$ Qn⁰: level of Q before the indicated steady-state input conditions were established

X : Irrelevant

† : transition from low to high (positive edge trigger)

Dn : $D_0/Q_0 \sim D_7/Q_7$ were put in the high-impedance mode is held.

Z : High-impedance state. Status of flip-flops before $D_0/Q_7 \sim D_7/Q_7$ were put in the high-impedance mode is held.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vı	Input voltage			-0.5~+15	V
.,	Output voltage	D ₀ /Q ₀ ~D ₇ /Q ₇	Off-state	-0.5~+5.5	V
V ₀	Output vortage	Qú, Qí	High-level state	-0:5~ V _{CC}	V
Topr	Operating free-air ambier	nt temperature range		-20~+75	℃
Tstg	Storage temperature ran	де		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Constant		Parameter			11.3		
Symbol		rarameter		Min	Тур	Max	Unit
Vcc	Supply voltage			4.75	5	5.25	V
	High-level	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{OH} ≥2.4V	0		-2.6	mA
Гон	output current	Qá Qí	V _{OH} ≧2.7V	0		-400	μА
		D (0 D (0	V _{OL} ≦0.4V	0		12	mA
	Low-level	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{OL} ≤0.5V	0		24	mA
IOL	output current	0' 0'	V _{OL} ≤0.4V	0		4	mA
	Ì	Qó, Qʻ7	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol		Parameter		Test con	ditions		Limits		Unit
Зуппоп		rarannetei		rest con	unions	Min	Typ *	Max	Onit
VIH	High-level input volt	High-level input voltage			2			V	
VIL	Low-level input volt	age						0.8	٧
V _{IC}	Input clamp voltage			V _{CC} =4.75V, I _{IC} =-	– 18mA		-	-1.5	V
VoH	High-level	$D_0/Q_0\sim D$	7/Q7	V _{CC} =4.75V	$I_{OH} = -2.6 \text{mA}$	2.4	3.1		V
VOH	output voltage	Qó, Qí		$V_1 = 0.8V, V_1 = 2V$	$I_{OH} = -400 \mu A$	2.7	3.4		V
		Dn/On~D)- /O-	V _{CC} =4.75V	$I_{OL} = 12 \text{mA}$		0.25	0.4	٧
Vol	Low-level	D0/ Q0 - L		V _I =0.8V	I _{OL} = 24mA		0.35	0.5	٧
VOL	output voltage	Qó, Q7		V ₁ = 0.8V V ₁ = 2 V	I _{OL} = 4 mA		0.25	0.4	٧
		Q0, Q7		V Z V	I _{OL} = 8 mA		0.35	0.5	٧
lozh	Off-state high-level output current D ₀ /Q ₀ ~D ₇ /Q ₇		$V_{CC} = 5.25V, V_{I} = 2V, V_{O} = 2.7V$				40	μΑ	
lozL	Off-state low-level ou	tput current	D ₀ /Q ₀ ~D ₇ /Q ₇	$V_{CC} = 5.25V$, $V_{I} = 2V$, $V_{0} = 0.4V$				-400	μΑ
		$D_0/Q_0\sim D$	₇ /Q ₇ , M/C ₁ , M/C ₂					40	μА
		Input other D ₀ /Q ₀ ~D	then 7/Q7, M / C ₁ , M / C ₂	V _{CC} =5.25V, V _I =2	.7V			20	μΑ
I _{IH}	High-level	D ₀ /Q ₀ ~D	7/Q7		V _I =5.5V			100	μА
	input current	M/C ₁ , M	/C ₂	V _{CC} =5.25V				200	μΑ
		Inputs other	r then 7/Q7, M /C ₁ , M /C ₂		V _I =10V			100	μΑ
1	Low-level	M/G ₁ , M/G ₂		V _{CC} =5.25V				-0.8	mA
TIL	input current	Inputs other	then M/C ₁ , M/C ₂	$V_1 = 0.4V$				-0.4	mA
los	Short-circuit	$D_0/Q_0\sim D$	7/Q7	V _{CC} =5.25V		-30		<u> </u>	mΑ
	output current (Note 1)	Qó, Q7		V ₀ = 0 V		-20		— 100	mA
Icc	Supply current			V _{CC} =5.25V (Note 2)			33	53	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	rarameter	rest conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		25	28		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		20	33	ns
t _{PHL}	time, from input T to outputs Q0, Q7			20	39	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF (Note 4)		17	25	ns
t _{PHL}	time, from input T-to inputs/outputs D ₀ /Q ₀ ~D ₇ /Q ₇ .	· · · · · · · · · · · · · · · · · · ·		23	39	ns .
t _{PZH}	Output enable time to high-level	R _L =665Ω, C _L =45pF (Note 4)		12	21	ns
t _{PZL}	Output enable time to low-level	R _L =665Ω, C _L =45pF (Note 4)		15	30	ns
t _{PHZ}	Output disable time from high-level	$R_L=665\Omega$, $C_L=5$ pF (Note 4)		12	15	ns
t _{PLZ}	Output disable time from low-level	$R_L=665\Omega$, $C_L=5$ pF (Note 4)		12	15	ns

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

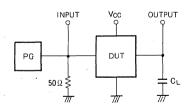
Symbol	Parameter	Test conditions		Limits			
Symbol	ndoi Farameter Test conditions		Min	Тур	Max	Unit	
tw(TH)	Clock input T high pulse width		30	13		ns	
tw(TL)	Clock input T low pulse width		30	17		ns	
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		35	18		ns	
tsu(D)	Setup time D $_{SR},~D_{SL},~D_0/Q_0\!\sim\!D_7/Q_7$ to T		20	10		ns.	
tsu(R)	Setup time R to T		30	23		ns	
th(M/C)	Hold time M/C ₁ , M/C ₂ to T		10	- 12		ns	
th(D)	Hold time DSR, DSL, D0/Q0 \sim D7/Q7 to T		0	– 5		ns	
th(R)	Recovery time R to T		0	- 8		ns	

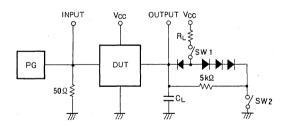
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with inputs T and OC at 4.5V..

Note 4: Measurement circuit

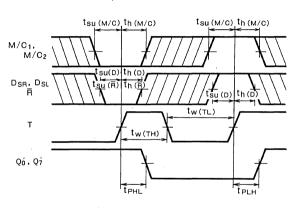


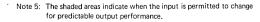


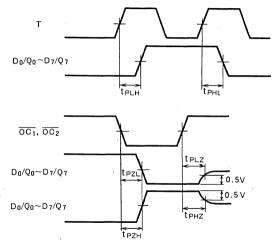
Symbol	SW 1	SW2
t pzH	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) All diodes are switching diodes ($t_{rr} \le 4ns$)
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

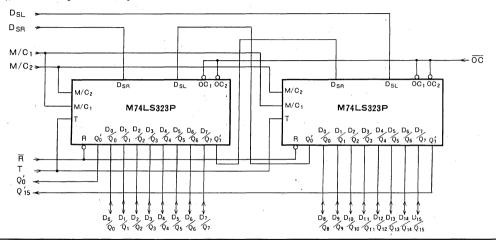






APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS323P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

DESCRIPTION

The M74LS352P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

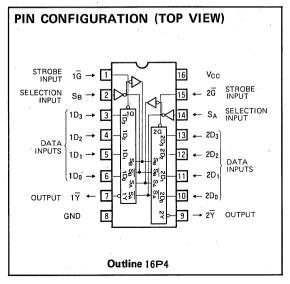
- Inverted outputs provided
- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

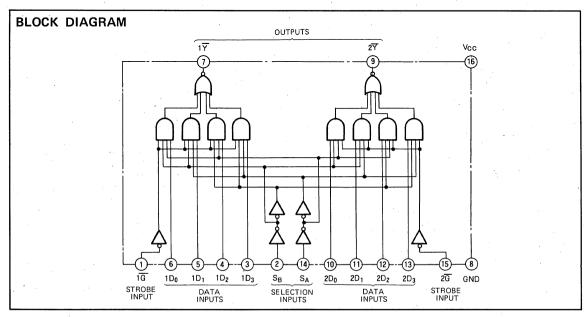
This IC has two data selector circuits which provide 1-line selection of 4 input signals and two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B , the input signal is output at \overline{Y} . By applying 4-bit parallel data to D_0 , D_1 , D_2 and D_3 , and connecting a synchronous divide-by-4 counter output to S_A and S_B , the D_0 , D_1 , D_2 and D_3 data appear in the order of D_0 , D_1 , D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high $1\overline{Y}$ and $2\overline{Y}$ are set high irrespective of the status of the input.



FUNCTION TABLE (Note 1)

S _B	SA	D ₀	D ₁	D ₂	. D3	Ğ	Ÿ
Х	X	×	×	×	×	Н	Н
L	L	L	Х	· ×	×	L	Н
L	L	. H	Х	×	×	L	L
L	н	X	L	×	×	L	Н
L	•н .	×	Н	×	×	L	L
Ι	L	×	X	L	×	L	Н
Н	L	×	×	н	×	L	L
Η	H	×	X	×	, L	L	Н
Н	Н	Х	Х	х	Н	L	L

Note 1 X: Irrelevant



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	. V
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature range	,	-65∼ + 150	ొ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

	•			Limits			
Symbol	Paramet	Parameter		Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Ioh	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
I OL	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = −20~+75°C, unless otherwise noted)

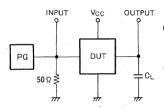
Symbol	Parameter	T	Test conditions		Limits		
Symbol	rarameter	lest condi			Typ *	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA	· .		-1.5	V
1/-	V _{OH} High-level output voltage	V _{CC} =4.75V, V _I =0.8	V _{CC} =4.75V, V _I =0.8V		3.4		
∨он		V _I = 2 V, I _{OH} = -400	$V_1 = 2 V$, $I_{OH} = -400 \mu A$			ŀ	V
VoL	Low-level output voltage	V _{CC} =4.75V	IOL= 4 mA		0.25	0.4	V
VOL		$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V ₁ =2.7	V			20	μА
Ιн	High-level input current	Vcc=5.25V, V _I =10V				0.1	mA
Iμ	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 \	V _{CC} =5.25V, V _O = 0 V			- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			6.2	10	mA ⁻

 $[\]boldsymbol{*}~:~$ All typical values are at VCC=5V, Ta=25°C.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

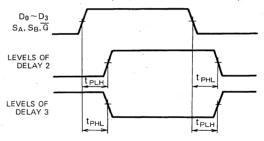
Symbol	Parameter	Test conditions		Unit			
Symbol	1 aranieter	lest conditions		Min	Тур	Max	Oilit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				7	20	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output				7	- 26	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0 = 15-5 (Nov. 4)			9	29	ns
t _{PHL}	time, from inputs S_A , S_B to output \overline{Y}	C _L = 15pF (Note 4)			14	38	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				8	. 24	ns
t _{PHL}	time, from input $\overline{\overline{G}}$ to output $\overline{\overline{Y}}$				13	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .

(2) C_L includes probe and jig capacitance



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Icc is measured with all inputs at 0V.

M74LS353P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS353P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

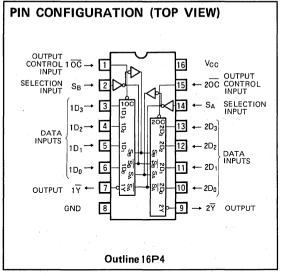
- Inverted outputs provided
- Output control inputs separate for each circuit
- Selection inputs common to both circuits
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signals two multiplexer circuits which convert the 4-bit parallel data into serial data by time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 , and 1 data is specified from among the data input by selection inputs S_A and S_B , the input signal is output at \overline{Y} . By applying 4-bit parallel data to data inputs D_0 , D_1 , D_2 and D_3 and by connecting the output of a synchronous divide-by-four counter to S_A and S_B , data D_0 , D_1 , D_2 and D_3 appear in the order of D_0 , D_1 , D_2 and D_3 , synchronized with the clock pulse. S_A and S_B are common to both circuits while output control inputs $1\overline{OC}$ and $2\overline{OC}$ are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, $1\overline{Y}$ and $2\overline{Y}$ are put in the high-impedance state ("Z") irrespective of the status of the inputs.

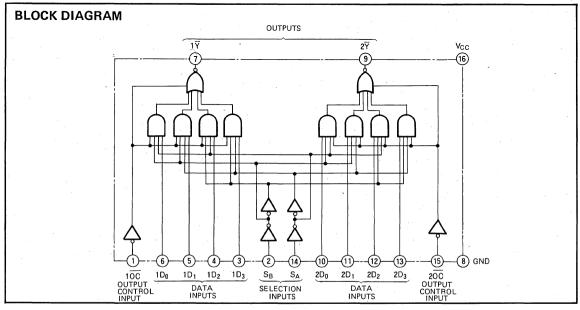


FUNCTION TABLE (Note 1)

S _B	SA	D ₀	D ₁	D ₂	D ₃	оc	Y
Х	×	X	×	×	×	Η	Z
Ľ	L	L.	×	×	×	٦	Н
L	L	Н	×	×	×	L	L
L	н	×	L	×	×	٦	н
L	Н	X	Ι	X	X	L	١
Н	L.	X	×	L	×	L	н
Н	L	Х	X	Н	×	. L	L
Н	Н	. X	X	×	L	L	Н
Н	Н	Х	×	Х	Н	L	L

Note 1 X : Irrelevant

Z: High-impedance state



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		−20~+75	rc
Tstg	Storage temperature range		−65∼+150	r

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Committee 1	Paramet		Limits				
Symbol	raramet	ei	Min	Тур	Max	Unit	
Vcc	Supply voltage	1	4.75	5	5.25	Ý	
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA	
	Low-level output current	V ₀ L≦0.4V	0		4	mA	
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75℃, unless otherwise noted)

Complete	Parameter	Total constitution			Limits		Unit
Symbol	rarameter	lest condition	Test conditions		Typ ∗	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	٧
V _{IC} ·	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	٧
VoH	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-2.6m$	V _{CC} =4.75V, V _I =0.8V V _I =2 V, I _{CU} =-2.6mA		3.1		٧
V _{OL}	Low-level output voltage	V _{CC} =4.75V V ₁ =0.8V, V ₁ = 2 V	I _{OL} = 4 mA		0.25	0.4	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I = 2 V,	1		0.00	20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I = 2 V,	V ₀ =0.4V			-20	μΑ
	High-level input current	V _{CC} =5.25V, V _I =2.7V	,			20	μΑ
Чн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA ·
1 _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
ios	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V	V _{CC} =5.25V, V _O = 0 V			<u> </u>	mA
ICCL	Supply current, all inputs low	V _{CC} =5.25V (Note 3)	V _{CC} =5.25V (Note 3)		7	12	mA
lccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)			8.5	14	mA

^{* :} All typical values are at V_{CC}= 5 V, Ta=25℃

Note 2: All measurements should be done quickly and not more than one output should

be shorted at a time.

Note 3: I_{CCL} is measured with all inputs at $0\dot{V}$. Note 4: I_{CCZ} is measured with $1\overline{0C}$ and $2\overline{0C}$ at 4.5V and all other inputs at 0V.

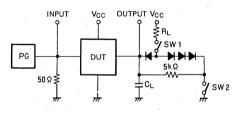
SWITCHING CHARACTERISTICS ($V_{CC}=5~V$, Ta=25%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	i ai airietei	iest conditions		Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	25	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output \overline{Y}	C ₁ = 15pF (Note 5)		6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0E 1361 (11010 5)		14	45	ns
t _{PHL}	time, from inputs S_A , S_B to output \overline{Y}			14	32	ns
t _{PZH}	Output enable time to high-level	$R_L = 2 k\Omega$, $C_L = 15pF$ (Note 5)		14	23	· ns
t _{PZL}	Output enable time to low-level	$R_L = 2 k\Omega$, $C_L = 15pF$ (Note 5)		15	23	ns
t _{PHZ}	Output disable time from high-level	$R_L = 2 k\Omega$, $C_L = 5 pF$ (Note 5)		14	41	ns
t _{PLZ}	Output disable.time from low-level	$R_L = 2 k\Omega$, $C_L = 5 pF$ (Note 5)		9	27	ns

M74LS353P

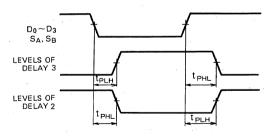
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

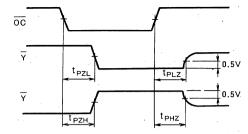
Note 5: Measurement circuit



Symbol	SW1	SW2
tрzн	Open	Closed
tpzL	Closed	Open
tpLZ	Closed	Closed
tphz	Closed	Closed

- The pulse generator (PG) has the following characteristics: $PRR=1MHz,\,t_r=6ns,\,t_r=6ns,\,t_w=500ns,\,V_P=3V_{P,P},\,Z_O=50\Omega.$ All diodes are switching diodes.
- C₁ includes probe and jig capacitance





M74LS365AP

HEX BUS DRIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS365AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

- Provided with output control inputs common to 6 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)
- High breakdown input voltage (V₁ ≥ 15V)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

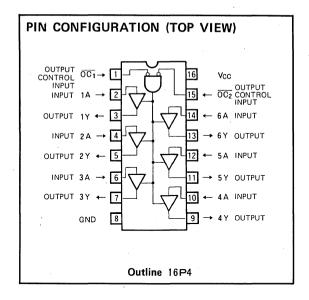
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When $\overline{OC_1}$ and $\overline{OC_2}$ are both low, high appears at the output Y if input A is high and low appears if A is low.

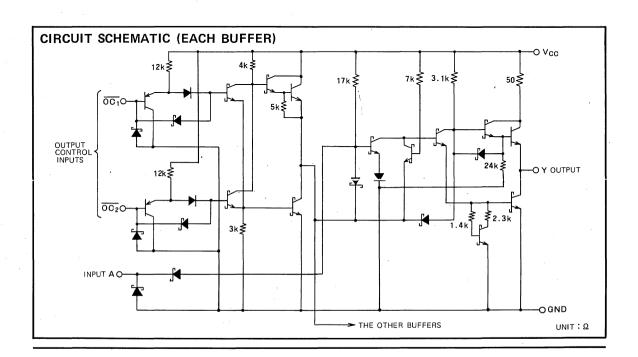
When either $\overline{OC_1}$ or $\overline{OC_2}$ or both are high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.



FUNCTION TABLE (Note 1)

OC ₂	Α	Υ
L	L	L
L	٠н	н
X	Х	Z
Н	Х	Z
	L L X	L L

Note 1: X : irrelevant
Z : high-impedance



HEX BUS DRIVER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		- 65~ + 150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

0	0		Limits		Unit	
Symbol	Parameter		Min	Тур	Max	Oiiit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ
		V _{OL} ≦0.4V	0		12	mA
lor	Low-level output current	V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Tor	st conditions		Limits		Unit
Зуппрог	Tarameter		l es	st conditions	Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC}	=-18mA			-1.5	V
VoH	High-level output voltage		V _{CC} =4.75V, V _I = V _I =2V, I _{OH} =-		2.4	3.1		· V
			V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V	1 _{0L} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_1(\overline{OC}) = 2V, V_0 = 2.4V$				20	μА
lozL	Off-state low-level output current		$V_{CC}=5.25V, V_1(\overline{OC})=2V, V_0=0.4V$				-20	μА
			V _{CC} =5.25V, V _I =	=2.7V			20	μА
Ιн	High-level input current		V _{CC} =5.25V, V _I =	= 10 V			0.1	. mA
		<u>oc</u>	V _{CC} =5.25V, V ₁	= 0.4V		,	-0.4	mA
i Lic	Low-level input current		V _{CC} = 5.25V	$V_1(\overline{OC}) = 0.4V$ $V_1 = 0.4V$			-0.4	. mA
	A	A	VCC=5.25V	$V_1(\overline{OC}) = 2V$ $V_1 = 0.5V$			- 20	μΑ
los	Short circuit output current (Note 2),		V _{CC} =5.25V, V _O =0V		- 40		-225	mA
Icc	Supply current		V _{CC} =5.25V, V _I =	= $0V$, $V_1(\overline{OC}) = 4.5V$		14	24	mA

^{* :} All values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

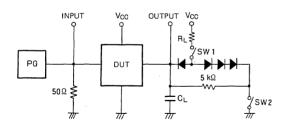
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Cumbal	D		Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =45pF		7	16	ns
t _{PHL} .	propagation time, from input Ato output Y	(Note 3)		10	22	ns
t _{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		13	35	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		15	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	30	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		16	35	ns

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

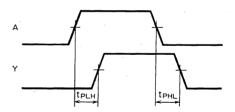
HEX BUS DRIVER WITH 3-STATE OUTPUT

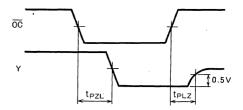
Note 3: Measurement circuit

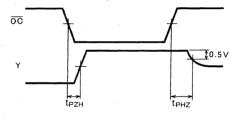


Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t PHZ	Closed	Closed

- \cdot (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P=3V_{P,P},\,Z_O=50\Omega.$
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance







DESCRIPTION

The M74LS366AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

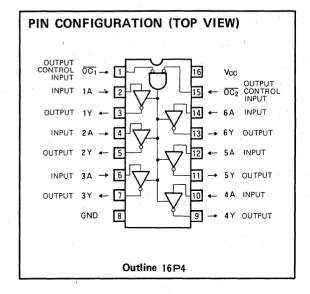
- Provided with output control inputs common to 6 circuits
- High fan-out ($I_{OL} = 24mA$, $I_{OH} = -2.6mA$)
- High breakdown input voltage (V₁ ≥ 15V)
- Wide operating temperature range ($T_a = -20 \sim +75$ °C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

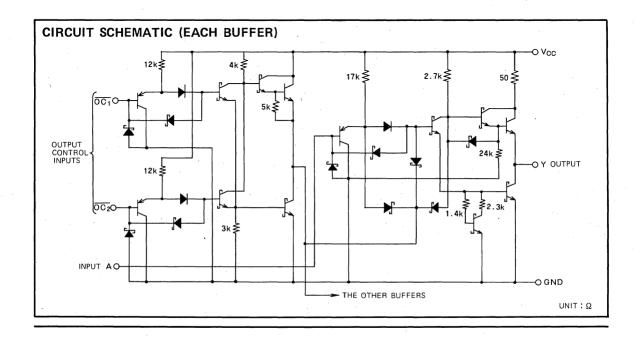
When OC_1 and OC_2 are both low, low appears in the output Y if input A is high and high appears if A is low. When either $\overline{OC_1}$ or $\overline{OC_2}$ both are high, all outputs Y are put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.



FUNCTION TABLE (Note 1)

OC ₁	OC ₂	Α	Y
L	L	L	Н
L	L	н	L
Н	X	X ·	Z
Х	Н	X	Z

Note 1: X: irrelevant Z: high-impedance



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ + 75°C, unless otherwise noted)

Symbol	Parameter			Limits	Unit	
Symbol	rarameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mA
		V _{OL} ≤0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condi	Test conditions		Limits		Unit
37111001	Farameter		l est condi	tions	Min	Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Voн	High-level output voltage		V _{CC} =4.75V, V _I =0.8	3V, I _{OH} =-2.6mA	2.4	3.1		. V
\/-·	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output vortage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA	-	0.35	0.5	V
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_1(\overline{OC}) = 2V, V_0 = 2.4V$				20	μА
lozL	Off-state low-level output current		$V_{CC}=5.25V, V_1(\overline{OC})=2V, V_0=0.4V$				-20	μА
	High Invalidation		V _{CC} =5.25V, V _I =2.7	V			20	μΑ
Ιн	High-level input current	•	V _{CC} =5.25V, V _I =10\	/			0.1	mA
		ōc	V _{CC} =5.25V, V _I =0.4	IV			-0.4	mA
				V _I (OC) =0.4V			-0.4	mΑ
l _{IL}	Low-level input current	A	Vcc=5.25V	V _I = 0.4 V				
			100 2121	$V_1(\overline{OC}) = 2V$		-20	-20	μА
				V _I = 0.5V				
los	Short-circuit output current (Note 2)		$V_{CC}=5.25V, V_{O}=0V$		- 40		225	mA
loc	Supply current		V _{CC} =5.25V, V _I =0V,	$V_1(\overline{OC}) = 4.5V$		12	21	mA

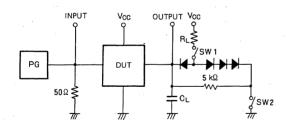
^{* :} All values are at V_{CC}=5V, T_a=25°C

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

	Davis	Total	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		7	15	ns
t _{PHL}	time, from input A to output Y	(Note 3)		7	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		10	35	ns
tezL	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		18	45	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	32	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		14	14	ns

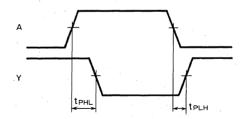
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time,

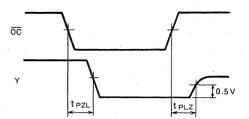
Note 3: Measurement circuit

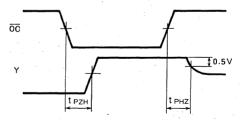


_		
Symbol	SW 1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω .
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.







M74LS367AP

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS367AP is a semiconductor integrated circuit constaining 6 buffers with 3-state output and is provided with output control inputs $1\overline{OC}$ and $2\overline{OC}$, which are common to 4 circuits and 2 circuits, respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits.
- High fan-out
- High breakdown input voltage
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

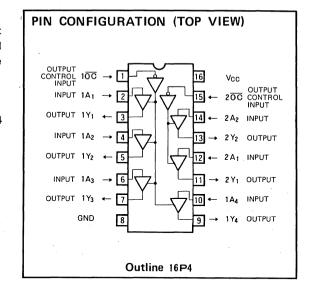
When \overline{OC} is low, high appears in the output Y if input A is high, and low appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

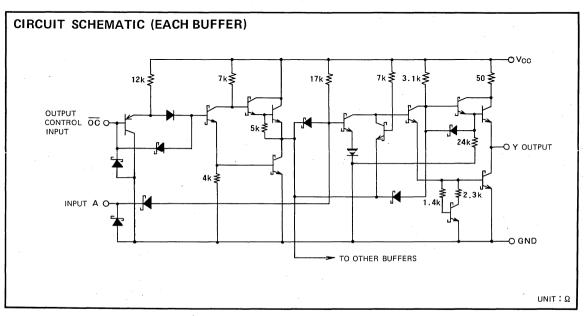
FUNCTION TABLE (Note 1)

ōc	Α	Y
L	L	L
L	н	н
Н	Х	Z

Note 1: X: irrelevant

Z: high-impedance





HEX BUS DRIVERS WITH 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			11-24		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.4V	0	:	-2.6	mA
	Low-level output current	V _{OL} ≤0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal	8		T			Limits	-	Unit
Symbol	Parameter		Test conditions		Min	Тур*	Max	Unit
V _{IH}	High-level input voltage				2			· V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	٧
VoH	High-level output voltage	· .	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-2.6mA		2.4	3.1		٧
.,	Law law law and a colored		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage			$I_{OL}=24 \text{ mA}$		0.35	0.5	. V
lozh	Off-state high-level output current	e high-level output current $V_{CC}=5.25V, V_1(\overline{OC})=2V, V_0=2.4V$				20	μА	
lozL	Off-state low-level output current		$V_{CC}=5.25V, V_1(\overline{OC})=2V, V_0=0.4V$				-20	μА
1	High-level input current			V _{CC} =5.25V, V _I =2.7V			20	μА
Ιιн	night-level input current		V _{CC} =5.25V, V _I =1	0 V			0.1	mA
1		OC	V _{CC} =5.25V, V _I =	0.4V			-0.4	mΑ
· IIL	Low-level input current		V - 5 25V	$V_{1}(\overline{OC}) = 0.4V$ $V_{1} = 0.4V$			-0.4	mA
,		A	V _{CC} =5.25V	$V_{I}(\overline{OC}) = 2V$ $V_{I} = 0.5V$			- 20	μΑ
los	Short-circuit output current		V _{CC} =5.25V, V _O =0V		-40		- 225	mΑ
loc	Supply current		V _{CC} =5.25V, V _I =0	$V, V_1(\overline{OC}) = 4.5V$		14	24	mA

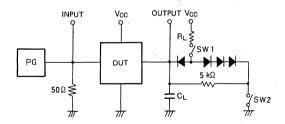
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			11-1-
Зупьот	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation	C _L =45pF		7	16	ns
t _{PHL}	time, from input A to output Y	(Note 3)		10	22	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		- 13	35	ns
tpzL	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		15	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	30	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		16	35	ns

^{* :} All typical values are at V_{CC} = 5V, T_0 = 25°C. Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

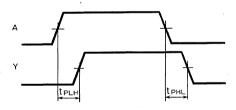
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

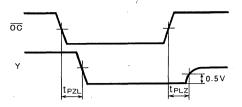
Note 3: Measurement circuit

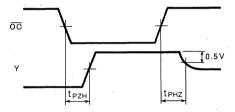


Symbol	SW 1	SW2
tpzh	Open	Closed
t _{PZL}	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.







M74LS368AP

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS368AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $1\overline{OC}$ and $2\overline{OC}$, which are common to 4 circuits and 2 circuits respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits
- High fan-out (I_{O L} = 24mA, I_{O H} = −2.6mA)
- High breakdown input voltage $(V_1 \ge 15V)$
- Wide operating temperature range $(T_a = -20^{\circ} +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

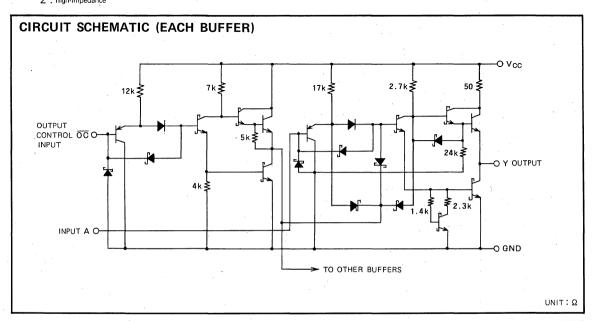
When \overline{OC} is low, low appears in the output Y if input A is high and high appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

ōc	Α	Υ.
L	L	Н
L	Н	L
Н	X	Z

Note 1: X: irrelevant
Z: high-impedance

PIN CONFIGURATION (TOP VIEW) OUTPUT CONTROL 100 INPUT OUTPUT INPUT 1A1 OUTPUT 1Y1 INPUT OUTPUT INPLIT 1A 2A. INPLIT OUTPUT 1Y2 INPUT 1A₃ 2Y1 OUTPUT OUTPUT 1Y2 INPUT GND 1Y4 OUTPUT Outline 16P4



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75 _.	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	nbol Parameter					
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mΑ
	Low level output augrent	V _{OL} ≦0.4V	0		12	mA
loL	Low-level output current	V _{0L} ≤0.5V	0	٠.	24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter		Test condit			Limits		Unit
Symbol	Parameter		rest condit	lest conditions		Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Voн	High-level output voltage		V _{CC} =4.75V, V ₁ =0.8	3V, I _{OH} = -2.6mA	2.4	3.1		V
			V _{CC} =4.75V	I _{OL} = 12 mA		0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I (OC)	$V_{CC} = 5.25V, V_1(\overline{OC}) = 2V, V_0 = 2.4V$			20	μА
lozL	Off-state low-level output current		$V_{CC} = 5.25V, V_1(\overline{OC}) = 2V, V_0 = 0.4V$				-20	μА
	Not be all the second		V _{CC} =5.25V, V _I =2.7V				20	μА
liH	High-level input current		V _{CC} =5.25V, V _I =10\	/			0.1	mA
		<u>oc</u>	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
				$V_1(\overline{OC}) = 0.4V$				
LIL	Low-level input current	١.		V _I =0.4V			-0.4	mΑ
		A	A V _{CC} =5.25V	$V_1(\overline{OC}) = 2 V$				
				V _I =0.5V		1	-20	μΑ
los	Short-circuit output current (Note 2)	-	V _{CC} =5.25V, V _O =0V		-40		- 225	mA
Icc	Supply current		V _{CC} =5.25V, V _I =0V,	$V_1(\overline{OC}) = 4.5V$		12	21	mA

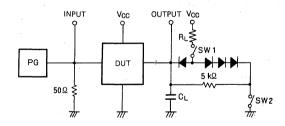
^{*} : All values are at $V_{CC}\!=\!5V$, $\,T_{a}\!=\!25^{\circ}\!C$, unless otherwise noted

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

		Total and distant	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high level, high-to-low-level output propagation	C _L =45pF		. 7	15	ns
t _{PHL}	time, from input A to output Y	(Note 3)		7	18	ns
t _{PZH}	Output enable time to high-level	$R_{\perp}=667\Omega$, $C_{\perp}=45pF$ (Note 3)		16	35 .	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		18	45	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		13	32	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		18	35	ns

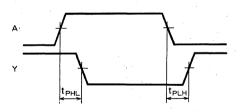
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

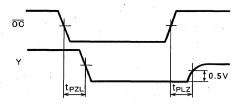
Note 3: Measurement circuit

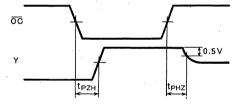


Symbol	SW 1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.







M74LS373P

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS373P is a semiconductor integrated circuit containing 8 D-type latch circuits with 3-state output and is provided with an output controlling input and an enable input common to all circuits.

FEATURES

- 3-state, high fan-out output
- Since pnp transistor input is used in output control and enable inputs, the input load factor is small
- The enable input has high noise margin (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and enable inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

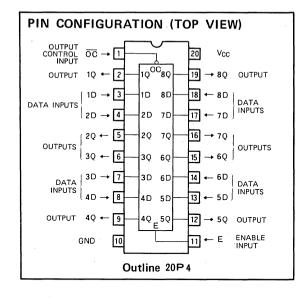
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Since the 8 D-type latches use pnp transistor input for the output control input \overline{OC} and enable input E, which are common to all 8 circuits, the input load factor is small. With a hysteretis of 400mV (typical) specially given to the input circuit E, noise margin is high.

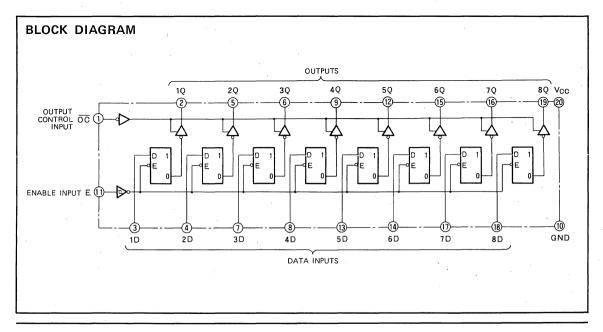
When E is high, the information from the data input D appears in the output \mathbf{Q} .

When the D signal changes, the signal that appears in Q also changes. When E changes from high to low, the status of D



immediately before the change is latched. While E is low, the status of Q does not change even if the D is changed. When \overline{OC} is high, 1Q-8Q are all put in the high-impedance state irrespective of other input signals. Since all

impedance state irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver. For application, see M74LS374P.



M74LS373P

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

ōc	E	D	Q
L	н	Н	Н
L	н	L	L
L	L	X	Q ⁰
Н	Х	X	Z

Note 1: Q0: level of Q before the indicated steady-state input conditions were established

Z : high-impedance

X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		$-0.5 \sim +7$	٧
Vı	Input voltage		-0.5~+15	٧
Vo	Output voltage	Off-state	-0.5~+7	٧
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃ .
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Unit		
Symbol			Min	Тур	Max	01111
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mĄ
		V _{OL} ≦0.4V	- 0		12	mA
lor	Low-level output current V _{OL} ≤0.5V		0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Combal	Parameter					Limits	1	Unit
Symbol			Test condi-	tions	Min	Typ*	Max	
VIH	High-level input voltage			·	2			٧
	1 1 :	Ε .	·			,	0.75	V
VIL	Low-level input voltage D, O	D, OC		7			0.8	
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-2.6m		2.4	3.1		٧
			V _{CC} =4.75V	I _{OL} =12 mA		0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24 mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =2V,	$V_0 = 2.7V$			20	. μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =2V,	V ₀ =0.4V			-20	μА
L	High level input gurrent		V _{CC} =5.25V, V _I =2.7	V			20	μА
ин .	High-level input current		V _{CC} =5.25V, V _I =10V				0.1	mA
IIL	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		- 30		-130	mA
locz	Supply current, all outputs off		V _{CC} =5.25V (Note 3)			24	40	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

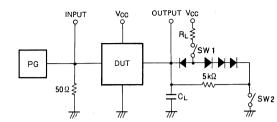
^{3:} I_{CCZ} is measured with \overline{OC} input at 4.5V.

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зуппьот		rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	18	ns
t _{PHL}	time, from input 1D~8D to output 1Q~8Q	C ₁ = 45 pF (Note 4)		11	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL-43 pr (Note 4)		14	30	ns
t _{PHL}	time, from input E to output 1Q~8Q			13	30	ns
t _{PZH}	Output enable time to high-level	R _L =667 Ω, C _L =45 pF (Note 4)		13	28	ns
t _{PZL}	Output enable time to low-level	$R_L=667 \Omega$, $C_L=45 pF$ (Note 4)		14	36	ns
t _{PHZ}	Output disable time from high-level	R _L =667 Ω, C _L = 5pF (Note 4)		16	20	ns
t _{PLZ}	Output disable time from low-level	R _L =667 Ω, C _L = 5pF (Note 4)		8	25	ns

Note 4: Measurme Measurement circuit

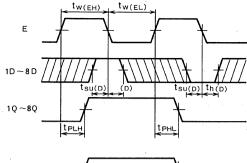


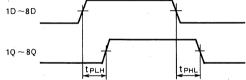
Symbol	SW 1	SW2
t PZH	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t PHZ	Closed	Closed

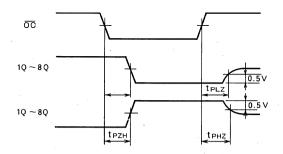
- (1) The pulse generator (PG) has the following characteristics:
- PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P,P}$, $Z_O = 50Ω$ (2) All diodes are switching diodes ($t_{ff} \le 4ns$)
- (3) C₁ includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C unless otherwise noted)

Combal		Test conditions	Limits			Unit
Symbol Parameter	rarameter	rest conditions	Min	Тур	Max	Onit
tw (EH)	Enable input E high pulse width		15	11		ns
tw (EL)	Enable input E low pulse width		15	10		ns
tsu	Setup time 1D~8D to E		5	-2		ns
th	Hold time 1D∼8D to E		20	7		ns







Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS374P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS374P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flipflop circuits with 3-state output, and is provided with an output control input and a clock input, which are common to all the circuits.

FEATURES

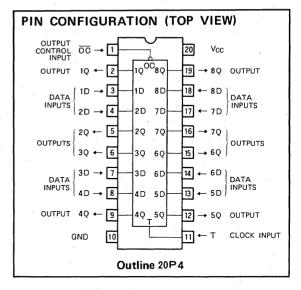
- Positive edge triggering
- 3-state high fan-out output
- The use of pnp transistor input for the output control and clock inputs has made the input load factor small
- The clock input has high noise margin.
 (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and clock inputs which are common to all 8 circuits.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

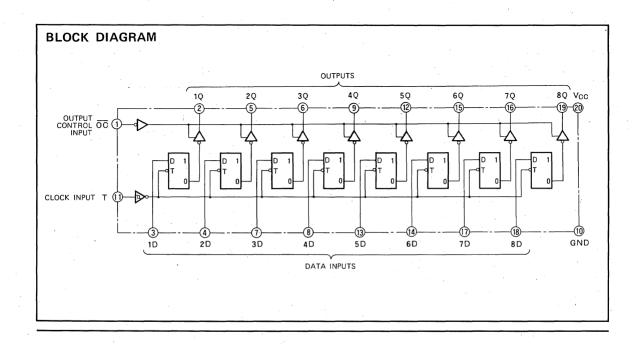
FUNCTIONAL DESCRIPTION

Since the 8 D-type ege-triggered flip-flop circuits use a pnp transistor input for the output control input \overline{OC} and clock input T, which are common to all 8 circuits, the input load factor is small. With a hysterisis of 400mV (typical) specially given to the input circuit T, noise margin is high.



When T changes from low to high, the information of data input D immediately before the change appears in the output O in accordance with the function table.

When \overline{OC} is high, 1Q - 8Q are all put into the high-inpedance state, irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register. I/O port, or bi-directional bus driver.



OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

ŌĊ	Т	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	O ₀
Н	X	Х	Z

Note 1: ↑: transition from low to high level

O⁰: level of Q before the indicated steady-state input conditions were established

Z: high-impedance

X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage	·	-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Sumbal	ymbol Parameter					
Syllibol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	. 0		-2.6	mA
la.	Low-level output current	V _{OL} ≤0.4V	0		12	mA
loL ·	V _{OL} ≤0.5V		0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Took cond	litiana	Limits			Unit
Symbol		rest cond	Test conditions		Typ*	Max	
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
	High-level output voltage	$V_{CC} = 4.75V, V_1 = 0.$	8V	2.4	2 1		
V _{OH}	nigh-level output voltage	V _I =2V, I _{OH} =-2.6 m	V _I =2V, I _{OH} =-2.6 mA		3.1		V
\/-	Law level output veltere	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24 mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V	, V ₀ =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V	, V ₀ =0.4V			-20	μА
1	High-level input current	V _{CC} =5.25V, V _I =2.7	1 V			20	μА
Ιн	Figh-level input current	V _{CC} =5.25V, V _I =10V	/			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-30		- 130	mĄ
locz	Supply current, all outputs off	V _{CC} =5.25V (Note 3)			27	45	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

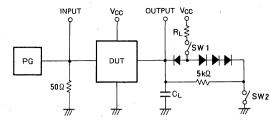
^{3:} I_{CCZ} is measured with OC input at 4.5V.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	—	Limits			11.24
Symbol		Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF (Note 4)		10	28	ns
t _{PHL}	time, from input T to output 1Q~8Q			13	28	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 4)		14	28	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 4)		14	28	ns
t _{PHZ}	Output disable time from high-level	R _L =667Ω, C _L = 5pF (Note 4)		16	20	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 4)		8	25	ns

Note 4: Measurement circuit

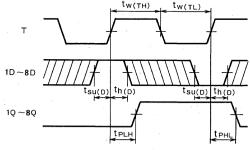


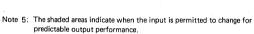
Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

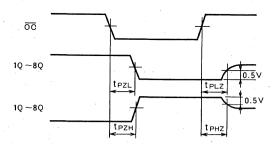
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{P.P.}$, $Z_0 = 50\Omega$ (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Oiiit
tw(TH)	Clock input T high pulse width	- 1	15	. 5		ns
t _{W(TL)}	Clock input T low pulse width		18	15		ns
· t _{SU(D)}	Setup time 1D~8D to T		20	6		ns
t _{h(D)}	Hold time 1D ~ 8D to T		- 4	1		ns





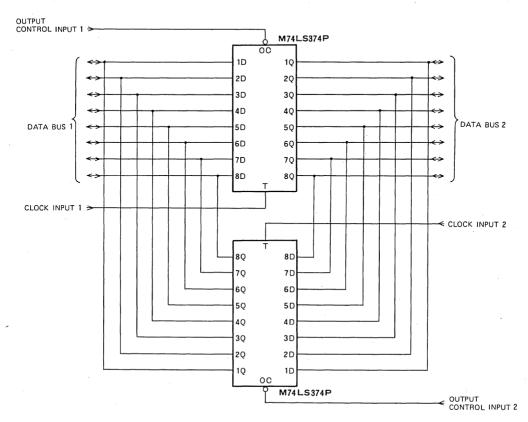


OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS

WITH 3-STATE OUTPUTS

APPLICATION EXAMPLE

8-Bit shift register



4.RIT RISTABLE LATCH

DESCRIPTION

The M74LS375P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Ω and $\overline{\Omega}$.

FEATURES

- Enable inputs common to two circuits each
- Q and Q outputs
- pin 8 GND, pin 16 Vcc.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{\mathbf{Q}}$. When the D signal changes, the signal that appears in outputs Q and $\overline{\mathbf{Q}}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{\mathbf{Q}}$ does not change even if D is changed.

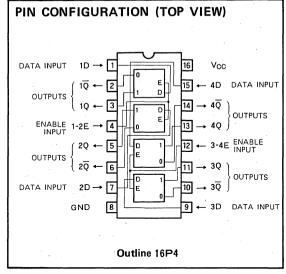
This IC has the same functions and electrical characteristics as M74LS75P and differs only in its pin configuration.

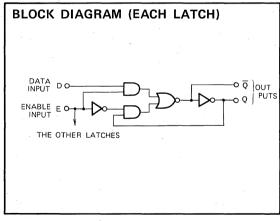
FUNCTION TABLE (Note 1)

E.	D	Q	Q
Н	H.	Н	L
H	L	L	Н
L	X	Q0	Q ⁰

Note 1 $Q^0, \overline{Q^0}$: Level of Q and \overline{Q} before the indicated steady-state input conditions were established.

X : Irrelevant





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter '	Condition	ons	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vι	Input voltage			-0.5~+15	V
V ₀	Output voltage	High-level state		-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range			-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C



4-BIT BISTABLE LATCH

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Limits			
Syllibol	Vcc Supply voltage	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА	
la.	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
loL	Fow-level outbut confent	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

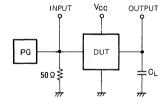
Symbol	Parameter		Test conditions			Limits		Unit
Symbol	rarameter		rest conditions		Min	Тур *	Max	Unit
VIH	High-level input voltage'				2			V
VIL	Low-level input voltage						0.8	V
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18m/	Α			-1.5	V
VoH	High-level output voltage $ \begin{array}{c} V_{CC}{=}4.75\text{V, } V_{I}{=}0.8\text{V} \\ V_{I}{=}2\text{V, } I_{OH}{=}-400\mu\text{A} \end{array} $		2.7	3.5		V		
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output voltage		$V_{l} = 0.8V, V_{l} = 2V$	IoL=8mA		0.35	0.5	V
		D	V _{CC} =5.25V				20	
1	High level in the summer	E	V _I = 2.7V				80	μΑ
Чн	High-level input current	D	V _{CC} =5.25V				0.1	^
		E	$V_{I} = 10V$				0.4	mA
	Low-level input current	D	V _{CC} =5.25V				-0.4	^
I⊫ .	Low-level input current	E	V _I = 0.4V				-1.6	mA .
los	Short-circuit output current (No	ote 2)	V _{CC} =5.25V, V _O = 0 V		-20		- 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			6.3	12	mA

^{* :} All typical values are at V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
- Cynnson	- Tarameter	rest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation	•		12	27	ns
t _{PHL}	time, from input D to output Q			8	17	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	0. 45.5 (May 4)		10	20	ns
t _{PHL}	time, from input D to output $\overline{ extstyle Q}$			6	15	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		13	2,7	ns
t _{PHL}	time, from input E to output Q			12	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	30	ns
t _{PHL}	time, from input E to output Q	,		6	15	ns

Note 4: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics:

PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

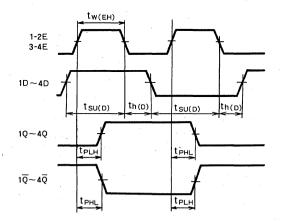
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

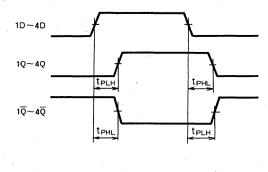
Note 3: ICC is measured with all inputs at OV.

4-BIT BISTABLE LATCH

TIMING REQUIREMENTS (VCC=5V, Ta=25°C, unless otherwise noted)

Constant		Test conditions	Limits			Unit
Symbol Parameter	lest conditions	Min	Тур	Max	Unit	
tw(EH)	Enable input E high pulse width		20	7		ns
tsu(D)	Setup time 1D ~ 4D to E		20	12		ns
th(D)	Hold time 1D ~ 4D to E		8	- 5		ns





High-level 3-4E, 1-2E

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

DESCRIPTION

The M74LS377P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common clock input and enable input.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Enable and clock inputs common to all 8 circuits
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

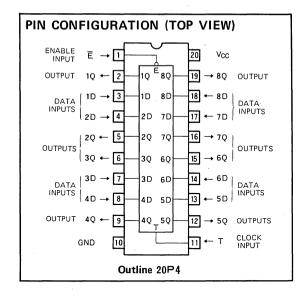
APPLICATION

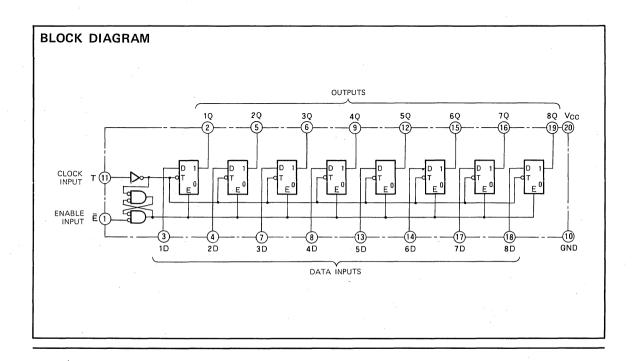
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with clock input T and enable input \overline{E} common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

When \overline{E} is set high, the output status does not change irrespective of the status of the other input signals. Malfunctioning does not result even if \overline{E} is set from high to low or from low to high.





OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

FUNCTION TABLE (Note 1)

		_	
Ē	Т	D	Q
Н	Х	Х	Q ⁰
L	1	Н	. Н
L	1	L	L
X	L	Х	O ₀

Note 1 ↑: Transition form low to high (positive edge trigger)

Q0: Level of Q before the indicated steady-state input conditions were established.

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage	·	-0.5~+15	٧
V ₀	Output voltage	High-level state	-0.5~V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	. ℃
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	raraniete	•	Min.	Тур	Max 5.25 — 400	Unit	
V _{CC}	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≧2.7V	0		-400	μА	
		V _{OL} ≦0.4V	0		4	mA	
lor	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D	T	tat		Limits		Unit
Symbol	Parameter	Test cond	itions	Min	Typ *	Max	
Viн	High-level input voltage			2			>
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
	Mish level output voltage	V _{CC} =4.75V, V _I =0.	8V	2.7	2.4		V
V _{OH}	High-level output voltage	V _I =2V, I _{OH} =-400,	ıΑ	2.7	3.4		
\/-·	I am la mana a mana a	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧
	History and in the second	V _{CC} =5.25V, V _I =2.	7 V			20	μА
• Тін	High-level input current	V _{CC} =5.25V, V _I =10	V .			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4	4V			-0.4	· mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-20		-100	mΑ
loc	Supply current	V _{CC} =5.25V (Note 3)			17	28	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

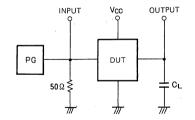
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	raianglei	Test conditions -	Min	Тур	Max	Oilit
f _{max}	Maximum clock frequency		30	40		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		11	27	ns
tphL	time, from T to $1Q \sim 8Q$			11	27	ns

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current is measured after 1D \sim 8D are set to 0V and T has been changed from 0V to 4.5V.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

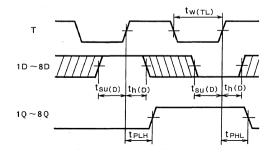
Note 4: Measurement circuit

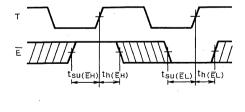


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f^r = 6ns, t_f = 6ns, t_W = 500ns. V_P = 3 $V_{P,P}$, Z_Q = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Constant	Description	Task and dising		Unit		
Symbol	Parameter .	Test conditions	Min	Тур	Max	Unit
tw(TL)	Clock input T low pulse width		20	8		ns
t _{SU(D)}	Setup time 1D∼8D to T		20	6		ns
t _{SU(ĒH)}	Setup time high E to T		10	0		ns
t _{SU(ĒL)}	Setup time low E to T		25	9		ns
t _{h (D)}	Hold time 1D∼8D to T		5	- 5		· ns
th (EH)	Hold time high $\overline{\mathbb{E}}$ to T		5	- 5		ns
th (EL)	Hold time low € to T		5	1		ns





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74LS386P is a semiconductor circuit containing four integral circuits configured into dual input exclusive OR gates.

FEATURES

- Capable of withstanding high input voltages $(V_1 \ge 15V)$
- Low power dissapation (P_d = 30.5mW typical)
- High operating speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

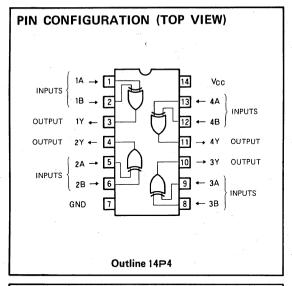
FUNCTIONAL DESCRIPTION

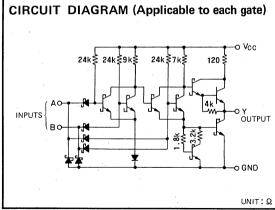
The use of Shottky TTL technology has enabled the achievement of high input voltages, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Υ
L	L	L
Н	Ļ	Н
L	Н	Н
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V _I	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V .
Topr	Operating free-air ambient temperature range		-20~+75	*c
Tstg	Storage temperature range		−65∼ + 150	*c



QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

	D			Limits		Unit
Symbol	. Param	neter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
loh	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75$ °C, unless otherwise noted.)

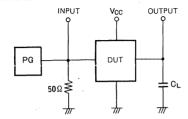
	D	Test conditions			Limits		Unit
Symbol	Parameter	rest conditions		Min	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
.,		V _{CC} =4.75V, V _I =0.8V			3.4		.,
V _{OH}		$V_1 = 2V, I_{OH} = -400 \mu A$		2.7			V
.,		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	V
	High Is all the	V _{CC} =5.25V, V _I =2.7V	<u>'</u>			40	μА
l _{IH}	High-level input current	V _{CC} =5.25V, V _I =10V				0.2	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.8	mA
Ios	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
Icc	Supply current	V _{CC} =5.25V (Note 2)			6.1	10	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

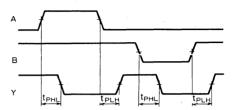
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

	Parameter	Test conditions	Limits			Unit
Symbol	i ai anietei	rest conditions	Min	Тур	Max	Oilit
tpLH	Low-to-high-level, high-to-low-level output	C. —1En E. Other inputs law (Note 2)		8	23	ns
t _{PHL}	propagation time	C _L =15pF, Other inputs low (Note 3)		12	17	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C ₁ = 15pF, Other inputs high (Note 3)		8	30	ns
t _{PHL}	propagation time	CL—13pF, Other Imputs high (Note 3)		10	22	ns

, Note 3, Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_{Γ} = 6ns, $t_{\bar{\Gamma}}$ = 6ns, t_W = 500ns, Vp = 3Vp.p, Z_O = 50 Ω . (2) C_L includes probe and jig capacitance.



Note 1. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{2.} Icc is measured with all inputs grounded.

M74LS390P

DUAL DECADE COUNTER

DESCRIPTION

The M74LS390P is a semiconductor integrated circuit containing two asynchronous decade counters with direct reset inputs

FEATURES

- High mounting density with 2 circuits equivalent to LS90 and LS290
- Direct reset inputs independent for both circuits
- Usable independently as binary and divide-by-5 counters
- High-speed counting (f_{max}= 80MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

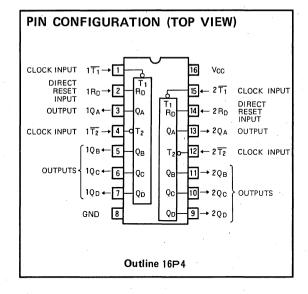
APPLICATION

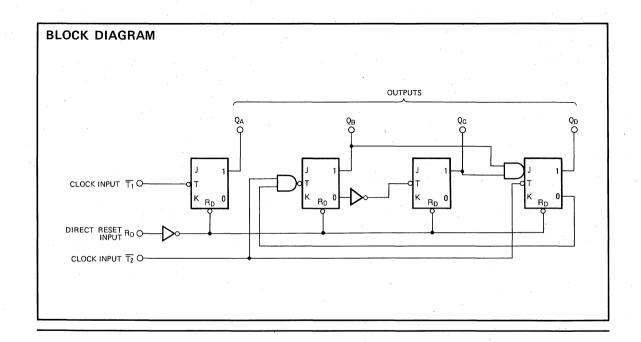
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and outputs Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and divide-by-5 counters can be reset simultaneously by setting direct reset input R_D high. For use as a counter, R_D is set low.





DUAL DECADE COUNTER

FUNCTION TABLE (Note 1)

Ŧ	R _D	QA	QB	Q _C	QD
Х	Н	L	L	L	L
1	L		Co	unt	

Note 1 ↓ : Transition from high to low (negative trigger)

X : Irrelevant

Count number	QA	· Q _B	Qc	Q _D
0	L	L	L	Ļ
1	Н	L	.L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	H
9	Н	L	L	Н

Valid when Q_{A} and $\overline{T_{2}}$ are connected and $\overline{T_{1}}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter Conditions		Limits	Unit
Vcc	Supply voltage	·	-0.5~+7	V
.,	Input voltage	Inputs T ₁ , T ₂	-0.5~+5.5	V
VI	mput voltage	Input R _D	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range	-	-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parame	tor		Limits		11-14
Syllibol	3ymoo Tarameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≤0.4V	0	-	4	mA
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parame	***	Tost son	distant		Limits		Unit
Symbol.	rarame	i arameter		Test conditions		Тур*	Max	Unit
VIH	High-level input voltage							V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18 mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.$		2.7	/3.4		V
\/.	Low-level output voltage		$V_1 = 2V$, $I_{OH} = -400 \mu A$ $V_{CC} = 4.75V$ $I_{OL} = 4 \text{ mA (Note 2)}$			0.25	0.4	V
V_{OL}	Low-level output voltage		$V_1 = 0.8V . V_1 = 2V$	I _{OL} = 8mA (Note 2)		0.35	0.5	V
		R _D					20	
		T ₁	V _{CC} =5.25V, V _I =2.	7V			100	μA
1	High-level input current	T ₂					200	
Ιн	riigii-level iliput current	R _D	V _{CC} =5.25V, V _I =10	V			0.1	
		T1		F. 1.			0.2	mA
		T ₂	$V_{CC} = 5.25V, V_I = 5.$	5 V			0.4	
		RD					-0.4	
lı <u>L</u>	Low-level input current	T ₁	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V			-1.6	mA
		T ₂					-2.4	
los	Short-circuit output current	(Note 3)	V _{CC} =5.25V, V ₀ =0\		-20		-100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4)			15	26	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A .

Note 3: All measurements should be done quickly not more than one output should be shorted at a time.

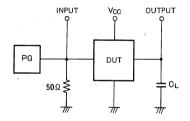
Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_D has been set from 4.5V to 0V.

DUAL DECADE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

	_			Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output $\overline{Q_A}$		25	80		MHz
fmax	Maximum clock frequency, from input \overline{T}_2 to output Q_B		12.5	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			8	20	ns
tpHL	propagation time, from input $\overline{T_1}$ to output Q_A			8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			24	60	ns
tPHL	propagation time, from input $\overline{T_1}$ to output Q_C			24	60	ns
· t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =15pF (Note 5)		10	21	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_B	·		10 ·	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			17	39	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_C			17	39	ns
t _{PLH}	Low-to-high-level, high-to-low-level output]		10	21	ns -
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			10	21	ns
t _{PHL}	High-to-low-level output propagation time, from input RD to outputs QA, QB, QC, QD			. 11	39	ns

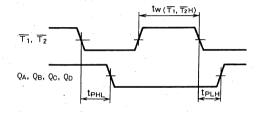
Note 5: Measurement circuit

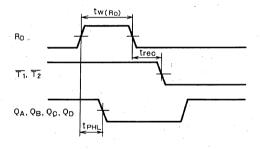


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, T_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P.P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	Oiiii
tw(T₁H)	Clock input $\overline{T_1}$ high pulse width		20	4		ns
t _W (T₂H)	Clock input T ₂ high pulse width		40	12		ns
tw(RD)	Direct reset R _D pulse width		20	4		ns
tr	Clock pulse rise time			400	100	ns
t _f	Clock pulse fall time			300	100	ns
trec(R _D)	Recovery time R_D to $\overline{T_1}$, $\overline{T_2}$		25	8		ns





M74LS393P

DUAL 4-BIT BINARY COUNTERS

DESCRIPTION

The M74LS393P is a semiconductor integrated circuit containing two 4-bit binary (hexadecimal) asynchronous counter circuits with direct reset inputs

FEATURES

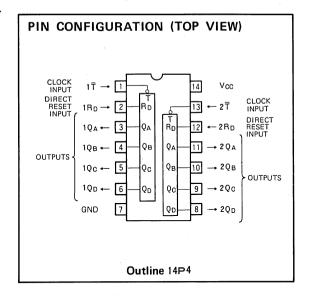
- High package density with 2 circuits equivalent to LS93 or LS293
- 2 discrete direct reset inputs
- High-speed counting (f_{max} = 75MHz typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

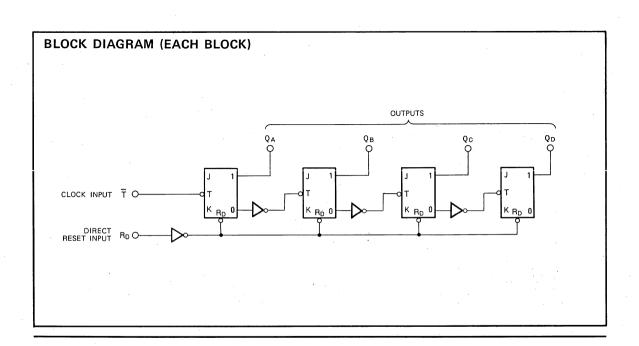
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a count pulse is fed to the clock input \overline{T} , pure binary code appear in at outputs Q_A , Q_B , Q_C , and Q_D . Counting is performed when \overline{T} changes from high to low. Reset is affected by making the direct reset input R_D high. For use as a counter, hold R_D low.





DUAL 4-BIT BINARY COUNTERS

FUNCTION TABLE (Note 1)

. ₹	R _D	QA	QB	Q _C	.Q _D
Х	Н	L	L .	L	L
1	L		Cou	nt	

Note 1: ↓: transition from high to low-level

X: irrelevant

Count	Q_{A}	QB	Qc	Q _D
. 0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	н	Н	L	L
4 .	L	L	Н	L
5	Н	Ϊ.	Н	L
6	L	н	Н	L
7	Н	н	Н	L
8	L	L	L	Н
9	Η	L	L	Н
10	L	н	L	Н
. 11	Н	.H	L.	Н
12	L	L	Н	Н
13	Н	L	Н	Н
14	L	Н	Н	Н
15	Ι	I	Н	Н

ABSOLUTE MAXIMUM RATINGS

($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
.,	In the second se	⊤input	-0.5~+5.5	
Vı	Input voltage	R _D input	-0.5~+15	, v
. V ₀	Output voltage	High-level state	-0.5~V _{CC}	V,
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal			Unit			
Symbol	Paramete	rarameter .				Unit
Voc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

C 1			T	141		Limits		Unit
Symbol	Parameter		Test cond	itions	Min	Тур*	Max	Onit
V _{IH}	High-level input voltage				. 2			V
VIL	Low-level input voltage						0.8	٧
V _{IC}	Input clamp voltage	clamp voltage		18mA	,		-1.5	V
VoH	High-level output voltage		1	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-400 μA		3.4		V
VoL	Low-level output voltage		V _{CC} =4.75V			0.25	0.4	٧
			V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	V
		R _D	V _{CC} =5.25V, V _I =2.7V				20	μΑ
	High level inner access	T	VCC-5.25V, VI-2.7	Y :			100	μΑ
lін	High-level input current	RD	V _{CC} =5.25V, V _I =10V	1			0.1	m A
		T ·	V _{CC} =5.25V, V _I =5.5	V			0.2	mΑ
1	Linux Investigation accounts	R _D					-0.4	4
l IL	Low-level input current	Ŧ	$V_{CC}=5.25V, V_{I}=0.4V$				-1.6	m A
los	Short-circuit output current (N	ote 2)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
Icc -	Supply current	V _{CC} =5.25V (Note 3)			15	26	mA	

*: All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: I_{CC} is measured with T input grounded and a momentary 4.5V, then grounded, applied R_D input.

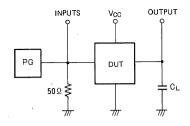


DUAL 4-BIT BINARY COUNTERS

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	i di diffetei	T SST SSTIGITION		Тур	Max	Unit _
f _{max}	Maximum clock frequency		25	75		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		8	20	ns
t _{PHL}	time, from input \overline{T} to output Q_A	C _L =15pF (Note 4)		8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			36	60	ns
t _{PHL}	time, from input \overline{T} to output Q_D			36	60	ns
tpHL	High-to-low-level output propagation time, from input R _D to output Q _A , Q _B , Q _C , Q _D			11	39	ns

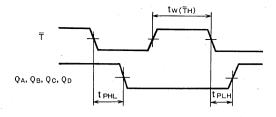
Note 4: Measurement circuit

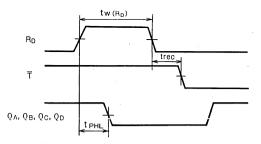


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _W (₸H)	Clock input T high pulse width		20	4		ns	
t _W (R _D)	Direct reset input RD pulse width		· 20	4		ns	
tr	Clock pulse rise time			400	100	ns	
tf	Clock pulse fall time			300	100	ns	
trec(RD)	Recovery time R _D to T		25	7		· ns	





M74LS395AP

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS395AP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

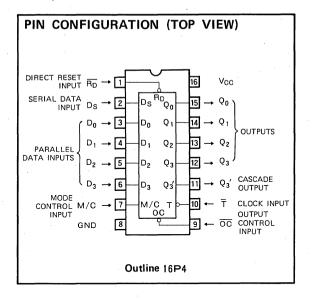
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Output control input provided
- Q₀~Q₃ usable in AND-Tie connection (3-state output provided)
- Bit number can be expanded
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ} C$)
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)

APPLICATION

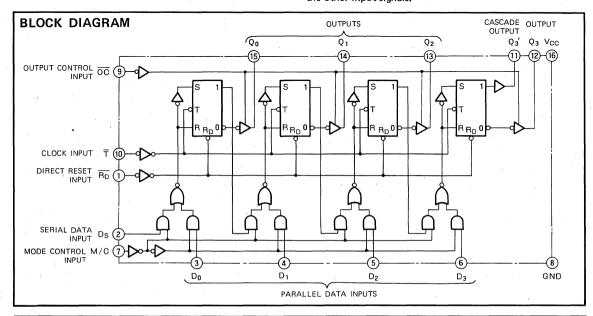
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-series/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to the serial data input D_S and the clock pulse is applied to the clock input \overline{T} , the serial data are shifted sequentially to outputs $Q_0 \sim Q_3$ and Q_3 in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and the 1-bit clock pulse is applied to the \overline{T} , signals $D_0 \sim D_3$ appear in outputs $Q_0 \sim Q_3$ and Q_3 . When \overline{T} changes from high to low, the right shift or parallel data read operation is performed. When M/C is kept in high, Q_3 is



connected to D₂, Q₂ to D₁ and Q₁ to D₀, the serial data are applied to D₃, and the clock pulse is applied to $\overline{\Gamma}$, the left shift operation is performed. When a high-level state is applied to output control input \overline{OC} , Q₀~Q₃ are put in a high-impedance state and AND-Tie connection is made possible. There will be no effect on the shift and parallel data reading operations even when \overline{OC} is changed. Cascade output Q₃' is used for bit number expansion. Even if \overline{OC} is changed in this state, there is no effect on the shifting and parallel data reading. By setting direct reset input \overline{RD} and \overline{OC} low, Q₀~Q₃' are reset low irrespective of the status of the other input signals.



4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

				Inj	put					·3-state	output		Cascade output
Function mode		M/C	-	D-		Paralle	input						0.1
	R _D M/C	'	Ds	Do	D ₁	D ₂	D ₃	Qo	Q ₁	Q ₂	Qз	Q3′	
Direct reset	L	X	Х	Х	×	Х	X	X	L	L `	L	L	L
Output hold	Н	Н	н	X	×	×	X	Х	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q3 ⁰	Q ₃ 0
Parallel output	Н	Н	↓	X	D ₀	D ₁	D ₂	D ₃	D ₀	D ₁	D ₂	D ₃	D3
Output hold	Н	L	Н	х	х	X	х	Х	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q3 ⁰	Q ₃ 0
Right shift	Н	L.	Ţ	Н	×	×	×	×	Н	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q2 ⁰
	Н	L	1	L	X	Х	х	Х	L	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q2 ⁰

Note 1. ↓ : Transition from high to low (negative edge trigger)

Q0: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

Output impedance state is high when OC is high.

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			$-0.5 \sim +7$	V
VI	Input voltage			-0.5~+15	V
.,	0	Q ₀ ~ Q ₃	Off-state	-0.5~+5.5	V
Vo.	Output voltage	Q ₃ ′	High-level output	-0.5~Vcc	V
Topr	Operating free-air ambien	nt temperature range		−20∼+75	°
Tstg	Storage temperature rang	ре		−65∼ + 150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol		Parameter	promotor		Limits			
Зуппьог		rarameter		Min	Тур	Max .	Unit	
Vcc	Supply voltage			4.75	5	5.25	٧	
lau	High-level	Q ₀ ~ Q ₃	V _{OH} ≥2.4V	0		-2.6	mA	
TOH	Output current	Q3'	V _{OH} ≧2.7V	0		-400	μΑ	
		00-	V _{OL} ≤0.4V	0		12	mΑ	
	Low-level	$Q_0 \sim Q_3$	V _{OL} ≤0.5V	0		24	mA	
IOL	IOL output current	0.1	V _{OL} ≤0.4V	0		4	mΑ	
		Q3'	V ₀ L≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditi			Limits		Unit
	raiametei		rest condition	rest conditions			Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -1	8mA			-1.5	V
VoH	High-level output voltage	Q ₀ ~Q ₃	V _{CC} =4.75V, V _I =0.8V	I _{OH} = -2.6mA	2.4	3.1		V
V OH	i ingri-rever output vortage	Q3′	V _I = 2 V	I _{OH} = -400 μ A	2.7	3.4		
		0 0-		I _{OL} = 12mA		0.25	0.4	V
VoL	Voi Low-level output voltage	Q ₀ ~ Q ₃	V _{CC} =4.75V	I _{OL} = 24mA		0.35	0.5	y
VOL	Low-level output voltage	Q ₃ ′	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 4 mA		0.25	0.4	V
				I _{OL} = 8 mA		0.35	0.5	V
lozh	Off-state high-level output current	Q ₀ ~Q ₃	$V_{CC} = 5.25V, V_I = 2V,$	V ₀ = 2.7 V			20	μА
lozL	Off-state low-level output current	Q ₀ ~Q ₃	V _{CC} =5.25V, V _I =2V,	V _O = 0.4 V			-20	μА
Лн	High-level input current		V _{CC} =5.25V, V _I =2.7\	/ .			20	μА
чн	· ·		$V_{CC} = 5.25V, V_I = 10V$	V _{CC} =5.25V, V _I = 10V			0.1	mA
HL	Low-level input current		V _{CC} =5.25V, V _I =0.4\	/			-0.4	mA
laa	Short-circuit output current (Note 2)	$Q_0 \sim Q_3$	\\		- 30		- 130	mA
los	Short-circuit output current (Note 2)	Q ₃ ′	$V_{CC} = 5.25V, V_{O} = 0 V$		- 20		- 100	mA
loc	Supply current	current V _{CC} =5.25V (I				21	31	mA
lccz	Supply current, all outputs off	urrent, all outputs off V _{CC} = 5.25V (Note 4)			22	34	mA	

All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current $|_{CC}$ should be measured with $\overline{\text{RD}}$, D_{S} and M/C at 4.5V and $D_{\text{D}}\sim D_{\text{3}}$, $\overline{\text{OC}}$ and $\overline{\text{T}}$ at 0V. Note 4: $|_{\text{OCZ}}$ is measured with $\overline{\text{RD}}$, D_{S} , M/C and $\overline{\text{OC}}$ at 4.5V, and $D_{\text{O}}\sim D_{\text{3}}$ at 0V after $\overline{\text{T}}$ has been set from 3V to 0V.

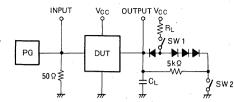


4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	i aranieter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30	40		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation			14	30	ns
t _{PHL}	time, from input \overline{T} to outputs $Q_0 \sim Q_3$, Q_3'	C _L = 15pF (Note 5)		16	30	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to output $Q_0 \sim Q_3$, Q_3'			20	35	ns
t _{PZH}	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		13	25	ns
t _{PZL}	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		15	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		11	17	ns
tPLZ	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		10	20	ns

Note 5: Measurement circuit

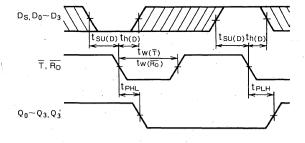


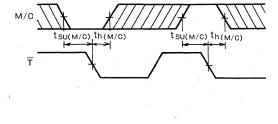
Symbol	SW1	SW2
tpzh	Open	Closed
tpzL	Closed	Open
tpLz	Closed	Closed
tphz	Closed	Closed

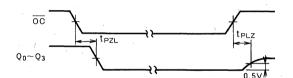
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}, Z_0 = 50\Omega.$
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C₁ includes probe and jig capacitance

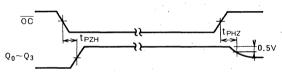
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
		rest conditions	Min	Тур	Max	Unit
tw(₹)	Clock input T high pulse width		25	10		ns
tw(RD)	Direct reset RD pulse width		20	5		ns
tsu(D)	Setup time D to T		20	9		ns
tsu(M/C)	Setup time M/C to T		40	16		ns
t _{h(D)}	Hold time D to Ţ		10	- 1		ns
th(M/C)	M/C hold time to \overline{T}		10	-12		ns









Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

MITSUBISHI LSTTLS M74LS423P

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

DESCRIPTION

The M74LS423P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- A. B complementary inputs provided
- Direct reset pulses with no one-shot operation.
- High input breakdown voltage $(V_1 \ge 15V)$
- Q and Q outputs
- Wide operating temperature range (T_a=-20~+75°C)

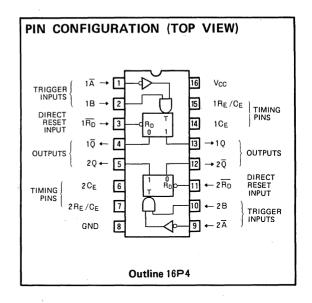
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1 on the next page, and by applying a trigger from input \overline{A} or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied.

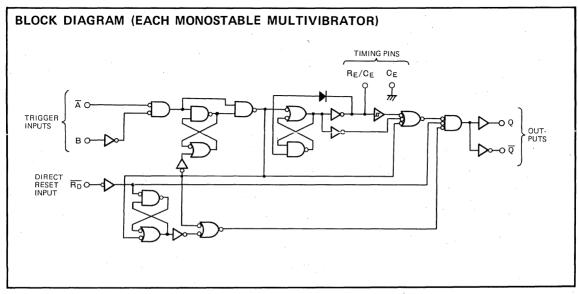
The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from \overline{A} or B immediately before the output pulse is completed, the



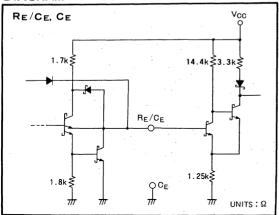
output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and \overline{Q} high by setting direct reset input \overline{R}_D low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the \overline{R}_D signal. (Fig. 2(c))

The above functions are the same as for the M74LS123P. However, when $\overline{R_D}$ changes from low to high with \overline{A} at low and B at high for the M74LS123P, the trigger is applied and one-shot operation takes place, whereas with the M74LS423P one-shot operation does not take place for the same change in $\overline{R_D}$.



TIMING TERMINAL EQUIVALENT CIRCUIT DIAGRAM



FUNCTION TABLE (Note 1)

R _D	Ā	В	Q	Q
L	Х	X	L	Н
Х	Н	Х	L	Н
X	Х	L	L	Н
Н	L	î	几	T_
Н	1	Н	<u></u>	

Note 1. ↑ Transition from low to high. (positive edge triggering)

: Transition from high to low. (negative edge

☐: Positive one-shot operation.

__: Negative one-shot operation.

X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E . Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect C_E to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

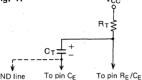


Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width tw

The output pulse width tw is set by RT and CT

2-1. When CT is greater than 1000pF

 $t_W = \kappa \cdot R_T \cdot C_T \text{ (ns)} \times (1+0.1)$

Depending on the product, fluctuations of about $\pm 10\%$ may arise.

Refer to $K-C_T$ characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is brought to K by value of R_T .)

 $R_{\rm T}$ is measured in kilohms and $C_{\rm T}$ in picofarads Depending on the product, fluctuations in the order of 3/-10%may occur.

R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF Refer to the output pulse width versus— C_T , R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and \overline{R}_D signal.

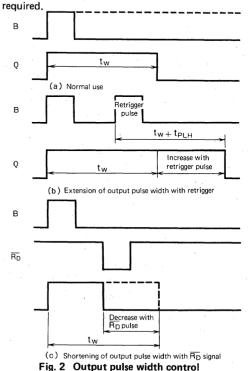
3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width $t_{\rm w}$ can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger function

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as



4. Precautions with use

- 4-1. Apply the retrigger pulse after a wait of 0.22C_T (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.
- 4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible (less than 3cm) and avoid signal wires which may be conducive to noise.
- 4-3. Connect an external capacitor of $0.01 \sim 0.1 \mu F$ with good high-frequency characteristics between pins V_{CC} and GND.
- 4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level stage	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	င
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramete	or :		Limits		Unit
Symbol	, arameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
1	Low-level output current	V _{OL} ≦0.4V	0		4	mΑ
loL		V ₀ L≦0.5V	0		8	mΑ
RT	External timing resistance		5		260	kΩ
Ст	External timing capacitance			No	ne	
CR	RE/CE pin wiring capacitance				50	рF

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Parameter	Tort on	nditions		Limits		Unit
Symbol	rarameter	lest con	Test conditions		Typ ∗	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	V
VoH	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.5		٧
V _{OL}	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} = 4 mA		0.25	0.4	V
	High-level input current	V _{CC} =5.25V, V _I =2	2.7V			20	μА
liH .	riign-iever input current	V _{CC} =5.25V, V _I =1	0 V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 3	3)		12	20	mΑ

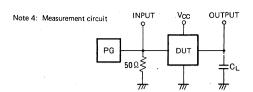
^{* :} All typical values are at $V_{CC}=5V$, $T_a=25^{\circ}C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, \overline{A} and B and \overline{A} set from 0V momentarily to 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25°C, unless otherwise noted)

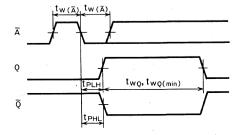
Symbol	D	Test conditions	Limits			Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input $\widetilde{\mathbf{A}}$ to output Q				33	ns
t _{PLH}	Low-to-high-level output propagation time, from input B to output Q				44	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{A} to output \overline{Q}	C _T = 0 pF			45	ns
t _{PHL}	High-to-low-level output propagation time, from input B to output $\overline{\mathbb{Q}}$	$R_T = 5 k\Omega$			- 56	ns
t _{PHL}	High-to-low-level output propagation time, from input RD to output Q	C _L =15 _p F (Note 4)			27	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}	i i			45	ns
t _{WQ (min)}	Minimum output pulse width, from inputs A. B to output Q				200	ns
t _{WQ}	Output pulse width, from inputs \overline{A} . B to output Q	$C_T = 1000 pF$, $R_T = 10 k \Omega$ $C_L = 15 pF$ (Note 4)	4		. 5	μs

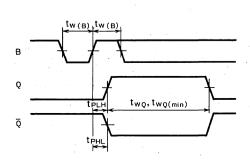


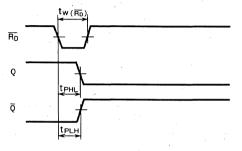
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz (100kHz with t_{WQ} measurement), t_r =6ns, t_w \geq 40ns, V_P =3 V_{PP} , Z_Q =50 Ω .
- (2) C₁ includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC} = 5 V , T_a = 25°C , unless otherwise noted)

Symbol	Symbol Parameter	Test conditions		Limits		Unit
Symbol	rest conditions	Min	Тур	Max	Onit	
t _{W(A)}	Trigger input Ā pulse width		40	•		ns
t _{W(B)}	Trigger input B pulse width		40			ns
tw(RD)	Direct reset input pulse width RD		40			ns



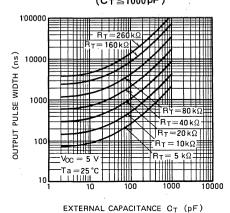




0.2

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VS CT. RT (CT≤1000pF)



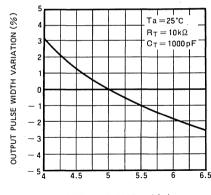
Note 5: The error of the output pulse width in the above graph is within ±20%.

$(C_{T} > 1000 pF)$ 0.9 K (FACTOR FOR DERIVING OUTPUT PULSE WIDTH) V_{CC} = 5 V 0.8 Ta = 25°C 0.7 KC-B-(tw 0.6 0.5 0.4 0.3

K VS CT

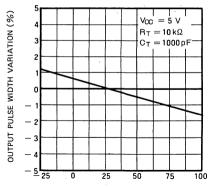
EXTERNAL CAPACITANCE C+ (pF)

OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



SUPPLY VOLTAGE VC (V)

OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



AMBIENT TEMPERATURE Ta (°C)

M74LS490P

DUAL 4-BIT DECADE COUNTER

DESCRIPTION

The M74LS490P is a semiconductor integrated circuit containing a dual circuit asynchronous decade counter with direct reset input and direct 9-set input.

FEATURES

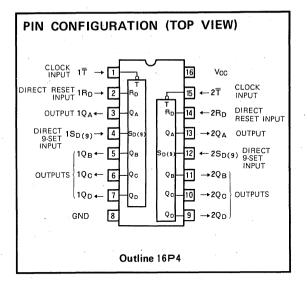
- Two integral circuits (the functional equivalent of LS90 and LS290) provide high mounting density capability
- Individual clock, direct clear, and set-to-9 inputs for each decade counter
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

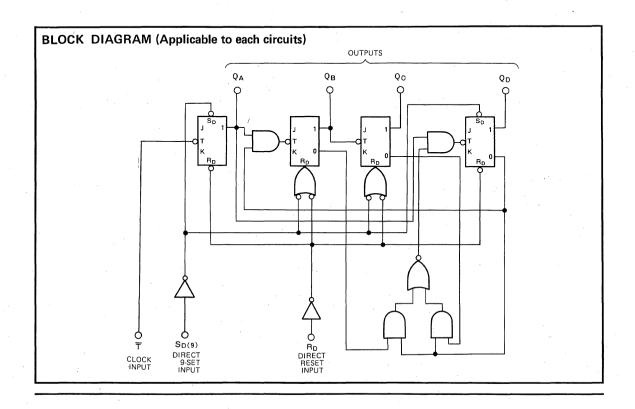
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions to produce binary-coded decimal output at Q_A , Q_B , Q_C , and Q_D in response to count pulse input at clock input \overline{T} . Counting occurs when \overline{T} transits from high to low-level. A high-level status at direct reset input R_D or direct 9-set input $S_{D(9)}$ initiates reset or a setting to 9 respectively. When operated as a counter, R_D and $S_{D(9)}$ are set low-level.





DUAL 4-BIT DECADE COUNTER

FUNCTION TABLE (Note 1)

Ŧ	RD	S _{D(9)}	QA	Qв	Qc	QD	
×	Н	L	L	L	L	L	
×	L	Н	Н	L	L	Н	
1	L	L	Count				

Note 1. ↓: Transition from high to low

(negative edge trigger)

X : Irrelevant

Count	Q _A	Q _B	Qc	QD
0	L	L	L	L
1	Н	L	L	L
2.	L	Н	L	L
3	Н	. н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	Ι	L	L	Н

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	Input voltage	INPUT T	-0.5~+5.5	V
V _I Input voltage	INPUT RD, SD(9)	-0.5~+15	V	
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumhal	Parame	Parameter Limits Min Typ Max		Limits			
Symbol	1 didilit					Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ	
		V _{OL} ≤0.4V	0		4	mA	
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Constant	Parameter	Test condition	•	Limits					
Symbol	rarameter		rest condition	5	Min	Typ *	Max	Unit	
V _{iH}	High-level input voltage				2			V	
V _{IL} .	Low-level input voltage						0.8	V	
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{1C} = -18n	nA _.			-1.5	V	
V _{OH}	High-level output voltage	."	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} = -400 μA		2.7	3.4		٧	
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧	
			V _I =0.8V, V _I =2V	I _{OL} =8mA	0.35		0.5	V	
		R _D , S _{D(9)}	V _{CC} =5.25V, V _I =2.7V				20		
Lan	High-level input current	₸	VCC-5.25V, VI-2.7V				100	μА	
LiH	righ-level input current	R _D , S _{D (9)}	V _{CC} =5.25V, V _I =10V				0.1	mA	
		Ŧ	V _{CC} =5.25V, V _I =5.5V				0.2	mA	
1.	Low level input ourrent	R _D , S _{D (9)}	V — F 25V V — 0 4V				-0.4	^	
I _{IL}	Low-level input current		T V _{CC} =5.25V, V _I	$V_{CC}=5.25V, V_{I}=0.4V$				-1.6	mΑ
Ios	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA	
1 _{CC}	Supply current		V _{CC} =5.25V (Note 3)			15	26	mA	

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

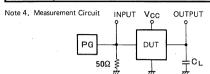
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} ICC is measured with all outputs open, both RD and SD(g) inputs grounded following momentary connection to 4.5V; all other inputs grounded.

DUAL 4-BIT DECADE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

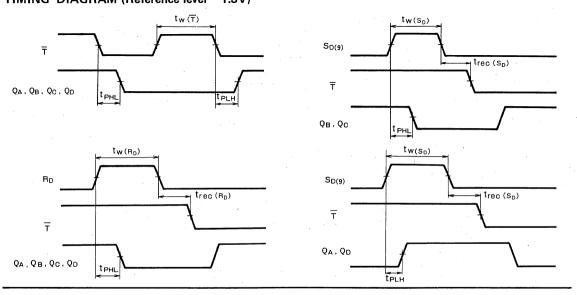
		Total and disional	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency (from input T to output Q _A)		25	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	20	ns
t _{PHL}	time, from input \overline{T} to output Ω_{A}			. 8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			. 20	39	ns
t _{PHL}	time, from input \overline{T} to outputs Q_B , Q_D			22	39	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		30	54	ns
t _{PHL}	time, from input \overline{T} to output Q_C			30	54	ns
t _{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A , Q_B , Q_C , Q_D			11	39	ns
t _{PLH}	Low-to-high-level output propagation time, from input $S_{D(9)} \mbox{ to outputs } \textbf{Q}_A \mbox{, } \textbf{Q}_D$:		11	39	ns
t _{PHL}	High-to-low-level output propagation time, from input $S_{D(9)}$ to outputs Q_B , Q_C			12	36	ns



- (1) The pulse generator (PG) has the following characteristics:
- The pulse generator (FG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_p = 3 V_p - P_p , Z_0 = 50 Ω . (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol			Limits			
	Parameter	Test conditions	Min	Тур	Max	Unit
tw(Ŧ)	Clock input T pulse width		20	5		ns
tw(RD)	Direct reset R _D pulse width		20	- 4		ns
tw(SD)	Direct 9-set S _{D(9)} pulse width		20	4		ns
tr	Clock pulse rise time			400	100	ns
tf	Clock pulse fall time			300	100	ns
trec (RD)	R_{D} recovery time to \overline{T}		25	8		ns
trec (SD)	$S_{D(9)}$ recovery time to \overline{T}		25	8		ns



OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS540P is a semiconductor integrated circuit containing 1 block of buffer with 3-state inverted output and common output control input for all 8 discrete circuits.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁≥5V)
- Output control inputs provided (OC1 OC2)
- High fan-out, 3-state output (I_{OL} = 24mA, I_{OH} = -15mA)
- Data flow-thru pin out
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

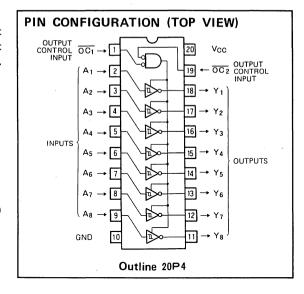
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and input high break-down voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When output control inputs \overline{OC}_1 and \overline{OC}_2 are low, a high-level signal appears at output Y if input A is low and a low-level signal appears if it is high.

All outputs are set to the high-impedance state regardless of the status of A when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state.

The input and output pins are arranged for facilitated



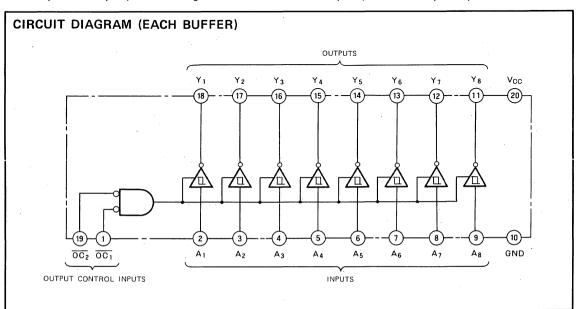
FUNCTION TABLE (Note 1)

Α	CC ₁	OC ₂	Υ
L	L	L	Н
Н	L	Y L	L
X	L	Н	Z
X.	Н	L	Z
X	Н	Н	Z

Note 1: Z: high-impedance

X: irrelevant

board layout (data flow-thru pin out).



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range	· · · · · · · · · · · · · · · · · · ·	−20~+75	℃
Tstg	Storage temperature range		-65~+150	,C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Limits			
Symbol			Min	Тур	Max	Unit.	
Vcc	Supply voltage	,	4.75	5	5.25	V	
	12.1.1	V _{OH} ≧2.4V	0		-3	mA	
Іон	High-level output current	0		15	mA		
		V _{OL} ≦0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Table 1997	Limits			Unit
Symbol	Parameter	Test conditions	Min	Typ*	Max	Onit
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _T , -V _T .	Hysteresis .	V _{CC} =4.75V	0.2	0.4	,	. V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
V-	High-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V$, $I_{OH} = -3 \text{ mA}$	2.4	3.4		٧
V _{OH}	i lightever output voltage	$V_1 = 2V$ $V_1 = 0.5V$, $I_{OH} = -15mA$	2			V
VoL	Low-level output voltage	$V_{CC} = 4.75V$ $I_{OL} = 12mA$		0.25	0.4	٧
VOL	Low-level output voltage	$V_1 = 0.8V$, $V_1 = 2V$ $I_{OL} = 24mA$		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	. μΑ
lozL	Off-state low-level output current	$V_{CC} = 5.25V, V_1 = 2V, V_0 = 0.4V$			-20	μА
I	High-level input current	V _{CC} =5.25V, V _I =2.7V			. 20	μА
Іін	riigii-level iliput current	V _{CC} =5.25V, V _I =10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0V	40		-225	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		. 13	25	mA
Iccl	Supply current, all outputs low	$V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V$		24	45	mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =4.5V		30	52	mA-

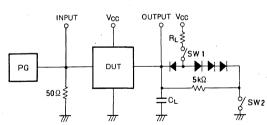
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol Parameter	D	Test conditions	Limits		, Unit	
	Parameter	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF			15	ns
t _{PHL}	time, from input A to output Y	(Note 3)			15	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)			38	ns
tpzh	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)			25	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)			25	ns.
t _{PHZ}	Output disable time from high-level	R _L =667Ω C _L = 5 pF (Note 3)			18	ns

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C. Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

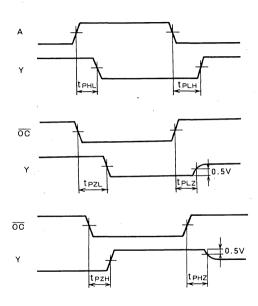
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

Note 3: Measurement circuit



٠.			
	Parameter	\$W 1	SW2
	t PZH	Open	Closed
,	t PZL	Closed	Open
,	t _{PLZ}	Closed	Closed
	t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P.P.} Z_O = 50Ω
 (2) All diodes are switching diodes (t_{ff} ≤ 4ns)
- (3) C₁ includes probe and jig capacitance.



OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS541P is a semiconductor integrated circuit containing 1 buffer block with 3-state non-inverted outputs and is provided with output control inputs which are common to 8 circuits and which are independent.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage (V₁ ≥ 15V)
- Output control inputs provided (OC₁, CO₂)
- High fan-out 3-state outputs
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Data flow-thru pin out
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

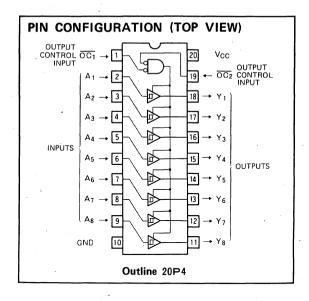
FUNCTIONAL DESCRIPTION

Since pnp transistors are used for the input circuits, the input load factor is small and a input high breakdown voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $\overline{OC_1}$ or $\overline{OC_2}$ is low, low appears in output Y if input A is low, and high appears in Y if A is high.

All outputs are set to the high-impedance state when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state.

The input and output pins are arranged for facilitated board layout (data flow-thru pin out).

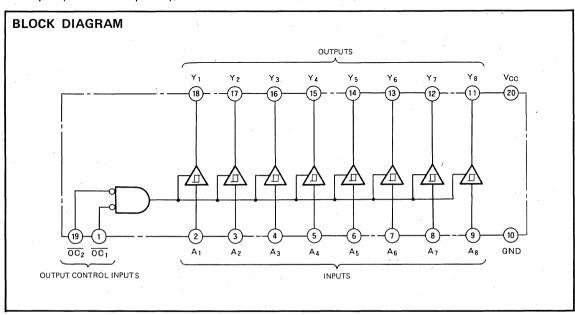


FUNCTION TABLE (Note 1)

Α	OC ₁	OC ₂	Υ
L	L	L	L
Н	L	L	. н
X	L	Ι	Z
Х	Н	L	Z
Х	Н	Н	Z

Note 1 Z : High-impedance

X: irrelevant





OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Complete	Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
1	High-level output current	V _{OH} ≥2.4V	0		-3	mA	
Іон	High-level output current	V _{0H} ≧ 2 V	0		— 15	mA	
1		V ₀ L≦0.4V	0		. 12	mA	
IOL	Low-level output current	V ₀ ∟≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

		T		Limits		11-2-
Symbol	· Parameter	Test conditions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V	0.2	0.4		٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
.,	High Is at subset college	$V_{CC}=4.75V$ $V_{I}=0.8V$, $I_{OH}=-3r$	nA 2.4	3.4		V
V _{OH}	High-level output voltage	$V_1 = 2V$ $V_1 = 0.5V, I_{OH} = -15$	mA 2			V
		V _{CC} =4.75V . I _{OL} =12m	Α	0.25	0.4	٧
VoL	Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24m	Α	0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V, V _O =0.4V		,	-20	μА
	History and the second	V _{CC} =5.25V, V _I =2.7V			20	μА
IIH	High-level input current	V _{CC} =5.25V, V _I =10V			. 0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0V	-40	1	-225	mA
Іссн	Supply current, all outputs high	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		18	32	mA
ICCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$		30	52	mA
locz	Supply current, all outputs disabled	V _{CC} =5.25V, V _I =0V, V _I =4.5V		32	55	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

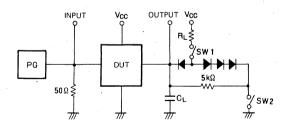
SWITCHING CHARACTERISTICS ($V_{CO} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

0	D	Took one distance		Unit		
Symbol	Parameter .	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		,	15	ns
t _{PHL}	time, from input A to output Y	(Note 3)			18	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $G_L = 45pF$ (Note 3)			38	ns
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)			32	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)			29	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)			18	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

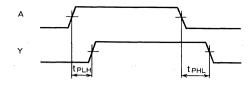
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

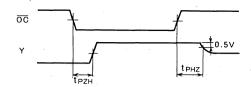
Note 3: Measurement circuit

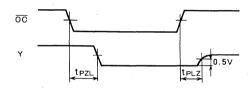


Symbol	SW1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t phz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) All diodes are switching diodes (t_{rr}. ≤ 4ns)
- (3) C₁ includes probe and jig capacitance.







DESCRIPTION

The M74LS595P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with a 3-state output latch.

FEATURES

- 8-bit serial in, parallel out shift register with latch
- Shift register has direct reset (RSFT)
- Independent clock input pins (TSET, TLAT)
- 3-state, high fan-out outputs ($Q_0 \sim Q_7$) ($I_{OL} = 24$ mA, $I_{OH} = -2.6$ mA)
- Cascade output pin provided (Q₇')
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATIONS

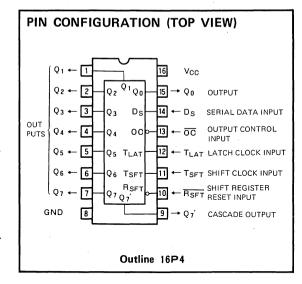
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops. Separate clocks are used for shifting and latching.

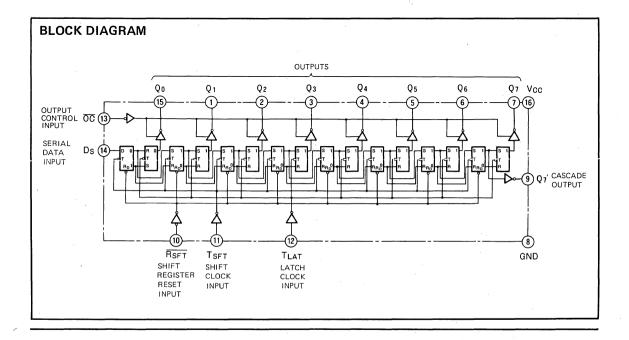
The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high.

Serial data input D_s is the data input of the first stage shift register and when it is high and a pulse is applied to T_{SFT} , the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT} , the low signal enters the shift register in sequence.



When the pulse is applied to T_{LAT} , the contents of the shift register are stored in the latch register and appear at $\Omega_0 \sim \Omega_7$. $\Omega_0 \sim \Omega_7$ are 3-state outputs with buffers. Cascade output Ω_7 at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.



When shift register reset input $\overline{R_{SFT}}$ is set low, the shift register and Q_7 are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output control input \overline{OC} , $O_0 \sim O_7$ are put in a high-impedance state but O_7 , does not change. \overline{OC} status changes have no effect on the shift operation

FUNCTION TABLE (Note 1)

Omereti	na mada			Input						3-stat	e output				Cascade
Operati	ng mode	R _{SFT}	T _{SFT}	TLAT	Ds	ōc	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q7	output Q'7
Reset	Shift t ₁	L	×	Х	. X	L	Q_0^0	Q ₁ 0	Q ₂ 0	Q ₃ 0	Q4 ⁰	Q ₅ ⁰	Q ₆ ⁰	Q ₇ 0	L
neset	Latch t ₂	×	×	Ť,	Х	L	L	L	L	L	L	L	L	L	L
	Shift t ₁	Н	1	Х	Н	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q ₇ 0	9 6 ⁰
Shift/latch	Latch t ₂	н	X	1	Х	L	Н	qo ⁰	q 1 ⁰	92 ⁰	93 ⁰	94 ⁰	q5 ⁰	96 ⁰	96 ⁰
operation	Shift t ₁	Н	1	Х	L	L	Q_0^0	Q1 ⁰	Q_2^0	Q ₃ ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q ₇ 0	96 ⁰
	Latch t ₂	Н	×	1	Х	L	L	900	9 1 ⁰	92 ⁰	q ₃ 0	94 ⁰	95 ⁰	96 ⁰	96 ⁰
3-s	tate	Х	×	×	X	Н	Z	Ζ.	Z	Z	Z	z	Z	Z	97

Note 1. ↑: transition from low to high level (positive edged trigger)

Q0: level of Q before the indicated steady-state input conditions were established

X : Irrelevant

q0 : contents of shift register before $T_{\mbox{\scriptsize SFT}}$ is applied

 $\ensuremath{\mathbf{q}}$: shift register contents

 t_1, t_2 : t_2 is set after t_1 has been set

Z: high-impedance state

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +.75$ °C, unless otherwise noted)

Symbol	Parar	meter	Test conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	. V
V _I	Input voltage			-0.5~+15	V
Vo	Output voltage	Q0~Q7	High-level state	-0.5~+5.5	V
VO	Output voltage	Q ₇ ′	Off-state	-0.5~V _{CC}	· V
T _{opr}	Operating free-air ambient te	mperature range		-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C ·

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol		Parameter			Limits				
Symbol		rarameter		Min	Тур	Max	Unit		
Vcc	Supply voltage			4.75	5	5.25	V		
	High-level output	Q0~Q7	V _{OH} ≥2.4∨	0		-2.6	mA		
Тон	current	Q ₇ ′	V _{OH} ≥2.7V	0		-400	μΑ		
		.00	V _{OL} ≤0.4V	0		12	mA		
I -	Low-level output	Q0~Q7	V _{OL} ≤0.5V	0		24	mA		
IOL	current .	Q7	V ₀ L≦0.4V	0		4	mA		
		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{OL} ≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

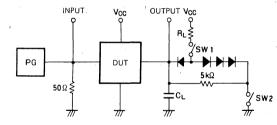
Symbol	Parameter		Test condit	tions		Limits		Unit
Зуппон	raidifietei		rest contain	iiona	Min	Тур 🛊	Max	Olit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
.,	High-level output voltage	Q ₀ ~Q ₇	V _{CC} =4.75V	I _{OH} =-2.6mA	2.4	3.1	-	٧
V _{OH}	Trigitiever output vortage	Q ₇ ′	V _I =0.8V, V _I =2V	I _{OH} =-400µA	2.7	3.4		٧
				I _{OL} =12mA		0.25	0.4	٧
	Low-level output voltage	Q ₀ ~Q ₇	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	
VoL	Low-level output voltage	0.1	V _I =0.8V	I _{OL} =4mA		0.25	0.4	· V
		Q ₁ '	V _I =2V	I _{OL} =8mA		0.35	0.5	
lozh	Off-state high-level output current	Q ₀ ~Q ₇	V _{CC} =5.25V, V _I =0.8V,	V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	Q ₀ ~Q ₇	V _{CC} =5.25V, V _I =0.8V,	V _I =2V, V _O =0.4V			-20	μА
			.,	V ₁ =2.7V			20	μА
I _{IH}	High-level input current		V _{CC} =5.25V	V _I =10V			0.1	mA
	Low-level input current	Ds					-0.4	mA
IIL	Low-level input current	Input except Ds	V _{CC} =5.25V, V _I =0.4	. v			-0.2	mA
	Chart size it and a second (Nata 2)	Q ₀ ~Q ₇	\	,	-30		-130	mA
los	Short-circuit output current (Note 2)	Q7	$V_{CC} = 5.25V, V_{O} = 0V$,	-20		-100	mA
Гссн	High-level supply current		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		29	50	mA
ICCL	Low-level supply current		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		39	65	mA
Iccz	Off-state supply current		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		41	65	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Cb1	Personne	Test conditions	-	Limits		11.12
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
f _{max}	Maximum repeat frequency		20	25		MHz
t _{PLH}	Low-to-high, high-to-low output propagation time, from			11	18	ns
t _{PHL}	input T _{SFT} to output Q' ₇	C ₁ = 15pF (Note 3)		16	25	115
t _{PHL}	High-to-low output propagation time from input $\overline{R_{SFT}}$ to output Q'_7	CL=15pr (Note 3)		19	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from	0 45-5 (N - 2)		12	18	ns
t _{PHL}	input T_{LAT} to outputs $Q_0 \sim Q_7$	C _L =45pF (Note 3)		22	35	115
t PZH	Output enable time to high level	B = 057.0 1.0 = 450.5 (No. + 2)		16	30	ns
tpzL	Output enable time to low level	$R_{L}=667 \Omega$, $C_{L}=45pF$ (Note 3)		20	38	ns
t _{PHZ}	Output disable time to high level	$R_1 = 667 \Omega$, $C_1 = 5pF$ (Note 3)		22	30	ns
t _{PLZ}	Output disable time to low level	IL-00/x, OL-3pr (Note 3)		17	38	ns

Note 3. Measurement circuit



Parameter	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

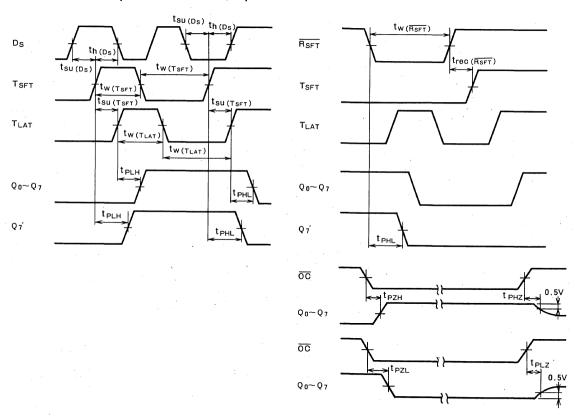
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{P,P}$, $Z_O = 50$ ohms.
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns).
 (3) C_L includes probe and jig capacitance.



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

	D			Limits		11.14
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw (Tsft)	Shift clock input pulse width		25	22		ns
tw(TLAT)	Latch clock input pulse width		20	12		ns
tw(RSFT)	Shift register reset pulse width	,	20	10		ns
t _{su(Ds)}	Setup time D _s to T _{SFT}		20	12		ns
t _{h (Ds)}	Hold time D _s to T _{SFT}		2	-1		ns
trec(RSFT)	Recovery time R _{SFT} to T _{SFT}	·	20	12		ns
t _{Su (TSFT)}	Setup time T _{SFT} to T _{LAT}	·	40	12		ns



DESCRIPTION

The M74LS596P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with an open collector output latch.

FFATURES

- 8-bit serial in parallel out shift register with latch.
- Shift register has direct reset (RSFT)
- Independent clock input pins (T_{SET}, T_{LAT})
- Open-collector, high fan-out outputs $(Q_0 \sim Q_7)$ $(I_n = 24mA)$
- Cascade output pin provided (Q'₇)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATIONS

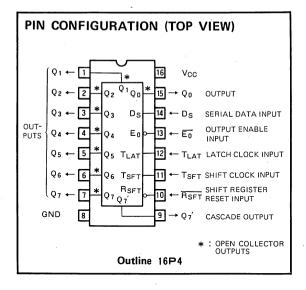
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops Separate clocks are used for shifting and latching.

The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high.

Serial data input D_s is the data input of the first stage shift register and when it is high and the pulse is applied to T_{SFT} , the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT} , the low signal enters a shift register in sequence.

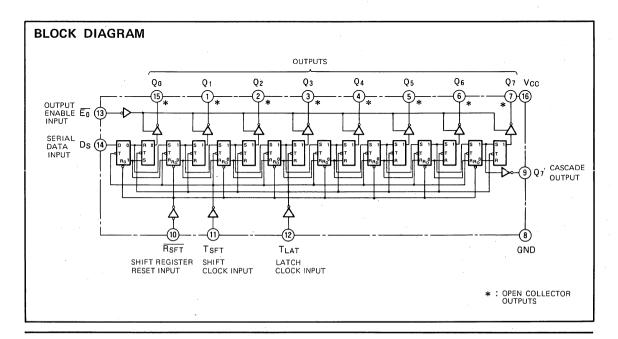


When a pulse is applied to T_{LAT} , the contents of the shift register are stored in the latch register and appear at $Q_0 \sim Q_7$. $Q_0 \sim Q_7$ are open collector outputs with buffers.

Cascade output \mathbf{Q}_7 ' at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.

When shift register reset input $\overline{R_{SFT}}$ is set low, the shift



register and Q_7' are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output enable input $\overline{E_0}$, $Q_0 \sim Q_7$ are set high but Q_7 does not change. $\overline{E_0}$ status changes have no effect on the shift operation.

FUNCTION TABLE (Note 1)

_ 1 .				Input		,			(Open colle	ctor outpu	ıt .			Cascade
Operatir	ng mode	RSFT	T _{SFT}	TLAT	Ds	Εo	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	output Q'7
	Shift t ₁	L	×	Х	Х	L	Q_0^0	Q ₁ 0	Q_2^0	Q ₃ ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Q ₇ 0	L
Reset	Latch t ₂	Х	Х	1	. X	L	L	L	L	L	L	L	L	L	L
	Shift t ₁	Н	1	X	Н	L	Q_0^0	Q ₁ 0	Q ₂ ⁰	Q ₃ 0	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Q ₇ 0	96 ⁰
Shift/latch	Latch t ₂	н	Х	1	Х	L	Н	90 ⁰	q 1 ⁰	92 ⁰	93 ⁰	94 ⁰	950	96 ⁰	96 ⁰
operation	Shift t ₁	н	1	Х	L.	L	Q_0^0	Q 1 ⁰	Q2 ⁰	Q ₃ ⁰	Q ₄ ⁰	Q ₅ 0	Q ₆ ⁰	Q ₇ 0	96 ⁰
	Latch t ₂	н	Х	1	Х	L	L	90 ⁰	91 ⁰	92 ⁰	93 ⁰	94 ⁰	95 ⁰	96 ⁰	q ⁰ 6
Output disab	ile	Х	Х	. X	· X	Н	Н	Н	Н	Н	Н	Н	Н	Н	q ₇

Note . ↑: transition from low to high level (positive edged trigger)

Q0: level of Q before the indicated steady-state input conditions were established

X : irrelevant

q0: contents of shift register before T_{SFT} is applied

q: shift register contents

t 1, t 2: t2 is set after t1 has been set

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Para	ameter	Conditions	Limits	· Unit
Vcc	Supply voltage			-0.5~+7	V.
V ₁	Input voltage	•		-0.5~+15	V
	Output voltage	Q0~Q7	Her to the second second	-0.5~+7	V
V ₀	Output voltage	Qi	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient	temperature range		-20~+75	°C
Tstq	. Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Cumbal		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	11-14				
Vcc		rarameter		Min	Тур	Max	Unit
Vcc			4.75	5	5.25	V	
High-I	High-level output	Q0~Q7	V ₀ =5.5V	0	,	100	μΑ
ТОН	Current	Q7	V _{OH} ≥2.7V	0		-400	μΑ
			V _{OL} ≤0.4V	0		12	mÀ
	Low-level output	Q0~Q7	V _{OL} ≤0.5V	0		. 24	mA
loL ,	current		V _{OL} ≤0.4V	0		. 4	mA
		Q ₇	V _{OL} ≤0.5V	0		8	. mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

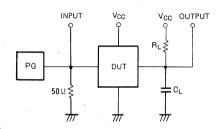
C	Deservator		T	. 1925		Limits		Unit
Symbol	Parameter	raidification		Test conditions		Тур	Max	Unit
VIH	High-level input voltage			-	2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	—18mA			-1.5	V
Vон	High-level output voltage	Q ₇	V _{CC} =4.75V, V _I =0.8V, V _I =2V, I _{OH} =-400 μA		2.7	3.4		٧
I _{OH}	High-level output voltage	Q ₀ ~Q ₇	V _{CC} =4.75V, V _I =0 V _I =2V, V _O =5.5V	.8V,			100	μΑ
VoL		0 - 0	Vcc=4.75V	I _{OL} =12mA		0.25	0.4	V
	Low-level output voltage	Q ₀ ~Q ₇	V _{CC} =4.75V V ₁ =0.8V	I _{OL} =24mA		0.35	0.5	V
	Cow-level output voltage	Qi	$V_1 = 2V$	I _{OL} =4mA		0.25	0.4	V
				I _{OL} =8mA		0.35	0.5	V
			Voc=5 25V	V ₁ =2.7V			20	μΑ
I _{IH}	High-level input current			V _I =10V			0.1	mA
1		Ds	Vcc=5.25V, Vi=0	4)/			-0.4	mA
l _{IL}	Low-level input current	Input except Ds	VCC=5.25V, VI=U	.4 V			-0.2	mA
los	Short-circuit output current (Note 2)	Q ₁	V _{CC} =5.25V, V _O =	DV	-20		-100	mA
Гссн	High-level supply current		V _{CC} =5.25V, V _I =0	IV, V₁=4.5V				mA
IccL	Low-level supply current		V _{CC} =5.25V, V _I =0	IV, V _I =4.5V				mA
locz	Off-state supply current		V _{CC} =5.25V, V _I =0	IV, V _I =4.5V				mA

^{* :} All values are at V_{CC}=5V, T_a=25°C

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Complete	D	Test conditions		Limits		Unit
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
f _{max}	Maximum repeat frequency from imput T _{SFT} to output Q' ₇		20	25		MHz
t _{PLH}	Low-to-high, high-to-low output propagation time, from			16	21	ns
t _{PHL}	at T _{SFT} to output Q' ₇	$R_L=2k\Omega$, $C_L=15pF$ (Note 3)		12	30	113
t _{PHL}	High-to-low output propagation time from input $\overline{R_{SFT}}$ to output O'_7			19	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from	,		24	42	
t _{PHL}	input T_{LAT} to outputs $Q_0 - Q_7$	B667.0. C455.5. (No. 2)		23	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from	$R_L=667 \Omega$, $C_L=45pF$ (Note 3)		30	60	20
t _{PHL}	input $\overline{E_0}$ to output $Q_0 - Q_9$			12	38	ns

Note 3. Measurement circuit

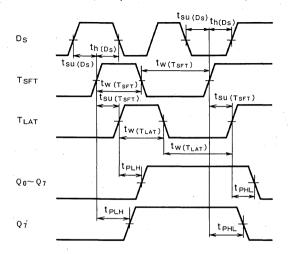


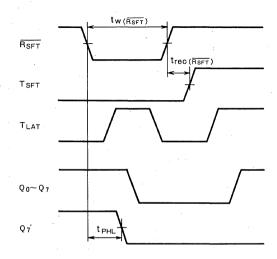
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r fins, t_f = fins, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50 ohms.
- (2) C_L includes probe and jig capacitance.

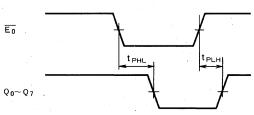
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

TIMING REQUIREMENTS (V_{CC}=5V, Ta = 25°C, unless otherwise noted)

Symbol	Dans	T		Limits		
Symbol	rarameter	ck input pulse width ister reset pulse width ie D _s to T _{SFT} e D _s to T _{SFT}	Min	Тур .	Max	Unit
tw(TsfT)	Shift clock input pulse width		25	22		ns
tw(TLAT)	Latch clock input pulse width	,	20	12		ns
tw(R _{SFT})	Shift register reset pulse width		20	9		ns
t _{su (Ds)}	Setup time D _s to T _{SFT}	-	20	12		ns
th (Ds)	Hold time D _s to T _{SFT}	·	2	-1		ns
trec(R _{SFT})	Recovery time R _{SFT} to T _{SFT}		. 20	12		ns
t _{su(TsfT)}	Setup time T _{SFT} to T _{LAT}		40	12		ns







DESCRIPTION

The M74LS620P is a semiconductor integrated circuit containing an octal bus transmitter/receiver with a tri-state inverted output.

FEATURES

- Two 8-bit data trains can be transmitted bidirectionally or as unidirectional pulses
- Input/output A and output/input B each exhibit hysteresis characteristics (Hysteresis width = 400mV typ)
- High fan-out capability (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment

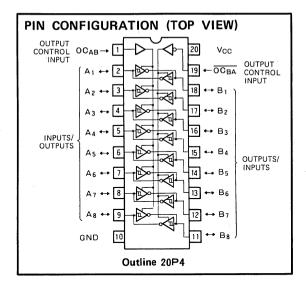
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

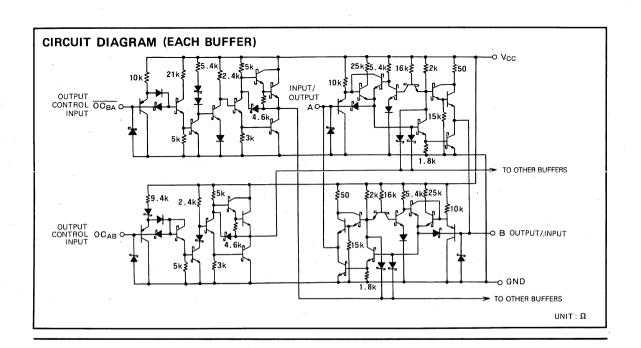
The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin.

The input/output direction is controlled by OC_{AB} and $\overline{\text{OC}_{\text{BA}}}.$

When OC_{AB} and $\overline{OC_{BA}}$ are high, A becomes the input pin, with output obtained at pin B. Conversely, when OC_{AB} are $\overline{OC_{BA}}$ are low, B is the input and A is the output.



A high impedance status is initiated at both pin A and B when OC_{AB} is low and $\overline{OC_{BA}}$ is high, isolating A from B. Precautions should be taken to guard against OC_{AB} being at a high while $\overline{OC_{BA}}$ is low. This condition will result in output from both A and B, and could result in the IC being destroyed.



FUNCTION TABLE (Note 1)

OCBA	OCAB	Α	В
L	L	0	1
Н	н	1	0
Н	L	Z	Z
L	Н	*	*

Note 1, 1 : Input pin

O: Output pin

Z: High-impedance (A and B isolated)

*: Inhibit (No output from either A or B)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
.,	1	A, B		-0.5~+5.5	٧
Vı	Input voltage OCAB, O	OCAB, OCBA		-0.5~+15	V
Vo	Output voltage		Off-state	-0.5~+5.5	V
Topr .	Operating free-air ambie	nt temperature range		-20~+75	°C
Tstg	Storage temperature range	ge		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits	Unit	
Symbol	Parame	Min Typ	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V
	IOH High-level output current	V _{OH} ≥2.4V	0		-3	mA ·
Гон .	High-level output current	V _{OH} ≥2V	0		-15	mA
	1 - 1 - 1 - 1 - 1	V _{OL} ≤0.4V	0		12	mΑ
OL	Low-level output current	V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

	Paramete					Limits		
Symbol	raramete	- Unamotor		Test conditions		Тур 🗱	Max	Unit
V _{IH}	High-level input voltage	:			2			٧
VIL	Low-level input voltage						0.6	· V
V _{T+} V _T	Hysteresis width	lysteresis width			0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V .
.,	. High-level output voltage	*	V _{CC} =4.75V	. I _{OH} =-3mA	2.4	3.4		٧
V _{OH}	This is to the control of the contro		$V_1=0.6V, V_1=2V$	I _{OH} = -15mA	2			· V
V-	Low level output voltage	ow-level output voltage		I _{OL} =12mA		0.25	0.4	٧
VoL Low-level output voltage	Low-level output voltage		V _I =0.6V, V _I =2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output curr	Off-state high-level output current		$V_1 = 2V, V_0 = 2.7V$	-		20	μΑ
lozL	Off-state low-level output curre	ent	V _{CC} =5.25V, V _I =0.6V,	$V_1 = 2V, V_0 = 0.4V$			-400	μА
		A, B	V - 5 05V V 0 7	.,			20	μΑ
1	High-level input current	OCBA, OCAB	$V_{CC}=5.25V, V_{I}=2.7V$				20	μΑ
-tim-	riigir level input current	A, B	V _{CC} =5.25V, V _I =5.5	V	•	-	0.1	mA
		OCBA, OCAB	V _{CC} =5.25V, V _I =10V				0.1	mA
HL	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	mΑ
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		-40		- 225	mA,
Гссн	Supply current, all outputs hig	h .	V _{CC} =5.25V, V _I =0V,	V ₁ =4.5V		48	70	mΑ
ICCL	Supply current, all outputs lov		V _{CC} =5.25V, V _I =0V,	V _I =4.5V		62	90	∨ mA
Iccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V,	V _I =4.5V		64	95	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

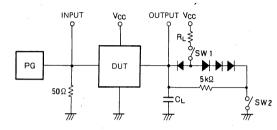


Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

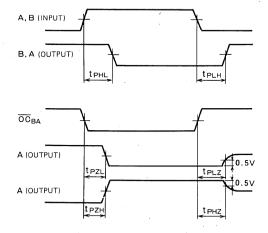
Symbol		arameter	Tost conditions		Limits		Unit
Symbol	, ,	arameter	Test conditions	Min	Тур	Max	
tpLH	Low-to-high-level output	From input A to output B			8	10	
LPLH	propagation time	From input B to output A	C ₁ = 45pF (Note 3)		8	10	ns
t	High-to-low level output	From input A to output B			12	15	ns
t _{PHL}	propagation time	From input B to output A			12	15	
+	Output enable time to low-level	From input OCBA to output A	D 0070 0 45-5 W 0		25	40	ns
t _{PZL}		From input OCAB to output B			25	40	
+	Output enable time to	From input OCBA to output A	$R_L=667 \Omega$, $C_L=45pF$ (Note 3)		23	40	
t _{PZH}	high-level	From input OCAB to output B			23	40	ns
+	Output disable time from	From input OCBA to output A			17	25	
t _{PLZ}	PLZ low-level	From input OCAB to output B			17	25	ns
	Output disable time from	From input OCBA to output A	$R_{\perp}=667 \Omega$, $C_{\perp}=5pF$ (Note 3)		19	25	ns
t _{PHZ}	high-level	From input OCAB to output B			19	25	

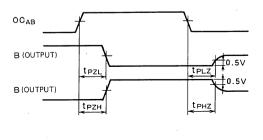
Note 3: Measurement Circuit



Paramete	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_P, P, Z_O = 50Ω.
 (2) All diodes have high-speed switching characteristics.
- (2) All diodes have high-speed switching characteristics (t_{rr} ≤ 4ns)
- (3) C₁ includes probe and jig capacitance.





DESCRIPTION

The M74LS640P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{O1} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

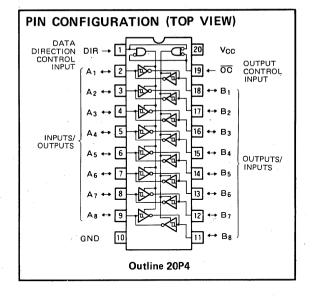
FUNCTIONAL DESCRIPTION

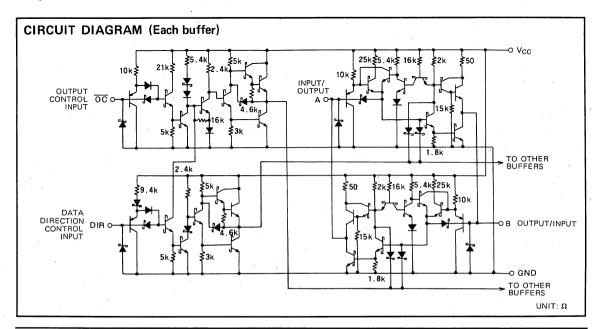
The inputs and outputs of the two buffer circuits with 3-state inverted outputs are connected together to form bidirectional buffers. Having hysteresis characteristics in the input section of input/output A and output/input B, noise margin is high.

The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal and when DIR is low, A is the output terminal and B is the input terminal.

When the output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.

A device, M74LS640-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.





FUNCTION TABLE (Note 1)

ōō	DIR	Α	В
L	L	ō	1
L	Н	1	ō
Н	×	Z	Z

Note 1:

I: Input pin

O: Output (inverted output) pin

Z: High impedance (A and B separated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \circ$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
.,	Input voltage A, B DIR, OC	A, B		-0.5~+5.5	V
VI		DIR, OC		-0.5~+15	V
Vo	Output voltage		Off state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range			-20~+75	°C
Tstg	Storage temperature ran	nge		−65~+150	°c

RECOMMENDED OPERATING CONDITIONS (Ta=-20~+75℃, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	raramen	rarameter		Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	V	
1	High-level output current	V _{OH} ≥2.4V	0		-3	mA	
Тон		V _{0H} ≧2V	0		-15	mA	
1	Low-level output current	V _{OL} ≤0.4V	0		12	mA	
IOL		V ₀ L≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = −20~+75°C, unless otherwise noted)

0	Parameter		Test conditions		Limits			
Symbol			i est cono	lest conditions		Тур*	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.6	V
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
			V _{CC} =4.75V	I _{OH} = - 3 mA	2.4	3.4		V
Vон	High-level output voltage		$V_{i}=0.6V, V_{i}=2V$	I _{OH} = - 15mA	. 2			V
VoL	Low-level output voltage		V _{CC} =4.75V			0.25	0.4	V
VOL	Low-level output voltage		V _I =0.6V, V _I =2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_{I} = 0.6V, V_{I} = 2V, V_{O} = 2.7V$				20	μA
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V	, V _I =2V, V ₀ =0.4V			-400	μА
		A, B	V 5 05V V 0 7V				20	μА
	High-level input current	DIR, OC	$V_{CC}=5.25V, V_{I}=2.7$	· V			20	μА
Iн	rigit-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
	DIR, Ō		V _{CC} =5.25V, V _I =10\	/			0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	IV			-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V · V _O =0\	,	40		-225	mA
Icch	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		48	70	mA
Iccl	Supply current, all outpus low		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		62	90	mΑ
I _{CCZ}	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		64	95	mA

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

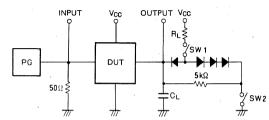
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter		T	Limits			11-11
Symbol			Test conditions	Min	Тур	Max	Unit
	Low-to-high level output	From input A to output B	-		- 8	10	
tpLH	propagation time	From input B to output A	0 45-5 (2)		8	10	ns ·
t _	High-to-low level output	From input A to output B	C _L =45pF (Note 3)		12	15	
t _{PHL}	propagation time	From input B to output A	,		12	.15	ns
		From input OC to output A			25	. 40	ns
t _{PZL}	Low output enable time	From input OC to output B	$R_L = 667\Omega$ $C_L = 45pF$		25	40	1115
	High output enable time	From input OC to output A	(Note 3)		23	40	
tpzh	riigii output enable time	From input OC to output B			23	40	ns
	Laurantan et la re	From input OC to output A			17	25	
tpLZ	Low output disable time	From input OC to output B	$R_L = 667\Omega$ $C_L = 5pF$		17	25	ns
. Ulah autaut	High output disable time	From input OC to output A	(Note 3)		19	25	
t _{PHZ}	migh output disable time	From input OC to output B			19	. 25	ns

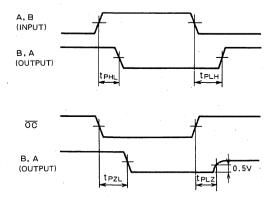
Note 3: Measurement circuit

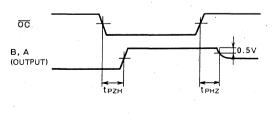


Parameter	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_P,P, Z_O = 50Ω

 (2) All diodes are high speed switching diodes
- $(t_{rr} \le 4ns)$. CL includes probe and jig capacitance.





M74LS640-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS640-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = -15mA)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

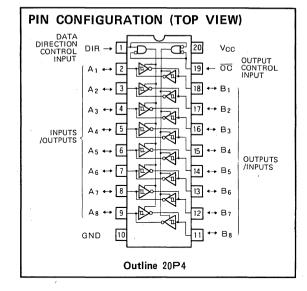
General purpose, for use in industrial and consumer equipment,

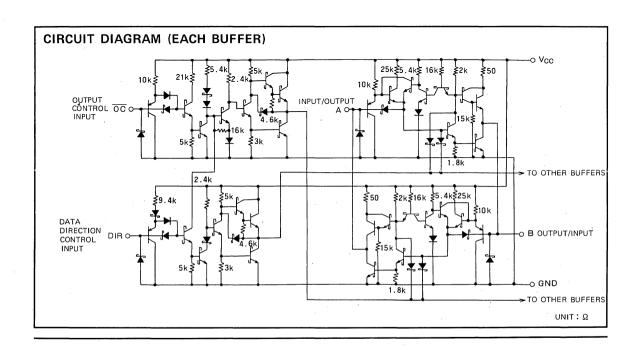
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	ō	ı
L	Н	1	ō
. н	X	Z	Z

Note 1: I : Input pin
O ! Output (inverted) pin

Z: High-impedance (A, B isolated)
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V _{CC}	Supply voltage			-0.5~+7	٧
.,	1	A, B		-0.5~+5.5	٧
V _I	Input voltage	DIR, OC		-0.5~+15	٧
Vo	Output voltage		Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		- 1	-20~+75	°C
Tstg	Storage temperature range			−65∼+150	ొ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Cumbal	Symbol Parameter			11.5		
Symbol			Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	٧
1	IOH High-level output current	V _{OH} ≥2.4V	0		-3	mA ·
ТОН		V _{0H} ≧2V	0		—15	mA
1	Low-level output current	V ₀ L≦0.4V	0		12	mA
IOL		V _{OL} ≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal	Parameter		Test conditions		Limits			
Symbol					Min	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage				2			٧
VIL	Low-level input voltage						0.6	V
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V	High-level output voltage		V _{CC} =4.75V	I _{OH} = - 3 mA	2.4	3.4		V
Vон	rigit-level output voltage		V _I =0.6V, V _I =2V	I _{OH} = - 15mA	2			V
	Low-level output voltage		V _{CC} =4.75V V _I =0.6V, V _I =2V	I _{OL} =12mA		0.25	0.4	٧
VoL				I _{OL} =24mA		0.35	0.5	V
				I _{OL} =48mA		0.4	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V	$V_1 = 2V_1 V_0 = 2.7V$			20	μA
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V	', V _I =2V, V _O =0.4V	•		-400	μА
	High-level input current	A, B	V _{CC} =5.25V, V _I =2.7V				- 20	μА
Luci		DIR, OC					20	μА
Iн	riigii-level iiiput current	A, B	V _{CC} =5.25V, V _I =5.5	5V	-		0.1	mA
	٠	DIR, OC	V _{CC} =5.25V, V _I =10\	V			0.1	mA
IIL	Low-level input current		V _{CC} =5.25V, V _I =0.4	4V			-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V . V _O =0\	/	-40		- 225	mA
Госн	Supply current, all outputs high V _{CC} =5.25V, V _I =0V, V _I =4.5V		, V _I =4.5V		48	70	mA	
ICCL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V, V _I =4.5V			62	90	mA
Iccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	', V _I =4.5V	`	64	95	mA

^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

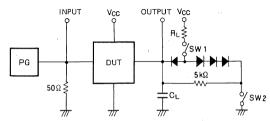
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

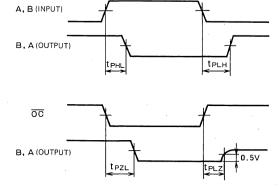
Symbol	Parameter		Test conditions	Limits			11-14
Syllibol	ratame	iter .	l est conditions	Min Typ Max		Unit	
t _{PLH}	Low-to-high-level	From input A to output B			8	10	ns
PLH	output propagation time	From input B to output A	0 -4505 (Nov. 2)		8	10	113
	High-to-low level	From input A to output B	C _L =45pF (Note 3)		12	15	
t _{PHL}	output propagation time	From input B to output A			12	15	ns
	Loudoud autout anable time	From input OC to output A			• 25	40	ns
t _{PZL}	Low-level output enable time	From input OC to output B			25	40	113
	High-level output enable time	From input OC to output A	$R_{\perp} = 667\Omega$ $C_{\perp} = 45 pF$ (Note 3)		23	40	ns
t _{PZH}	High-level output erlable time	From input OC to output B			23	40	115
	Low-level output disable time	From input OC to outputA			17	25	ns
t _{PLZ}	Low-level output disable time	From input OC to output B	$R_{\perp} = 667\Omega$ $C_{\parallel} = 5pF$ (Note 3)		17	25	115
	High-level output disable time	From input OC to output A	NL = 667% CL = 5pF (Note 3)		19	25	nc
t _{PHZ}		From input OC to output B			19	25	ns

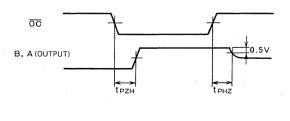
Note 3: Measurement circuit



Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) All diodes are switching diodes ($t_{rr} \le 4ns$).
- (3) C_L includes probe and jig capacitance.





OCTAL RUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted open collector outputs.

FFATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (IOL = 24mA)
- Wide operating temperature range. (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

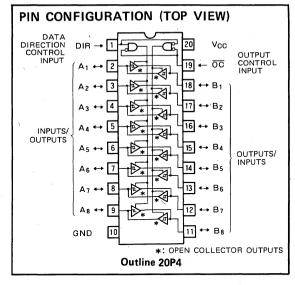
FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

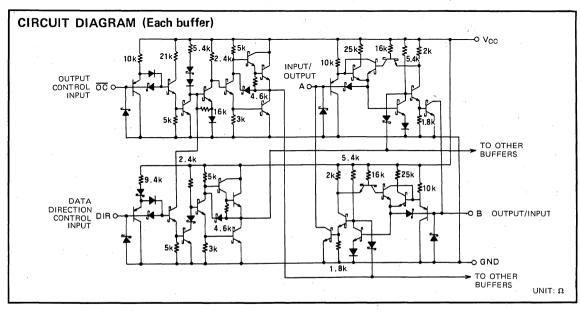
When DIR is high, A is the input pin and B is the output pin. When DIR is low then B is input terminal and A is the output terminal. When output control input OC is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

The functions and pin connections of this IC are identical to those of M74LS645P.



A device, M74LS641-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

FUNCTION TABLE (Note 1)

ÖC	DIR	А	В
L	L	0	1
L	Н	1	0
н.	X	Н	Н

Note 1: I: Input pin

O: Output (non-inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
V _{CC}	Supply voltage			-0.5~+7	, v
.,.	Input veltore	A, B		-0.5~+7	V
VI	Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		High-level state	-0.5~+7	V
Topr	Operating free-air ambi	ent temperature range		-20~+75	°
Tstg	Storage temperature rai	nge		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-20~+75℃, unless otherwise noted)

Complete	Parameter			11-11		
Symbol	raran	neter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
loH	High-level output current	V ₀ =5.5V	0		100	μА
	1 11	V _O L≦0.4V	0		12	mA
IOL	IOL Low-level output current	V _O L≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramete	-	Test cond	litions		Limits		Unit
Symbol	raiamete		l est conc		Min	Typ *	Max	Onit
V _{IH}	High-level input voltage				2			٧
VIL	Low-level input voltage						0.6	٧
V _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	I8mA			- 1.5	٧
Іон	High-level output current	,	V _{CC} =4.75V, V _I =0.6V, V	'ı'=2V, V ₀ =5.5V			100	μΑ
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_i=0.6V, V_i=2V$ $I_{OL}=24 \text{ mA}$				0.35	0.5	V
		А, В	V 5 05V V - 2 7				20	μА
	Lish lovel is not some	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.7$	V			20	μΑ
Iн	High-level input current	А, В	V _{CC} =5.25V, V _I =5.5	V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10V	, ·			0.1	mA
l _{IL}	Low-level input current	Low-level input current		V			-0.4	mA
Іссн	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V,	. V _I = 4.5V		48	70	mA
ICCL	Supply current, all outputs lo	utputs low $V_{CC}=5.25V, V_I=0V, V_I=4.5V$			62	90	mA	
locz	Supply current, all outputs o	ff	V _{CC} =5.25V, V _I =0V,	, V ₁ =4.5V		64	95	mA

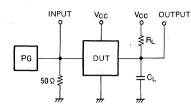
^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

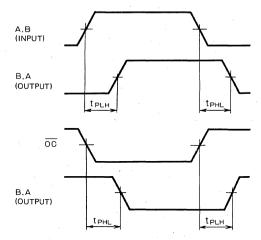
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol		ameter	Test conditions		Limits			Unit	
Symbol	ran	ameter	rest conditions		Min	Тур	Max	Unit	
	Low-to-high level output propagation time From input A to output B From input B to output A	From input A to output B				20	25		
t _{PLH}			20	25	ns				
	High-to-low level output	From input A to output B		Γ		15	25		
t _{PHL}	propagation time	From input B to output A	0 45-5 0 6570 (N-4-3)	0 -45-5 B -667.0 (Not	- CC7 O (Note 2)		15	25	ns
	Low-to-high level output	From input OC to output A	$C_{L}=45pF, R_{L}=667 \Omega$ (No	ote 21		25	40		
t _{PLH}	propagation time	From input OC to output B		T		25	40	ns	
	High-to-low level output	From input OC to output A	·			30	50		
t _{PHL}	propagation time	From input OC to output B		Γ		30	· 50	ns	

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_g = 500ns, V_P = 3 V_P , Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.



M74LS641-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output
 A and output/input B
- High fan-out (I_{O1} = 48mA)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

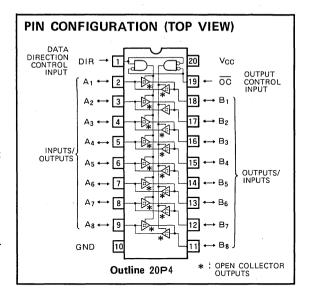
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector non-inverted outputs are made two-way buffers.

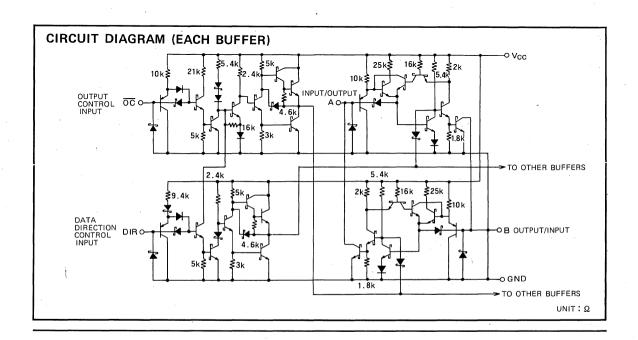
The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input \overline{OC} is high,



both A and B go to high and are isolated.

The functions and pin connections of this device are identical to those of M74LS645-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

FUNCTION TABLE (Note 1)

ŌĊ	DIR	, А	В
L	L	0	1
L	Н	1	0
Н	Χ .	Н	н

Note 1: | : Input pin

O: Output (non-inverted) pin

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75℃, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
		A, B		-0.5~+7	V
. V _I	Input voltage	DIR, OC	·	$-0.5 \sim +15$	- V
Vo	Output voltage	- It	High-level state	$-0.5 \sim +7$	V
Topr	Operating free-air ambien	t temperature range		-20~+75	ı °C
Tstg	Storage temperature rang	9		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

				Limits		
Symbol	Paramet	rarameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μΑ
1	Low-level output current	V _{OL} ≤0.4V	0		12	mΑ
IOL	Low-level output current	V ₀ L≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

C	Parameter		Test conditions		Limits			Unit
Symbol	Paramete	3F -	l est cond	itions	Min	Typ *	Max	Onit
V _{IH}	High-level input voltage		1,		2			V
VIL	Low-level input voltage						0.6	٧
V _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
·Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18 mA			-1.5	٧
Іон	High-level output current		V _{CC} =4.75V, V _I =0.6V,	V _I =2V, V ₀ =5.5V			100	μΑ
			4 751	I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage		V _{CC} =4.75V V _I =0.6, V _I =2V	I _{OL} =24mA		0.35	0.5	٧
				I _{OL} =48mA		0.4	0.5	V
		A, B		714			20	μΑ
	Ulah tauat ianah aurana	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.$, / V			20	μΑ
Iн	High-level input current	A, B	V _{CC} =5.25V, V _I =5.	.5V			0.1	mA
·		DIR, OC	$V_{CC} = 5.25V, V_I = 10V$				0.1	mA
IIL	Low-level input current		V _{CC} =5.25V, V _I =0	.4V			-0.4	· mA
Іссн	Supply current, all outputs high		V _{CC} =5.25V, V _I =0	V,. VI = 4.5V		48	70	mΑ
ICCL	Supply current, all outputs low	•	V _{CC} =5.25V, V _I =0	V, V _I = 4.5V		62	90	mΑ
lccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0	$V, V_1 = 4.5V$		64	95	mA.

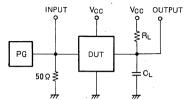
^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25°C

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

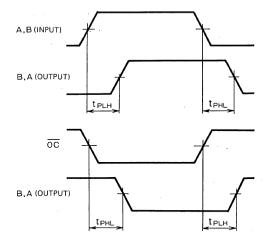
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Param		Test conditions	Limits			Unit
Symbol	Param	eter	l est conditions	Min	Тур	Max	Unit
•	Low-to-high-level output	From input A to output B	,		20	25	ns
t _{PLH}	propagation time	From input B to output A		20	25	115	
•	High-to-low level output From input A to output B propagation time From input B to output A			15	25	ns	
t _{PHL}		From input B to output A	0 17 7 7 0 00 0 (No. 12 0)		15	25	"5
+	Low-to-high level output	From input OC to output A	C _L =45pF, R _L =667 Ω (Note 2)		25	40	ns
t _{PLH}		From input OC to output B			25	40	115
+	g to lott lottel output	From input OC to output A			30	50	ne
t _{PHL}	propagation time From input OC to outp				30	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_o = 50Ω .
- (2) C_L includes probe and jig capacitance.



OCTAL RUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74LS642P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (IOI = 24mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

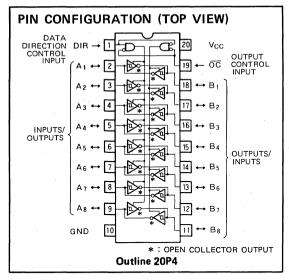
FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with inverted output open collectors are connected together to form bi-directional buffers.

The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

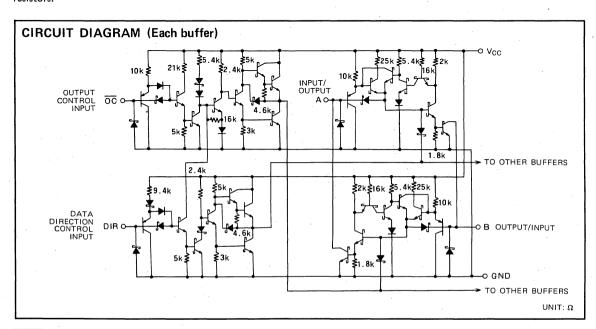
When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input \overline{OC} is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.



The functions and pin connections of this IC are identical to those of M74LS640P.

A device, M74LS642-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	ō	ı
L	Н	· 1	ō
Н	X	Н	н

Note 1: I: Input pin

O: Output (inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
.,		A, B		-0.5~+7	V
VI	Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		High-level state	-0.5~+7	V
Topr	Operating free-air ambie	ent temperature range		-20~+75	℃
Tstg	Storage temperature ran	nge		-65~+150	င

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

C	Parameter			Limits			
Symbol	raidi	T diditions.			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V ₀ =5.5V	0		100	μА	
	IOL Low-level output current	V _{OL} ≤0.4V	0		12	mA	
IOL		V _{OL} ≤0.5V	0		24	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramet	or.	Test cond	litions		Limits		11-14
Symbol	Faramet	ei	. rest cond	ittions	Min	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	18 mA			- 1.5	V
Гон	High-level output current		V _{CC} = 4.75V, V _I = 0.6V,	V _I = 2 V, V _{OH} = 5.5 V	1		100	μΑ
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
VOL	Low-level output voltage		V _I =0.6V, V _I =2V	I _{OL} =24 mA		0.35	0.5	V
		A, B					20	μΑ
L	Little Investigance accesses	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.5$	$V_{CC} = 5.25V, V_1 = 2.7V$			20	μΑ
Iн	High-level input current	А, В	V _{CC} =5.25V, V _I =5.5	5V			0.1	mΑ
		DIR, OC	V _{CC} =5.25V, V _I =10	V			0.1	mΑ
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	4∨			-0.4	mA ·
Іссн	Supply current, all outputs h	igh	V _{CC} =5.25V, V _I =0V	, V _i = 4.5V		48	70	mA
ICCL	Supply current, all outputs to	ow .	V _{CC} =5.25V, V _I =0V	, V _I = 4 . 5V		62	90	mΑ
Iccz	Supply current, all outputs o	ff	V _{CC} =5.25V, V _I =0V	, V ₁ =4.5V		64	95	mA

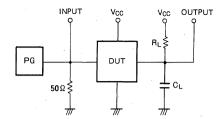
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25$ °C.

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

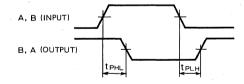
SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C, unless otherwise noted)

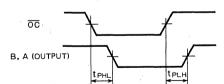
Symbol	Por	ameter	Test conditions	Limits			Unit	
Зуппрог	rai		rest conditions	Min	Тур	Max	Onit	
t PLH Low-to-high level output	From input A to output B			16	25			
' PLH	propagation time	From input B to output A			16	25	ns	
+	High-to-low level output propagation time	From input A to output B	C _L =45pF, R _L =667 Ω		14	25	ns ns	
PHL		From input B to output A			14	25		
+	Low-to-high level output	From input OC to output A	(Note 2)		25	40		
t _{PLH}	PLH propagation time	From input OC to output B	(Note 2)		25	40		
t	High-to-low level output From input OC to output A				30 .	60		
t PHL propagation time		From input OC to output B			30	60	ns	

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_W = 500ns, V_P = 3 V_P , Z_O = 50 Ω
- (2) CL includes probe and jig capacitance.





M74LS642-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74LS642-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{O L} = 48mA)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

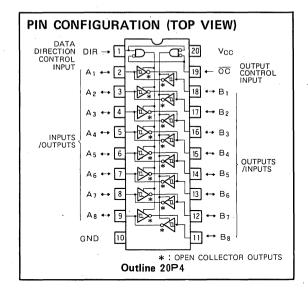
General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

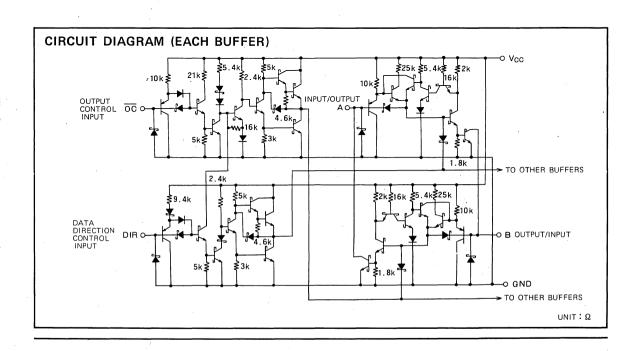
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector inverted outputs are made two-way buffers.

The input/output A and output/input B sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are high and A and B are isolated.



The functions and pin connections of this device are identical to those of M74LS640-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

ōc	DIR	А	В
L	L	ō	· I
L	H.	1	ō
н	X	н	Н

Note 1: | : Input pin

Output (inverted) pin

X : Irrelevant

MAXIMUM ABSOLUTE RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Pa	rameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	٧
.,		A, B		-0.5~+7	٧
Vı	Input voltage	DIR, OC		-0.5~+15	٧
Vo	Output voltage		High-level state	-0.5~+7	٧
Topr	Operating free-air ambie	ent temperature range		-20~+75	င
Tstg	Storage temperature ran	ige		−65~+150	. °C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol Parameter VCC Supply voltage			Unit			
Symbol	Para	raiametei		Тур	Max	Oille
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V ₀ =5.5V	0		100	μΑ
	V _{OL} ≤0.4V	0		12	mA	
IOL	IOL Low-level output current	V _{OL} ≤0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted)

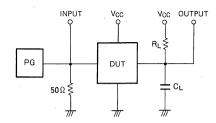
Symbol	Paramet	meter Test conditions				Limits		Unit
Symbol	raidillet	eı	rest condit	Test conditions		Typ *	Max	Oiiit
V _{IH}	High-level input voltage	High-level input voltage			2			٧ .
VIL	Low-level input voltage			- 1			0.6	· V
V _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
Vic	. Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 _, mA			- 1.5	٧
Гон	High-level output current		V _{CC} = 4.75V, V _I = 0.6V, V	$V_1 = 2V, V_0 = 5.5V$			100	μΑ
			V 4 75V 10	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage		V _{CC} =4.75V V _I =0.6V, V _I =2V	I _{OL} =24mA	: 1	0.35	0.5	٧
			VI-0.6V, VI=2V	I _{OL} =48mA		0.4	0.5	٧
		A, B	V 5 05V V 0 5	11.4			20	μΑ
	Of the formal factors accounts	DIR, OC	$V_{CC} = 5.25V, V_I = 2.7V$				20	μА
Ин	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V., V _I = 10 ³	V _{CC} =5.25V., V _I = 10V			0.1	mA
lıL	Low-level input current		V _{CC} =5.25V, V _I =0.4	1 V			-0.4	mA
Іссн	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$		48	70	mA
ICCL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		62	90	mA
Iccz	Supply current, all outputs of		V _{CC} =5.25V, V _I =0V	, V _I = 4.5V		64	95	mA

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

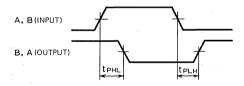
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

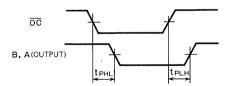
Symbol Parai		otor	Test conditions	Limits			Unit
Symbol	, rarati	eter	rest conditions	Min	Тур	Max	·
+	Low-to-high-level output	From input A to output B			16	25	ns
t _{PLH}	propagation time	From input B to output A	,		16	25	
+_	High-to-low level outpout propagation time	From input A to output B			14	25	ns
t _{PHL}		From input B to output A	0 45-5 5 007 0 (N-+-2)		14	25	"5
+	Low-to-high level output	From input OC to output A	C _L =45pF, R _L =667 Ω (Note 2)		25	40	ns
t _{PLH}	propagation time	From input OC to output B			25	40	115
• -	High-to-low-level output	From input OC to output A			30	60	
t _{PHL}	propagation time	From input OC to output B			30	60	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
 - $V_P = 3V_{P-P}, Z_0 = 50\Omega.$
- (2) CL includes probe and jig capacitance.





M74LS643P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS643P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

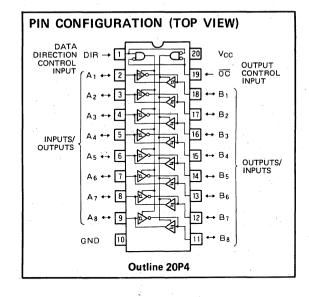
The inputs and outputs of the two buffer circuits with 3state outputs are connected together to form bi-directional buffers

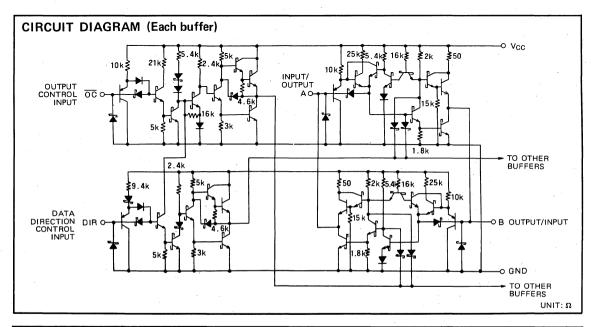
The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.

A device, M74LS643-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.





OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

ōC	DIR	Α	В
L	L	0	ı
L	Н	1	ō
Н	×	Z	Z

Note 1: I: Input pin

O: Output (non-inverted output) pin

O: Output (inverted output) pin

Z: High impedance (A, B separated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
V Input valence		A, B		-0.5~+5.5	V
VI	V _I Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		Off state	-0.5~+5.5	V
Topr	Operating free-air ambie	ent temperature range		-20~+75	ొ
Tstg	Storage temperature ran	nge		-65~+150	rc

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			11-14		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
1	I_{OH} High-level output current $V_{OH} \ge 2.4V$ $V_{OH} \ge 2.V$	V _{0H} ≥2.4V	0		-3	mA
I 'OH		0		-15	mA	
1	Low-level output current	V ₀ L≦0.4V	0		12	mA
IOL	Low-level output current	V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Test cond	litions		Limits		Unit
Symbol	Farameter		Test conditions		Min	Тур*	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.6	V
V _{T+} -V _T -	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18 mA			-1.5	
Va High level output voltage		V _{CC} =4.75V	I _{OH} = - 3 mA	2.4	3.4		V	
Уон	High-level output voltage		V _I =0.6V, V _I =2V	I _{OH} = - 15mA	2			V
			V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6\	V, V _I =2V, V ₀ =2.7V			20	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V, V _I =2V, V _O =0.4V				-400	μÀ
		A, B	\\	V 5 05W W 0 7W			20	μА
	Mak Javat Sanus	DIR, OC	$V_{CC}=5.25V, V_{I}=2.3$	/ V			20	μА
Iн	High-level input current	A, B .	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10\	/			0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	4V			-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0\	/	-40		- 225	mA
Гссн	Supply current, all outputs high	ply current, all outputs high V _{CC} =5.25V, V _I =0V, V _I =4.5V			48	70	mA	
IccL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		62	90	mA
Iccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		64	95	mA ·

*: All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

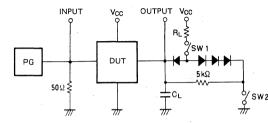


OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

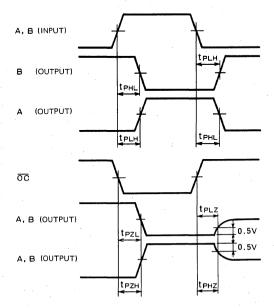
0	D.:		Too	t conditions		Limits		Unit
Symbol	Par	ameter	rest conditions		Min	Тур	Max	Unit
	Low-to-high level output	From input A to output B				8	10	
t _{PLH}	propagation time	From input B to output A	0 45-5	(1)		8	10	ns
•	High-to-low level output	From input A to output B	C _L =45pF	(Note 3)		12	15	
t _{PHL}	propagation time	From input B to output A				12	15	ns
	1 a a a b.l. a	From input OC to output A	$R_1 = 667\Omega$ $C_1 = 45pF$			25	40	ns
t _{PZL}	Low output enable time	From input OC to output B		$C_L = 45pF$		25	40	115
	High output enable time	From input OC to output A		(Note 3)		23	40	ns
t _{PZH}	nigh output enable time	From input OC to output B				23	40	,,,,
	Lour output disable time	From input OC to output A				17	25	ns
t _{PLZ}	Low output disable time	From input OC to output B	$R_L = 667\Omega$	$C_1 = 5pF$		17	25	115
	High output disable time	From input OC to output A] -	(Note 3)		. 19	25	ns
t _{PHZ}	riigii output disable time	From input OC to output B			19	25	1 "5	

Note 3: Measurement circuit



	Parameter	SW 1	SW2
	t _{PZH}	Open	Closed
	t PZL	Closed	Open
	t _{PLZ}	Closed	Closed
,	t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_F = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3Vp,p, Z_O = 50 Ω All diodes are high speed switching diodes
- (t_{rr} ≤ 4ns).
 (3) C_L includes probe and jig capacitance.



M74LS643-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS643-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out $(I_{OI} = 48mA, I_{OH} = -15mA)$
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

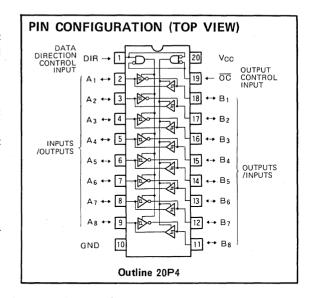
General purpose, for use in industrial and consumer equipment,

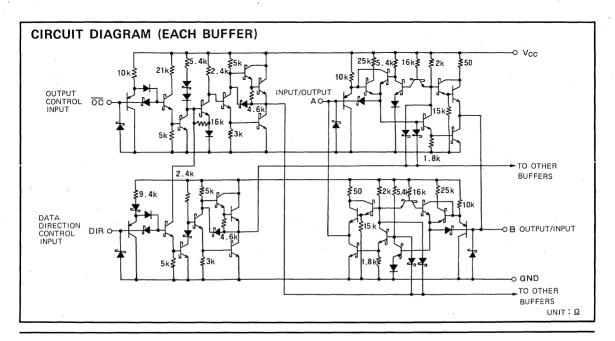
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are mutually connected and the buffers with non-inverted outputs and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	· · L	0	1
L	Н	ı	ō
Н	×	Z .	Z

Note 1: | : Input pin

O: Output (non-inverted) pin

O: Output (inverted) pin

Z: High-impedance (A, B are isolated)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter Cor		Conditions	Limits	Unit	
Vcc	Supply voltage			-0.5~+7	V	
.,	1	A, B		-0.5~+5.5	V	
VI	V _I Input voltage	input voitage	DIR, OC		$-0.5 \sim +15$	V
Vo	Output voltage		Off-state	-0.5~+5.5	V	
Topr	Operating free-air ambier	nt temperature range		-20~+75	င	
Tstg	Storage temperature rang	ge		−65∼+150	ా	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Unit			
Symbol	raiamete	Min	Тур	Max	Onit		
Vcc	Supply voltage		4.75	5	5.25	V	
1	IOH High-level output current	V _{OH} ≥2.4V	0		-3	mA	
Гон	riigh-level output current	0		-15	mA		
1			V _{OL} ≤0.4V	0		12	mA
IOL	Low-level output current VoL≤0.5V		0		48	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Cumbal	Par	ameter	Test condit	ione		Limits		Unit
Symbol	rara	ameter	rest condit	ions	Min	Typ *	Max	Onit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage	I input voltage				0.6	٧ .	
V _{T+} V _T	Hysteresis width		V _{CC} =4.75V		0.2	0.4	-	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	V
.,	High land and a release		V _{CC} =4.75V	I _{OH} = -3mA	2.4	3.4		V
Voн	OH High-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OH} = - 15mA	2			. V
			Vcc=4.75V	I _{OL} =12mA		0.25	0.4	V
V _{OL} Low-leve	Low-level output voltage	_ow-level output voltage		I _{OL} =24mA		0.35	0.5	V
			$V_i=0.6V, V_i=2V$	I _{OL} =48 mA		0.4	0.5	V
lozh	Off-state high-level output current $V_{CC} = 5.25V$, $V_1 = 0.6V$, $V_1 = 2V$, $V_0 = 2.7V$		$V_1 = 2V, V_0 = 2.7V$			20	μΑ	
lozL	Off-state low-level output	current	V _{CC} = 5.25V, V _I = 0.6V,	$V_1 = 2V, V_0 = 0.4V$			-400	μА
		A, B					20	μА
.	High-level input current	DIR, OC	$V_{CC} = 5.25V, V_i = 2.7$	V			20	μΑ
IIH	right-level input current	A, B	V _{CC} =5.25V, V _I =5.5	iV .			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I = 10 ⁴	V .			0.1	mA
lic .	Low-level input current V _{CC} =5.25V, V _I = 0.4V		V ;			-0.4	mA	
los	Short-circuit output current (Note 2) V _{CC} =5.25V, V _O = 0 V		-40		- 225	mA		
Гссн	Supply current, all outpu	ts high	$V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V$			48	70	mA
ICCL	Supply current, all outpu	its low	$V_{CC} = 5.25V, V_1 = 0 V, V_1 = 4.5V$			62	90	mA
Iccz	Supply current, all outpu	its off	V _{CC} =5.25V, V _I = 0 V	V, V _I = 4.5V		64	95	mA

^{*.:} All typical values are at V_{CC}=5V, Ta=25℃

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

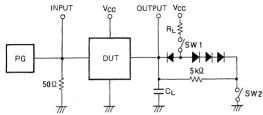


OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

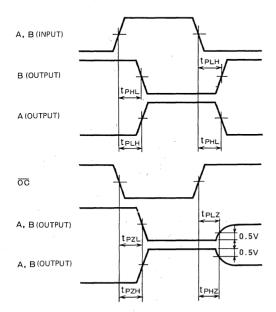
Symbol	Para	neter	Test conditions		Limits		Unit
Symbol	Fald	neter	, rest conditions	Min	Тур	Max	Unit
	Low-to-high-level output	From input A to output B			8	10	
t _{PLH}	propagation time	From input B to output A	0 45-5 (No. 2)		8	10	ns
t	High-to-low level output	From input A to output B	C _L =45pF (Note 3)		12	15	
t _{PHL}	propagation time	From input B to output A			12	15	ns
	Low-level output enable	From input OC to output A			25	40	ns
t _{PZL}	time	From input OC to output B	B 5570 0 45-5 (Note 2)		25	40	
	High-level output enable	From input OC to output A	$R_L = 667\Omega$ $C_L = 45pF$ (Note 3)		23	40	ns
t _{PZH}	time	From input OC to output B			23	40	
	Low-level output disable	From input OC to output A			17	25	ns
t _{PLZ}	time	From input OC to output B	R _L =667Ω C _L =5pF (Note 3)		. 17	25	113
	High-level output disable	From input OC to output A			19	25	ns
t _{PHZ}	time	From input OC to output B			19	25	113

Note 3: Measurement circuit



Symbol t PZH		SW 1	SW2	
	t pzh	Open	Closed	
	t PZL	Closed	Open	
	t PLZ	Closed	Closed	
ĺ	t _{PHZ}	Closed	Closed	

- (1) The pulse generator (PG) has the following characteristics:
 $$\begin{split} PRR = 1 MHz, \, t_r = 6 ns, \, t_f = 6 ns, \, t_w = 500 ns, \\ V_P = 3 V_{P,P}, \, \, Z_0 = 50 \Omega. \end{split}$$
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$.
- (3) C_L includes probe and jig capacitance.



DESCRIPTION

The M74LS644P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted, non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OI} = 24mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

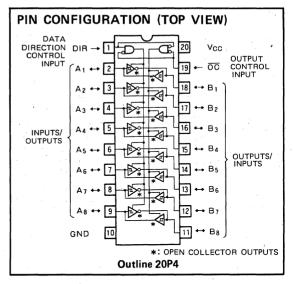
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The inputs and outputs of the buffer circuits with open collector outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

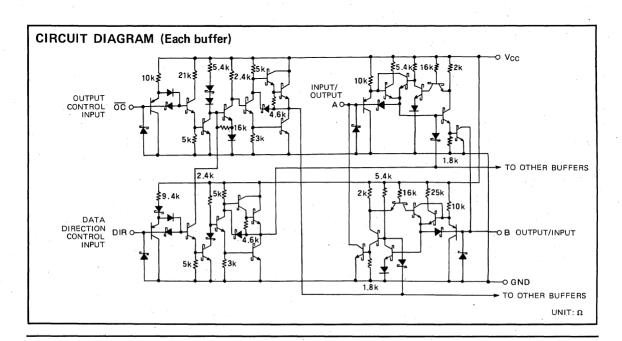
When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input \overline{OC} is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.



The functions and pin connections of this IC are identical to those of M74LS643P.

A device, M74LS644-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



FUNCTION TABLE (Note 1)

<u>oc</u>	DIR	Α	В
L	L	0	1
L	Н	ı	ō
Н	x	Н	н

Note 1: I: Input pin

O: Output (non-inverted output) pin

O: Output (inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
V _I Input voltage	A, B		-0.5~+7	V	
٧١ .	DIR, OC			0.5~+15	V
Vo	Output voltage		High-level state	-0.5~+7	V
Topr	Operating free-air ambi	ent temperature range		-20~+75	·c
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramete		Limits			
Symbol	Faramete	Tarameter			Max	Unit
Vcc	Supply voltage	4.75	5	5.25	V	
Іон	High-level output current	V ₀ =5.5V	. 0		100	μА
	Low-level output current	V ₀ L≦0.4V	. , 0		12	mA
loL	Low-level output current	V _{0L} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

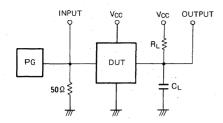
Symbol	Parameter		Test see	1141	Limits			Unit
Symbol			l est cond	Test conditions		Typ *	Max	Omt
V _{IH}	High-level output voltage				2			٧
VIL	Low-level output voltage						0.6	٧
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Гон	High-level output current		V _{CC} =4.75V, V _I =0.6V, V _I =2V, V _O =5.5V				100	μА
VoL	Low-level output voltage		V _{CC} =4.75V I _{OL} =12mA			0.25	0.4	V
VOL	Low-level output voltage	v-lever output vortage		I _{OL} =24mA		0.35	0.5	V
		A, B	V 5 05V V 0	7)./	,		20	μА
	Mish Israel issues surrous	DIR, OC	$V_{CC}=5.25V, V_{I}=2.7$	/V			20	μА
1ін	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10 ^V	V			0.1	mΑ
I _I L	Low-level input current		V _{CC} =5.25V, V _I =0.4V				-0.4	mA
Icch	Supply current, all outputs h	igh	V _{CC} =5.25V, V _I =0,V, V _I =4.5V			48	70	mA
I _{CCL}	Supply current, all outputs le	ow	V _{CC} =5.25V, V _I =0V, V _I =4.5V			62	90	mA
Iccz	Supply current, all outputs of	ff	V _{CC} =5.25V, V _I =0V, V _I =4.5V			64	95	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

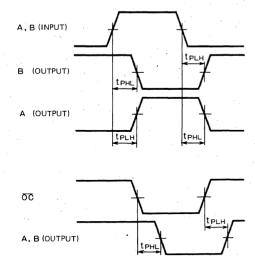
0	р.		Test conditions		Limits		Unit ns
Symbol	Par	ameter	l est conditions	Min	Тур	Max	Unit
Low-to-high level output		From input A to output B			16	25	
t PLH propagation time	From input B to output A			20	25	115	
High-to-low level output	From input A to output B			14	25		
t _{PHL}	propagation time	From input B to output A	C _L =45pF, R _L =667 Ω		15	25	ns
• _	Low-to-high level output	From input OC to output A	CL 45PF, NL 807 S2		25	40	
t _{PLH}	propagation time	From input OC to output B	(Note 2)		25	40	ns
1 -	High-to-low level output	From input OC to output A			30	60	
t _{PHL}	propagation time	From input OC to output B			30	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_P.P, Z_O = 50Ω

 (2) C_L includes probe and jig capacitance.



M74LS644-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS644-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted and non-inverted outputs.

FFATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA)
- Wide operating temperature range (T_a = −20~+75°C)

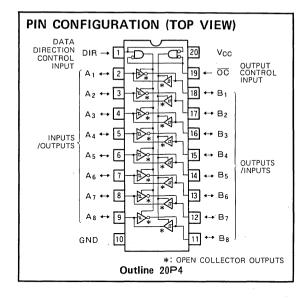
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

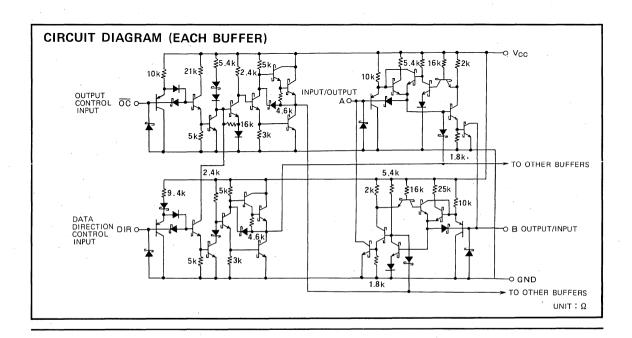
In this device the inputs and outputs are connected mutually and the buffers with open collectors inverted outputs and the buffers with the non-inverted outputs are made two-way buffers, the input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and



A the output pin. When \overline{OC} is high, both A and B are high, and A and B are isolated.

The functions and pin connections of this device are identical to those of M74LS643-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	0	1
L	Н	1	ō
Н	Х	Н	Н

Note 1: | Input pin

O: Output (non-inverted) pin
O: Output (inverted) pin

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Condit	Conditions		Unit
Vcc	Supply voltage		* 1	-0.5~+7	V	
	Input voltage	A, B			-0.5~+7	V
VI	input vortage	DIR, OC			-0.5~+15	V
Vo	Output voltage		High-level state		-0.5~+7	V
Topr	Operating free-air ambient temperature range				-20~+75	°C
Tstg	Storage temperature range			***************************************	−65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol				Limits			
Symbol	Parameter		Min	Тур	Max	Unit .	
Vcc	Supply voltage	4.75	5	5.25	V		
loH	High-level output current	V ₀ =5.5V	<i>(</i> ∙ 0		100	μА	
	1 1 1 1	V _{OL} ≤0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≦0.5V	0		48	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

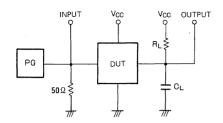
6						Limits		Unit V V V μA V V
Symbol	Paramet	er	l est co	nditions	Min	Typ *	Max	
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.6	V
V _{T+} V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	٧
Гон	High-level output current		V _{CC} =4.75V, V _I =0.	6V, V ₁ =2V, V ₀ =5.5V			100	μΑ
VoL			\/	I _{OL} =12mA		0.25	0.4	V V V μA V V μA μA μA mA mA
	Low-level output voltage		V _I =0.6V, V _I =2V	V _{CC} =4.75V		0.35	0.5	V
ĺ			VI=0.0V, VI=2V	I _{OL} =48mA		0.4	0.5	V
		A, B	V _{GG} =5.25V, V _I =2.7V			20	μА	
Local	High-level input current	DIR, OC	VC0=5.25V, V =2	./٧			20	μА
I _{IH}	riigirieveriiipat carrent	A, B	V _{CC} =5.25V, V _I =5	.5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =1	0V			0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0	.4V			-0.4	mA
Icch	Supply current, all outputs high		V _{CC} =5.25V, V _I =0	V, V _I =4.5V		48	70	mA
IccL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0	V, V _I =4.5V		62	90	mA
locz	Supply current, all outputs of	f	V _{CC} =5.25V, V _I =0	V, V _I =4.5V		64	95	mA

^{*}: All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

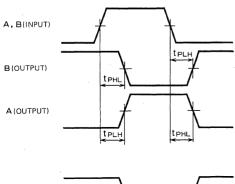
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Param	notor	Test conditions		Limits		Unit
Symbol	T di di		rest conditions	Min	Тур	Max	Unit
t	Low-to-high-level output From input A to output B From input B to output A	From input A to output B			16	25	
t _{PLH}				20	25	118	
+ High	High-to-low level output	From input A to output B			14	25	20
t _{PHL}	propagation time	From input B to output A	0 -45-5 B = 667.0 (Nove 0)		15	25	ns
t	Low-to-high level outpout	From input OC to output A	$C_L=45pF$, $R_L=667 \Omega$ (Note 2)		25	40	
t _{PLH}	propagation time	From input OC to output B			25	40	ns
t	High-to-low-level outpout	From input OC to output A			30	60	
t PHL propagation time	propagation time	From input \overline{OC} to output B			30	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.





DESCRIPTION

The M74LS645P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out ($I_{OI} = 24\text{mA}$, $I_{OH} = -15\text{mA}$)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment

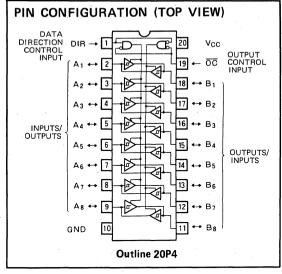
FUNCTIONAL DESCRIPTION

The inputs and outputs of the buffer circuits with 3-state outputs are connected together to form bi-directional buffers.

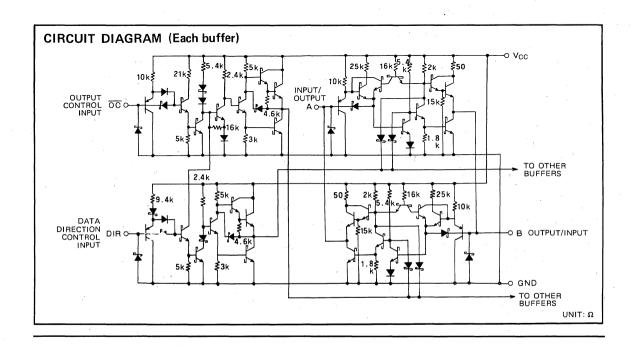
The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.



A device, M74LS645-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



FUNCTION TABLE (Note 1)

ŌĊ	DIR	А	В
L	L	0	ı
L	Н	1	0
н	×	Z	Z

Note 1: 1: Input pin

O: Output (non-inverted output) pin -Z: High impedance (A, B separated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol			Conditions	Limits	Unit
Vcc			voltage		V
	Input voltage	A. B		-0.5~+5.5	V
VI	Input vortage	DIR, OC		-0.5~+15	V V V V C C
Vo	Output voltage		Off state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		·	-20~+75	℃
Tstg	Storage temperature range			−65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

C	D			Limits			
Symbol	Parameter		.Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	V		
	Lligh lovel autout average	V _{OH} ≧ 2.4V	0		-3	mA	
Іон	High-level output current	V _{OH} ≧ 2V	0		- 15	mΑ	
	Law law law and a second	V _{OL} ≤ 0.4V	0		12	mΑ	
loL	Low-level output current	V _{OL} ≤ 0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Por	ameter	Test cond	itions		Limits		
Symbol	Fai	arrieter	rest cond	Itions	Min	Тур *	.Max	. Unit
VIH	High-level input voltage				2			٧
VIL	Low-level input voltage	The state of the s		1			0.6	٧ .
V _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	٧
.,	High-level output voltage		V _{CC} =4.75V	I _{OH} = - 3mA	2.4	3.4		V
Voн			$V_1 = 0.6V, V_1 = 2V$	I _{OH} = - 15mA	2			٧
\/ -	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	٧
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_I = 0.6V,$	$V_1 = 2V, \ V_0 = 2.7V$			20	μΑ
lozL	Off-state low-level output	Off-state low-level output current		$V_1 = 2V, \ V_0 = 0.4V$			-400	μΑ
		A, B		V 5.05V V 0.7V			20	μΑ
İ İ	High-level input	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.7$	V			20	μΑ
Iн	current	A, B	V _{CC} =5.25V, V _I =5.5	V			0.1	20 μA 20 μA
		DIR. OC	V _{CC} =5.25V, V _I = 10V	/			0.1	mA
li∟`	Low-level input current		V _{CC} =5.25V, V _I =0.4	V.			-0.4	mΑ
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O = 0	/	- 40		- 225	mA
Гссн	Supply current, all outputs high		V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5 V		48	70	mA
ICCL	Supply current, all outpus low		V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5V		62	90	mA
locz	Supply current, all outp	uts off	V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5V		64	95	mΑ

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

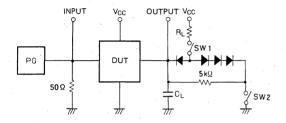
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS (Voc=5V, Ta=25°C, unless otherwise noted)

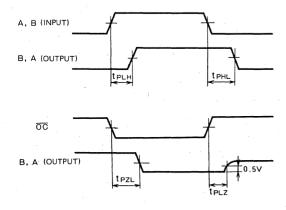
Symbol	Par	ameter	Test conditions	Limits		Unit	
Syllibol	, a	ameter	Test conditions	Min	Тур	Max	Oill
	Low-to-high level output	From input A to output B			12	15	ns
t _{PLH}	propagation time From input B to output A	From input B to output A	$C_1 = 45 \text{ pF}$ (Note 3)		12	15	. ns
	High-to-low level output	From input A to output B	C _L =45pF (Note 3)		12	15	ns
t PHL propagation time	From input B to output A			12	15	""	
	Low output onable time	From input OC to output A			25	40	ns
tpZL	Low output enable time From input OC to output B	R _L =667 Ω, C _L =45pF		25	40	115	
•	High outputopolile time	From input OC to output A	(Note 3)		23	40	
tpzH	High outputenable time	From input OC to output B	(Note 3)		23	40	ns
•	I dibla dima	From input OC to output A			17	25	
t _{PLZ}	Low output disable time	From input OC to output B	R _L =667Ω, C _L =5pF		17	25	ns
	I link and a direktor direct	From input OC to output A	(Note 3)		19	25	
t _{PHZ}	High output disable time	From input OC to output B	1,1010 0,		19	25	ns

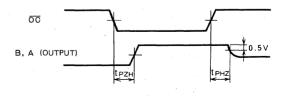
Note 3: Measurement circuit



Parameter	SW 1	SW2	
t PZH	Open	Closed	
t PZL	PZL Closed		
t PLZ	Closed	Closed	
t PHZ	Closed	Closed	

- The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P, P, Z_O = 50Ω
 All diodes are high speed switching diodes
- $(t_{rr} \leq 4ns)$.
- (3) CL includes probe and jig capacitance.





M74LS645-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS645-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out ($I_{OL} = 48mA$, $I_{OH} = -15mA$)
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

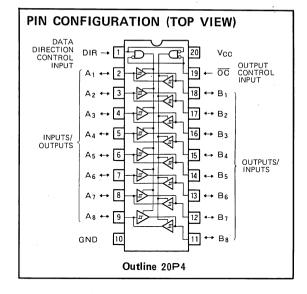
General purpose, for use in industrial and consumer equipment.

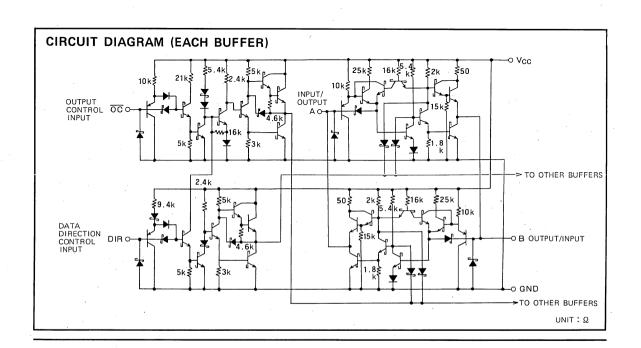
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state non-inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





M74LS645-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

-				
Ĺ	ŌC	DIR	Α	В
L	L	L	0	1
L	L	H	· 1	0
	Н	X	. Z	Z

Note 1: | I Input pin

O: Output (non-inverted output) pin

Z: High impedance (A and B are isolated)

X : |rrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~ +75℃, unless otherwise noted)

Symbol	Param	eter	Conditions	Limits	Unit
Vcc	Supply voltage		·	-0.5~+7	V -
Vı	V _I Input voltage	А, В	·	-0.5~+5.5	V
VI		DIR, OC		-0.5~+15	٧
Vo	Output voltage		Off-state	$-0.5 \sim +5.5$	٧
Topr	opr Operating free-air ambient temperature range			-20~+75	°
Tstg	Storage temperature range	,		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol Vcc IOH	Parameter			Limits			
	Farameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
1	High-level output current	V _{OH} ≥ 2.4V	0		-3	mA	
тон	riigii-level output current	V _{OH} ≧ 2V	0		— 15	mΑ	
	Low-level output current	V _{OL} ≤ 0.4V	. 0		12	mA	
IOL	Low-rever output current	V _{OL} ≤ 0.5V	. 0		48	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Test condit	ione		Limits		Unit
Symbol	raianietei		lest condit		Min	Тур 🛪	Max	Offit
VIH	High-level input voltage				2			· V
VIL	Low-level input voltage						0.6	٧
$V_{T+}-V_{T-}$	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5 ,	٧
.,	High-level output voltage		V _{CC} =4.75V	I _{OH} = -3mA	2.4	3.4		٧
Voн	riigii-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OH} = 15mA	2		Typ * Max 0.6 0.4 -1.5 3.4 0.25 0.4	٧
			V 4 751/	I _{OL} =12mA		0.25	0.4	, V .
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	٧
1			$V_1 = 0.6V, V_1 = 2V$	I _{OL} =48mA		0.4	0.5	٧
Tozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V	$, V_1 = 2V, V_0 = 2.7V$			20	μΑ
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V	$, V_1 = 2V, V_0 = 0.4V$			-400	μА
		A, B	\\	1) /			20	μА
Luc	High-level input current	DIR, OC	$V_{CC} = 5.25V, V_{I} = 2.7V$				20	μА
	riigii-level iliput current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
	<u> </u>	DIR, OC	V _{CC} =5.25V, V _I =10\	1			0.6 -1.5. 0.4 0.5 0.5 20 -400 20 0.1 0.1 -0.4 -225 70 90	mA
1114	Low-level input current		V _{CC} =5.25V, V _I =0.4	IV.			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} = 5.25V . V _O = 0V	/	- 40		-225	mA
Гссн	Supply current, all outputs high	*	V _{CC} =5.25V, V _I =0V	, V _I =4.5V		48	70	mA .
ICCL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		62	90	mA
I _{CCZ}	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		64	95	mA

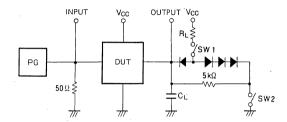
^{* :} All typical values are at V_{CC}=5V, Ta=25°C

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

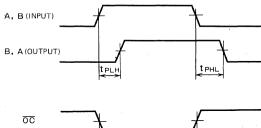
Symbol Low-to-high-level outp	Paran	notor	Test conditions		Limits		
Зутыот	raran	ieter	rest conditions	Min	Тур	Max	Unit
+_	Low-to-high-level output	From input A to output B			12	15	ns
t _{PLH}	propagation time	From input B to output A	C ₁ = 45 pF (Note 3)		12	15	115
t	High-to-low level output propagation time	From input A to output B	CL=45pF (Note 3)		12	15	ns
t _{PHL}		From input B to output A			12	15	
1	Low-level output enable time High-level output enable	From input OC to output A	1		25	40	ns ns
1 _{PZL}		From input OC to output B			25	40	
+		From input OC to output A	R _L =667Ω, C _L =45pF (Note 3)		23	40	
t _{PZH}	time .	From input OC to output B	•		-23	40	
+	Low-level output disable	From input OC to output A			17	25	ns ns
t _{PLZ}	time High-level outpout disable	From input OC to output B			17	25	
t		From input OC to output A	$R_{\perp}=667 \Omega$, $C_{\perp}=5pF$ (Note 3)		19	25	
t _{PHZ}	time	From input OC to output B			19	25	

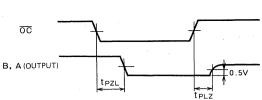
Note 3: Measurement circuit

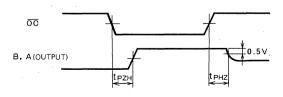


Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- $V_P = 3V_{P.P}$, $Z_0 = 50\Omega$. (2) All diodes are switching diodes ($t_{rr} \le 4ns$)
- (3) C_L includes probe and jig capacitance.







M74LS668P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS668P is a semiconductor integrated circuit containing a synchronous decade counter function with an up/down control input and preset input.

FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

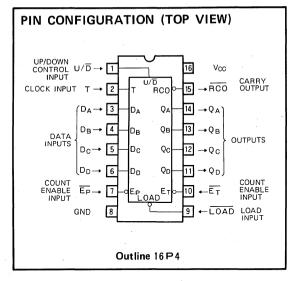
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

Data is also acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D ; and occurs after preset is initiated by dropping load input (LOAD) to a low-level.

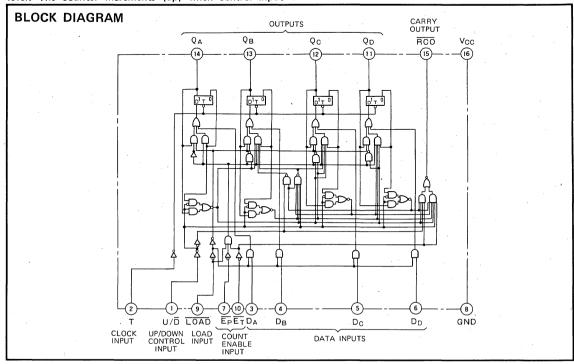
Up/down counter operations are initiated when \overline{LOAD} is high-level, and the count enable input $(\overline{E_P}$ and $\overline{E_T})$ is low-level. The counter increments (up) when control input



 U/\overline{D} is high-level, and decrements (down) at low-level.

Carry output (\overline{RCO}) goes low-level (active) at 9_2 during up counting operations and at O_2 while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a decade counter. (See the application example provided in the back of this specification sheet.)

Counter operations are inhibited when $\overline{\text{LOAD}}$ and $(\overline{\text{E}_{P}})$ or $\overline{\text{E}_{T}}$) are all high-level.



FUNCTION TABLE (Note 1)

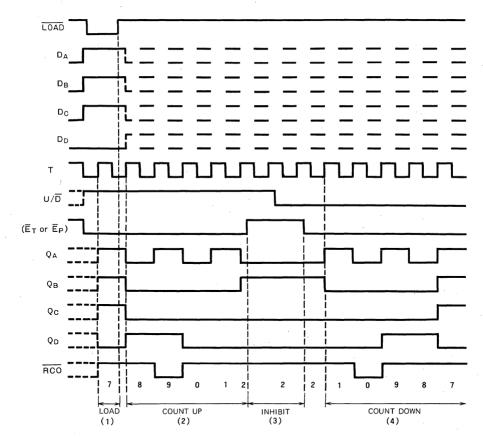
LOAD	Еp	ĒΤ	U/Ď	Т	QA	Q _B	Qс	QD	RCO*
L	. X	Х	Х	1	D _A	D _B	Dc	D _D	Н
Н	L	L	Н	1		COUNT	UP		Н
Н	L	L	L	1		COUNT	DOWN		Н
Н	н	Х	X	×		COUNT	INILIDIT		
H.	×	Н	×	X	,	COUNT	INFIIDIT		Н

Note 1. 1 : Transition from low to high

Transition from two to right free varieties of the following states of the following that the following states of the followi

 $\overline{RCO} = Q_A \cdot Q_D \cdot (U/\overline{D}) \cdot \overline{E_T}$ $\overline{RCO} = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{U/D}) \cdot \overline{E}_T$

TIMING DIAGRAM



Timing diagram notes:

- (1) Preset at 7
- (2) Increment at 8, 9, 0, 1, 2
- (3) Count inhibit
- (4) Decrement at 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage '		−0.5∼+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range	,	−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C	Parama	Parameter			Limits			
Symbol	rarame	ter	Min	Min Typ Max				
Vcc	Supply voltage		4.75	5	5.25	. V		
I _{OH}	High-level output current	V _{OH} ≧2.7V	. 0		-400	μА		
	Law lovel autout augrent	V _{OL} ≤0.4V	0		4	mA		
IOL	L Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter		T dist	Test conditions		Limits		
Symbol	,	rarameter	lest condition	s	Min	Тур	Max	Unit
V _{IH}	High-level input vo	tage			2			٧.
VIL	Low-level input vol	tage					0.8	. V
V _{IC}	Input clamp voltag	е .	V _{CC} =4.75V, I _{IC} =-18	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH} High-level output voltage		oltage	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-400μA		2.7	3.4		٧
.,		-1	V _{CC} =4.75V	I _{OL} =4 mA		0.25	0.4	V
VoL	Low-level output v	Low-level output voltage		I _{OL} =8mA		0.35	0.5	V
	High-level input	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$,			20	
		T, E _T	V _{CC} =5.25V, V _I =2.7V				20	μА
		LOAD					40	
I _{IH}	current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$					0.1	
		T, E _T	V _{CC} =5.25V, V _I =10V			,	0.1	mA
		LOAD					0.2	
		$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$					-0.4	
HE	Low-level input current	T, E _T	$V_{CC}=5.25V, V_{I}=0.4V$				-0.4	mA
Sorreite		LOAD	1				-0.8	
los .	Short-circuit outpu	t current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
1cc	Supply current		V _{CC} =5.25V (Note 3)			20	34	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C. Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.



^{3.} ICC is measured after applying a momentary 4.5V, then ground, to clock input with other inputs grounded and the outputs open.

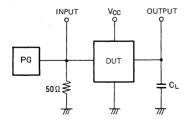
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Cumalani	D	Total conditions	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		25	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			24	40	
t _{PHL}		C _L = 15pF (Note 4)		30	60	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A , Q_B , Q_C , and Q_D			18	27	ns
t _{PHL}				15	27	""
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	17	ns
t _{PHL}	time, from input ET to output RCO			24	45	113
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input U/D to output RCO			20	35	
t PHL				20	40	ns

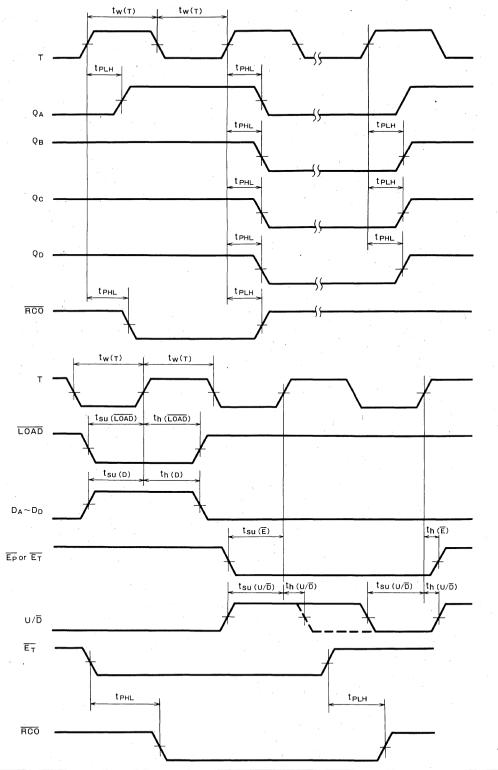
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

tsu(D) S	Parameter	Test conditions		Unit		
	Parameter	lest conditions	Min	Тур	Max	Unit
t _w	Clock T pulse width		25	10		ns
t _{su(D)}	Setup time D _A ∼D _D to T	·	20	18		ns
t _{su(E)}	Setup time E _T , E _P to T		35	26		ns
tsu(LOAD)	Setup time LOAD to T		25	15		ns
t _{su(U/□)}	Setup time U/D to T		30	20		ns
th	Setup time of all inputs to T	·	0	— 15		ns

Note 4. Measurement circuit

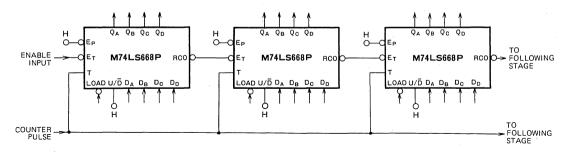


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_{\rm W}$ = 500ns, $V_{\rm P}$ = 3 $V_{\rm P.P}$, $Z_{\rm O}$ = 50 Ω . (2) C_L includes probe and jig capacitance.



APPLICATION EXAMPLE

10ⁿ counter with cascade connection



DESCRIPTION

The M74LS669P is a semiconductor integrated circuit containing a synchronous 4-bit binary counter function with an up/down control input and preset input.

FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

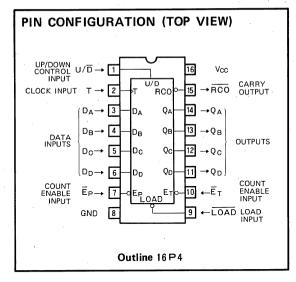
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

Data is acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D ; and occurs after preset is initiated by dropping load input (\overline{LOAD}) to a low-level.

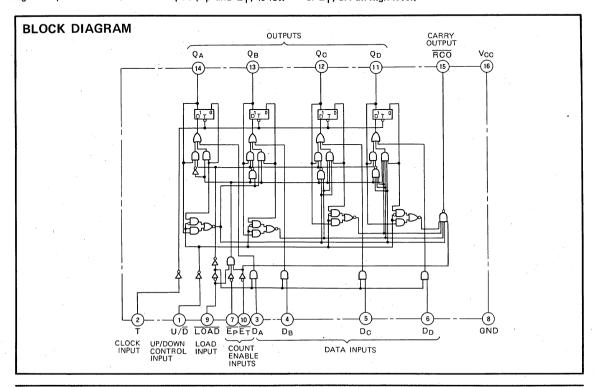
Up/down counter operations are initiated when $\overline{\text{LOAD}}$ is high-level, and the count enable input $(\overline{\mathbb{E}_P} \text{ and } \overline{\mathbb{E}_T})$ is low-



level. The counter increments (up) when control input U/\overline{D} is high-level, and decrements (down) at low-level.

Carry output (\overline{RCO}) goes low-level (active) at 15₂ during up operations, and at 0₂ while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a binary counter. (See the application example given for M74LS668P.)

Counter operations are inhibited when $\overline{\text{LOAD}}$ and $(\overline{\text{E}_{P}})$ or $\overline{\text{E}_{T}}$) are all high-level.





FUNCTION TABLE (Note 1)

LOAD	Εp	ĒΤ	U/D̄	Т	QA	QB	Qc	QD	RCO*
,L	×	×	Х	1	D_A	DB	Dc	D _D	H
Н	L	L	Н	1	COUNT UP				Н
Н	L	· L	L	1	COUNT DOWN				Н
Н	Н	Х	Х	Х	COUNT INHIBIT				
Н	Х	Н	Х	×				н	

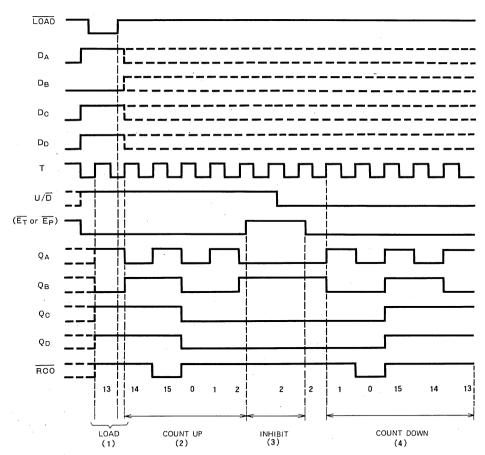
Note 1. † : Transition from low to high

X : Irrelevant

* REC is normally at high-level, however, when E_T is low and the counter is incrementing, Q_A , Q_B , Q_C and Q_D will be high, and RCO will be low. Also, when the counter is decrementing, Q_A , Q_B , Q_C and Q_D will be low, and RCO will also be low.

 $\overline{RCO} = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (U/\overline{D}) \cdot \overline{E_T}$ $\overline{RCO} = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D (U/\overline{D}) \cdot \overline{E_T}$

TIMING DIAGRAM



Timing diagram notes:

- (1) Preset at 13
- (2) Increment at 14, 15, 0, 1, 2
- (3) Count inhibit
- (4) Decrement at 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V.
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol						
Symbol	Param	eter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
1он	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
	Low-level output current	V _{OL} ≤0.4V	0		4.	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Parameter	Test conditions			Limits		Unit
Symbol		Parameter	rest conditions	i	Min	Тур	Max	Unit
V _{IH}	High-level input vol	tage			2			V.
V _{IL}	Low-level input vol	tage					0.8	٧
Vic	Input clamp voltage	•	V _{CC} =4.75V, I _{IC} =-18m	nA			-1.5	٧
Vон	High-level output vo	pltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400 \mu A$		2.7	3.4		V
		altago	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V _{OL}	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
_		D_A , D_B , D_C , D_D , $\overline{E_P}$, U/\overline{D}		1			20	
		T, E _T	V _{CC} =5.25V, V _I =2.7V				20	μА
	High-level input	LOAD					40	
hн	current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$					0.1	
		T, ET	$V_{CC}=5.25V, V_{I}=10V$			0.1	mA	
		LOAD	,				0.2	
		$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$					-0.4	
1	Low-level input current	T, ET	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
		LOAD					-0.8	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		-20		¹ —100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)		- N	, 50	34	mA

^{*} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with 'all other inputs grounded.

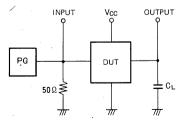
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0 1 1	Parameter	Task and distance		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Oilit
f _{max}	Maximum clock frequency		25	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			24	40	
t _{PHL}	propagation time, from input T to output RCO			32	60	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		20	27	
t _{PHL}	time, from input T to outputs Q_A , Q_B , Q_C , and Q_D			15	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			10	17	ns
t _{PHL}	propagation time, from input E _T to output RCO			28	45	. 115
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			25	35	
t _{PHL}	time, from input U/D to output RCO			20	40	ns

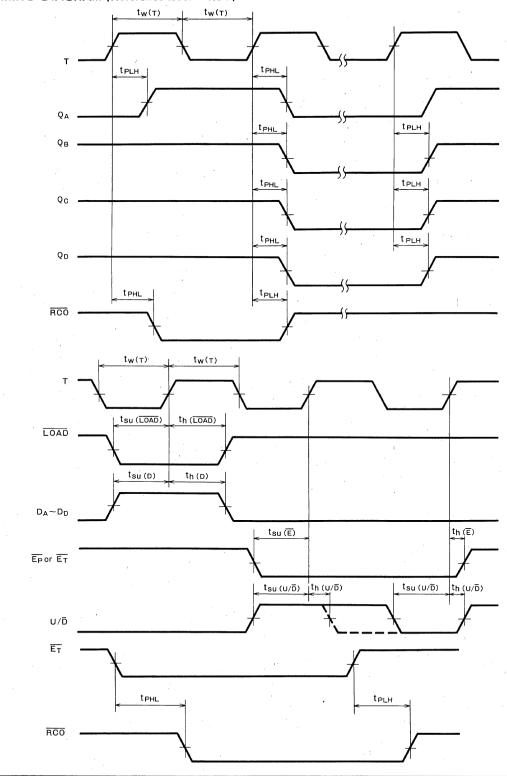
TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

	2	Tark soudising		Unit		
Symbol	. Parameter	Test conditions	Min	Тур	Max	Unit
tw	Clock T pulse width		25	, 12		ns
t _{su(D)}	Setup time D _A ∼D _D to T	7	20	18		ns
t _{su(E)}	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
t _{SU (LOAD)}	Setup time LOAD to T		25	15		ns
t _{su(U/D̄)}	Setup time U/D to T		30	20		ns
th	Setup time of all inputs to T		0	— 15		ns

Note 4. Measurement Circuit



- The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_t = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
 C_L includes probe and jig capacitance.



M74LS670P

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS670P is a semiconductor integrated circuit containing a 4 word x 4 bit register file circuit with 3-state outputs.

FEATURES

- Since read address and write address are independent, simultaneous writing and reading of data is possible.
- Provided with read enable input and output control inputs
- Storage capacity can be easily expanded with the aid of the enable input.
- AND-tie may be used (With 3-state output)
 Wide operating temperature range (T_a = -20 ~ +75°C)

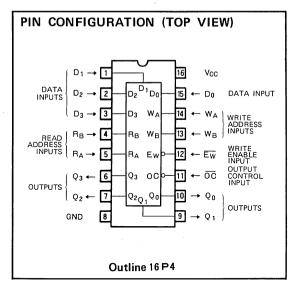
APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

16 flip-flops are used as storage devices, and a discrete enable input, address input, and output controlling input are provided for reading and writing. Accordingly, during writing, the contents of other words can be read, and during reading, other words can be written, thereby enhansing to high-speed operation.

The 3-state output permits 128-output AND-tie even in the worst condition. Expansion of up to 512 words is possible. possible.

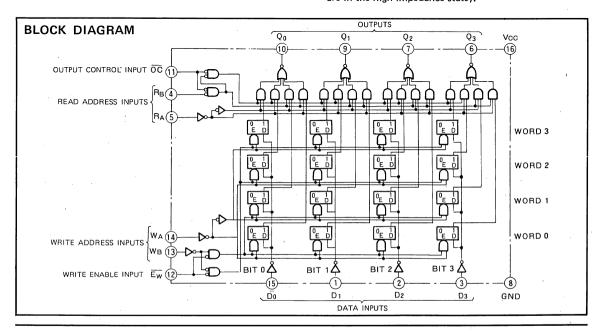


Writing Method

By designating a word using write address inputs W_A and W_B and applying data to the data inputs D_0 , D_1 , D_2 , and D_3 , writing into each bit is performed. For writing the write enable input $\overline{E_W}$ is held low (Writing will not be performed if $\overline{E_W}$ is high)

Readout Method

When a word is designated by read address inputs R_A and R_B , the contents of each bit appear in the outputs Q_0 , Q_1 , Q_2 , and Q_3 . For reading the output control input \overline{OC} is held low. (when \overline{OC} is high, all the outputs are in the high-impedance state).



4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Writing Method

,,,	WA WB		Word					
,WA	WB	Ew	0	1	2	3		
×	×	Н	Q ⁰	Q ⁰	Q ⁰	Q ⁰		
L	L	L	Q=D	Q0	Q0	Q ⁰		
Н	L	L	Q ⁰	Q=D	Q0	Q ⁰		
L	Н	L	Q0	Q ⁰	Q=D	Q ⁰		
Н	Н	L	Q0	Q0	Q0	Q = D		

Readout Method

RA	RB	ōc	Q_0	Q ₁	Q ₂	Q3
X	×	Н	Z	Z	Z	Z
L.	L	L	W ₀ B ₀	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃
Н	L	L	W ₁ B ₀	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃
L	Н	٦	W ₂ B ₀	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃
Н	Н	L	W ₃ B ₀	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃

Note 1: Q0: The level of Q before the indicated steady-state input conditions were established.

O = D : The four selected internal latch outputs will assume the states applied to the four external data inputs.

WxBy: The Yth bit of word X. X: irrelevant Z: high-impedance

ABSOLUTE MAXIMUM RATINGS $(T_a = -20 \sim +75^{\circ}C,)$

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V.	
Vı	Input voltage		-0.5~+15	V	
Vo	Output voltage	Off-state	-0.5~+5.5	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	℃	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0				Unit		
Symbol	Parame	ter	Min	Тур	Max	0
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.4V	0		-2.6	· mA
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	. 0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70^{\circ}C$, unless otherwise noted)

0				***		Limits		Unit
Symbol	Paramete	ır .	Test cond	itions	Min ·	Тур*	Max	Oiiit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage	`					0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
VoH	High-level output voltage	igh-level output voltage		V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-2.6mA		3.1		٧
.,			V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	٧
lozh	Off-state high-level output cu	rrent	V _{CC} =5.25V, V _I =2V, V _I =2.7V				20 .	μА
lozL	Off-state low-level output cur	rent	V _{CC} =5.25V, V _I =2V, V _I =0.4V				_ 20	μА
		Ew					40	
		ŌĊ	V _{CC} =5.25V, V _I =2.7V				60	μA
Lon	10.6.1	Other input				20		
ļЛн	High-level input current	Ew	,				0.2	
		ŌC	V _{CC} =5 .25V , V _I = 10V	1			0.3	mΑ
		Other input					0.1	
		Ew					-0.8	
l ₁ L	Low-level input current	ŌC	V _{CC} =5.25V, V _I =0.4	V			-1.2	mA
		Other input					-0.4	
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-30		— 130	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			30	50	mA



^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

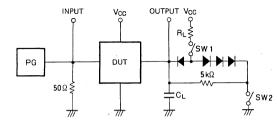
3: Icc is measured with W_A, W_B, R_A, R_B inputs grounded and D₀ ~ D₃, E_W, OC inputs at 4.5V.

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

C	Parameter	Test conditions		Unit		
Symbol	rarameter	rest conditions	Min	Тур	Max	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	40	ns
t _{PHL}	time, from input RA, RB to output Q0, Q1, Q2, Q3			14	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15p F (Note 4)		11	45	ns
t _{PHL}	time, from input $\overline{E_W}$ to output Q_0 , Q_1 , Q_2 , Q_3	OL - ISPF (Note 4)		16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	e,		9	45	ns
t _{PHL}	from input D_0 , D_1 , D_2 , D_3 to output Q_0 , Q_1 , Q_2 , Q_3			14	40	ns
t _{PZH}	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 4)		6	35	ns
t _{PZL}	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 4)		10	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 4)		16	50	ns
t _{PLZ}	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 4)		7	35	ns

Note 4: Measurement circuit



Symbol	SW 1	SW2		
t _{PZH}	Open	Closed		
t PZL	Closed	Open		
t PLZ	Closed	Closed		
t	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics:
- PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

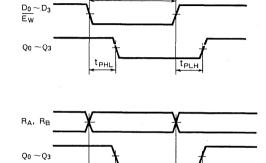
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
			Min	Тур	Max	Unit
tw(Ew)	Write enable input Ew pulse width		25	9		ns
tw(oc)	Output control input OC pulse width		25	9		ns
t _{SU(D)}	Setup time D ₀ ~D ₃ to E _W		10	5		ns
t _{SU(W)}	Setup time W _A , W _B to E _W		15	-2		ns
t _{h (D)}	Hold time D ₀ ∼D ₃ to E W		15	1		ns
t _{h (W)}	Hold time W _A , W _B to E _W		5	0		ns
tlatch	Latch time for new date (Note 5)		25	5		ns

Note 5: Latch time is the time allowed for the internal output of the latch to assume the state of new data.

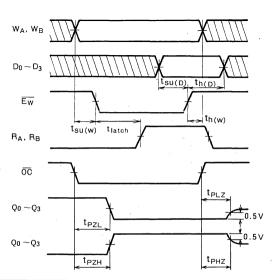
t_{PLH}

TIMING DIAGRAM (Reference level = 1.3V)



Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

t_{PHL}



NEW PRODUCT

MITSUBISHI LSTTLS M74LS682P

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS682P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal 24kΩ pull-up resistors on the Q inputs
- Active pull-up outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

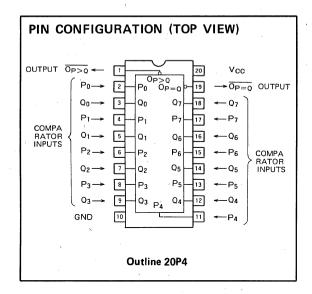
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

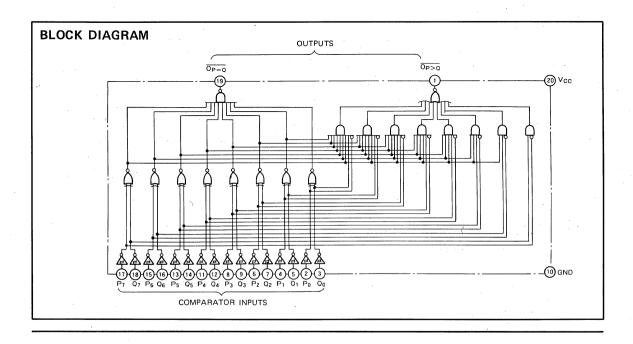
 $Q_0 \sim Q_7$ have internal pull-up resistors (=24k Ω), so that misoperation due to noise is reduced on condition that $Q_0 \sim Q_7$ are open.

Beside the IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application. $\ \ \,$



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	Op=Q	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No ·	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	





FUNCTION TABLE

P, Q	O _{P=Q}	0 _{P>Q}
P=Q	L	Н
P>Q	н	L
P <q< td=""><td>н</td><td>Н</td></q<>	н	Н

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	Input voltage	Inputs P	-0.5~+15	V
Vı		Inputs Q	-0.5~V _{CC} +0.5	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20~+75℃, unless otherwise noted)

C	Parameter			Limits .			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	٧		
1 _{0H}	High-level output current	V _{OH} ≥ 2.7V	0		-400	μΑ	
	Low-level output current	V _{OL} ≦0.4V	0		12	mA	
loL		V _{OL} ≤0.5V	0		24	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Tost o	Test conditions		Limits		
Symbol	raramete	:r	Test c	Test conditions		Тур*	Max	Unit
V _{IH}	High-level input voltage •				2			V.
VIL	Low-level input voltage						0.8	V
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V			0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA				-1.5	٧
VoH	High-level output voltage		$V_{CC} = 4.75V$, $V_1 = 2V$, $V_1 = 0.8V$, $I_{OH} = -400\mu A$		2.7			V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL			$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
		P, Q	V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =2.7V V _{CC} =5.25V, V _I =10V			20	μΑ
LiH	High-level input current	Р	V _{CC} =5.25V, V _I					
	Q		V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =5.5V			0.1	mA
	1 11	Р					-0.2	mA
T _I L	Low-level input current Q		$V_{CC}=5.25V, V_1=0.4V$				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O	V _{CC} =5.25V, V _O =0V			100	mA
loc	Supply current		V _{CC} =5.25V (Note 2)			42	70	mA

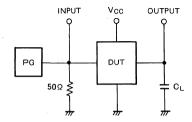
^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C. Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

^{2:} ICC is measured with all inputs at value of 4.5V.

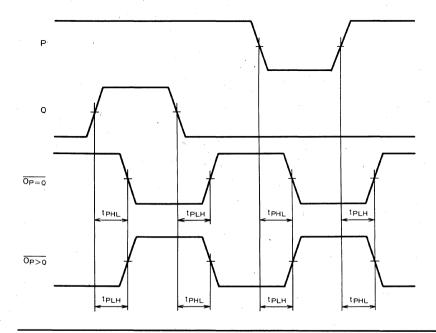
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

0	Parameter	T	Limits			Unio
Symbol		Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high level, high-to-low level output			13	30	
t PHL	propagation time from inputs P to output Op=Q			16	30	ns
t PLH	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{OP} = Q$ Low-to-high level, high-to-low level output			12	30	
tpHL		C _L =45pF (Note 3) All other input pins in low-state		17	30	ns
t PLH				24	30	
t PHL	propagation time from inputs P to output OP>Q			21	30	ns
tpLH	Low-to-high level, high-to-low level output		,	26	30	
t PHL	propagation time from inputs Q to output $\overline{O_{P>Q}}$			27	30	ns

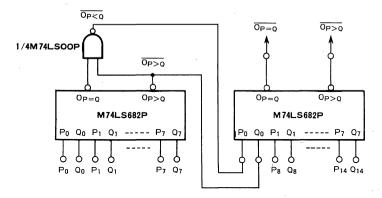
Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P .p, Z_D = 50 Ω
- (2) C_L includes probe and jig capacitance.



APPLICATION EXAMPLE Example of 15-bit comparator



DESCRIPITON

The M74LS683P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal 24kΩ pull-up resistors on the Q inputs
- Open collector outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

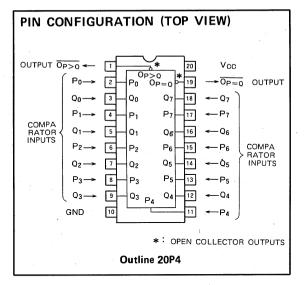
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

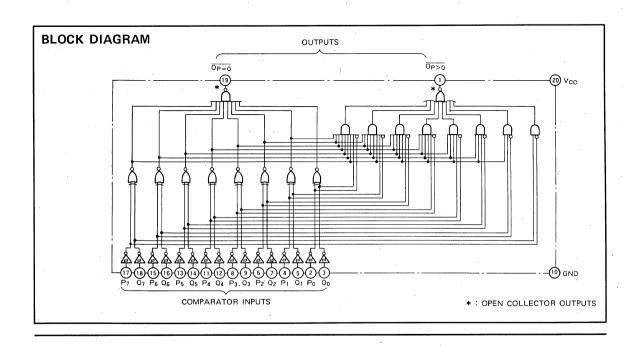
 $Q_0\sim Q_7$ have internal pull-up resistors (=24k Ω), so that misoperation due to noise is reduced on condition that $Q_0\sim Q_7$ are open.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Type	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	Op=Q	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No .	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



FUNCTION TABLE

P, Q	O _{P=0}	OP>Q
P=Q	L	. н
P>Q	Н	٦
P <q< td=""><td>Н</td><td>Н</td></q<>	Н	Н

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	Input voltage	Inputs P	-0.5~+15	V
Vı		Inputs Q	-0.5~V _{CC} +0.5	V
V ₀	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	ာ
T _{stg}	Storage temperature range		−65∼+150	ဗ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Unit		
Symbol			Min	Тур	Max	Unit .
Vcc	Supply voltage	4.75	5	5.25	V	
Іон	High-level output current	V ₀ =5.5V	0		100	μΑ
1	Low-level output current	V ₀ L≦0.4V઼	0		12	mA
lor		V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

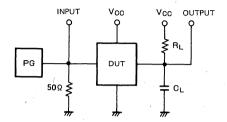
Symbol	Parameter		Took	Test conditions		Limits		
Symbol	rarameter		rest	conditions	Min	Min Typ *		Unit
Уін	High-level input voltage				2			٧
VIL	Low-level input voltage						0.8	V
V _{T+} V _{T-}	Hysteresis width		V _{CC} =4.75V	V _{CC} =4.75V		0.4		٧
. V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA				-1.5	٧
Гон	High-level output current	ligh-level output current		$V_{CC}=4.75V, V_1=2V, V_1=0.8V, V_0=5.5V$			100	μΑ
	Low-level output voltage		V _{CC} =4.75V I _{OL} =12m			0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
		P, Q	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
Liн	High-level input current	Р	V _{CC} =5.25V, V _I	=10V ·				
	. Q		V _{CC} =5.25V, V _I =5.5V				0.1	mA
	Low-level input current	Р	V _{CC} =5.25V, V ₁ =0.4V			-0.2	-0.2	mA
IIL	Low-level input current	Q					-0.4	mA
lcc	Supply current		V _{CC} =5.25V (Note 1)			42	70	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C. Note 1: I_{CC} is measured with all inputs at value of 4.5V.

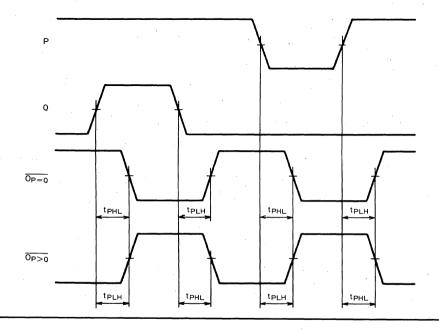
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Farameter	rest conditions	Min	Тур	Max	Oilit
tpLH	Low-to-high level, high-to-low level output			23	45	
t PHL	propagation time from inputs P to output $\overline{O_{P=Q}}$			20	30	ns
tpLH	Low-to-high level, high-to-low level output			21	40	
tpHL	propagation time from inputs Q to output $\overline{O_{P=Q}}$	B6670 O4505 (Note 0)		20	35	ns
tPLH	Low-to-high level, high-to-low level output	R _L =667Ω, C _L =45pF (Note 2) All other input pins in low-state.		26	45	
tpHL	propagation time from inputs P to output $\overline{OP>Q}$		-	22	30	ns
tpLH	Low-to-high level high-to-low level output			28	45	
t PHL	propagation time from inputs Q to output Op>Q			26	30	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P, P, Z_O = 50Ω
 (2) C_L includes probe and jig capacitance.



MITSUBISHI LSTTLS M74LS684P

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS684P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Active pull-up outputs.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

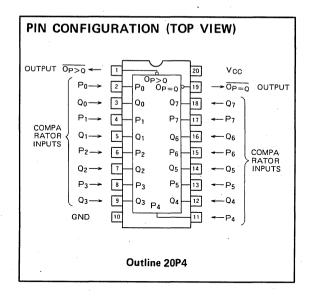
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

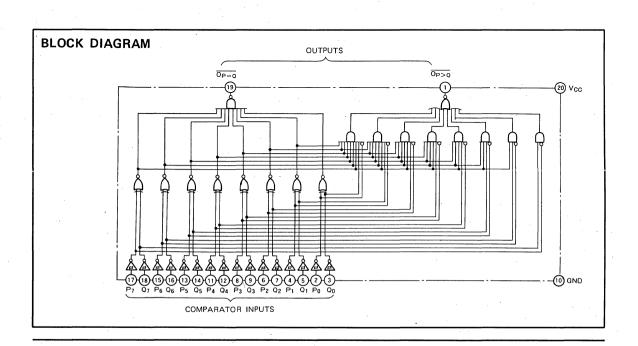
Note that this IC, in comparison to M74LS682P, does not have internal pull-up resistors on its inputs $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	0 _{P=0}	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



FUNCTION TABLE

. P, Q	O _{P=0}	0 _{P>0}
P=Q	L	Н
P>Q	. н	L
P <q< td=""><td>н</td><td>Н</td></q<>	н	Н

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	' V
Vı	Input voltage		-0.5~+15	٧
V ₀	Output voltage	High-level state	-0.5~V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	ొ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	Parar	neter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
lон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ	
		V _{OL} ≦0.4V	0		12	mA	
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

CombI			Test conditions		Limits		Unit
Symbol	Parameter	l est co			Тур *	Max	Unit
V _{IH} .	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V			0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	٧
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_1 = 2V$, $V_1 = 0.8V$, $I_{OH} = -400\mu$ A		2.7			٧
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
V _{OL}	Low-level output voltage	$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	٧
		V _{CC} =5.25V, V _I =	-2.7V			20	μΑ
, lin .	High-level input current	V _{CC} =5.25V, V _I =	=10V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.2	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
lcc	Supply current	V _{CC} =5.25V (Note	⊋2)		40	65	mA .

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

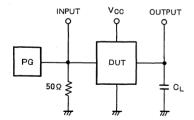
· Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit
t PLH	Low-to-high level, high-to-low level output			13	30	
t PHL	propagation time from inputs P to output Op=Q			16	30	ns
t PLH	Low-to-high level, high-to-low level output			. 12	30	
t PHL	propagation time from inputs Q to output Op=Q	0 -45-5 (1) - 0		17	30	ns
t PLH	Low-to-high level, high-to-low level output	C _L =45pF (Note 3) All other input pins in low-state		24	30	
t PHL	propagation time from inputs P to output OP>Q			21	30	ns
t _{PLH}	Low-to-high level, high-to-low level output			26	30	
t PHL	Propagation time from inputs Q to output $\overline{OP>Q}$			27	30	ns

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

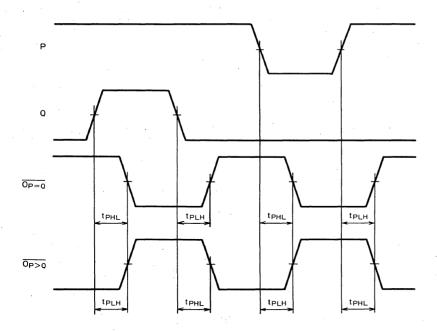
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

^{2:} ICC is measured with all inputs at value of 4.5V.

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_t = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P, P, Z_O = 50Ω
 (2) C_L includes probe and jig capacitance.



MITSUBISHI LSTTLS M74LS685P

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS685P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mW typical)
- Open collector outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in for industrial and consumer equipment.

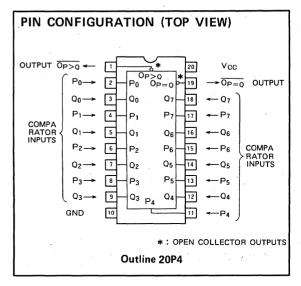
FUNCTIONAL DESCRIPTION

The eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

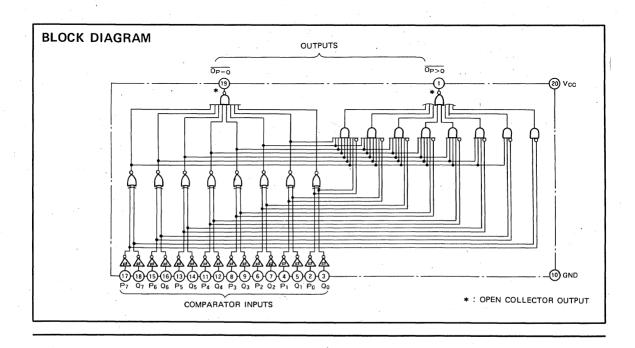
Note that this IC, in comparison to M74LS683P, does not have internal pull-up resistors on its inputs $\Omega_0 \sim \Omega_7$.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	Op=0	OP>0	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No .	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector ,	



FUNCTION TABLE

P, Q	O _{P=Q}	O _{P>Q}
P=Q	L	Н
P>Q	Н	L
P<0	. н	H

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	υ
Tstg	Storage temperature range		-65~ +150	r

RECOMMENDED OPERATING CONDITIONS (Ta = −20~+75℃, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	Param	eter 	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V ₀ =5.5V	0		100	μΑ	
	Low-level output current	V ₀ L≦0.4V	0		12	mΑ	
lor	Low-level output current	V _{OL} ≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

0	Parameter	Test conditions		1	Limits		
Symbol	or rest conditions		onditions	Min	Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{T+} V _{T-}	Hysteresis width	V _{CC} =4.75V			0.4		٧ .
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
Гон .	High-level output current	V _{CC} =4.75V, V _I =2V, V _I =0.8V, V _O =5.5V				100	μΑ
	Low lovel custous values	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
1	High level input austral	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
UН	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA ·
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.2	mA
Icc	Supply current	V _{CC} =5.25V (Not	e 1)		40	65	mΑ

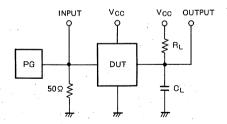
^{*:} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

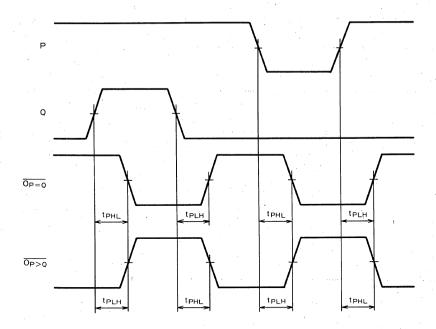
Symbol	Parameter	Test and distance	Limits			Unit
Joynnboi	Farameter	Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high level, high-to-low level output			23	45	
t _{PHL}	propagation time from inputs P to output OP=Q			20	35	ns
tpLH	Low-to-high level, high-to-low level output	1		21	45	
t _{PHL}	propagation time from inputs Q to output $\overline{O_{P=Q}}$	D =6670 0 45-5 (N : 0)		20	35	ns
tpLH	Low-to-high level, high-to-low level output	R_{\perp} =667Ω, C_{\perp} =45pF (Note 2) All other input pins in low-state		26	45	
t _{PHL}	propagation time from inputs P to output OP>Q	, and a super part of the supe		22	35	ns
t _{PLH}	Low-to-high level, high-to-low level output			28	45	
t PHL	propagation time from inputs Q to output $\overline{O}_{P>Q}$			26	35	ns

Note 1: ICC is measured with all inputs at value of 4.5V.

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_W = 500ns, V_P = 3 V_P , P_T = 50 Ω
- (2) C_L includes probe and jig capacitance.



MITSUBISHI LSTTLS M74LS688P

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

DESCRIPTION

The M74LS688P is a semiconductor integrated circuit containing two 8-bit words comparator functions with enable input.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input (E)
- Active pull-up output
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

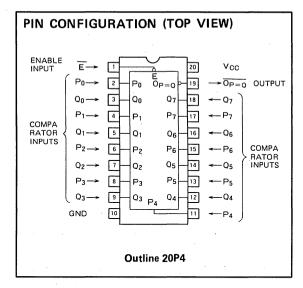
FUNCTIONAL DESCRIPTION

When enable input \overline{E} is low, two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at output $\overline{O_{P=0}}$.

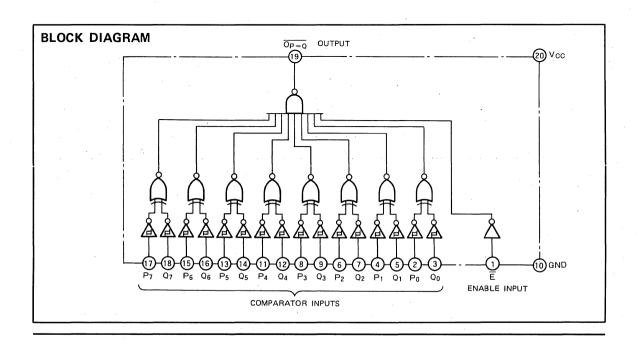
When E is high, $\overline{O_{P=Q}}$ is high in spite of $P_0 \sim P_7$ and $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	O _{P=0}	O _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

FUNCTION TABLE (Note 1)

P, Q	Ē	O _{P=Q}
P=Q	L	L
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
Х	Н	н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Sýmbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage	1	-0.5~+7	V
Vı	Input voltage		-0.5~+15	· V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	ొ
T _{stg}	Storage temperature range		−65∼+150	ဗ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

	Parameter					
Symbol	1DOI Farantetei	ieter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		400	μΑ
		V _{OL} ≤0.4V	0		12	, mA
IOL	Low-level output current V _{OL} ≤0.5V		. 0		24	mA-

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	D	Test conditions -		Limits			
Symbol	Parameter			Min	Typ *	Max	Unit
ViH	High-level input voltage		. 2			٧	
VIL	Low-level input voltage	1				0.8	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V		0.4		٧	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =			-1.5	V	
VoH	High-level output voltage	V _{CC} =4.75V, V ₁ =2V, V ₁	2.7			٧	
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	· V
VoL	Low-level output voltage	V ₁ =2V V ₁ =0.8V	I _{OL} =24mA		0.35	0.5	٧
	IP-h l- all and a second	V _{CC} =5.25V, V _I =	2.7V			. 20	μΑ
Iн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
, կլ	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.2	mA
los	Short-circuit output current	V _{CC} =5.25V, V _O =	-20		- 100	mA	
Loc	Supply current	V _{CC} =5.25V (Note:	2)		40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.

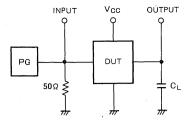
Note 2: ICC is measured with all other inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			11.4
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t pLH	Low-to-high level, high-to-low level output			12	23	
t PHL	propagation time from inputs P to output Op=Q			18	28	ns
t PLH	Low-to-high level, high-to-low level output	0 -45-5 (0 0)		11	23	
t PHL	propagation time from inputs Q to output Op=Q	C _L =45pF (Note 3) All other input pins in low-state		19	28	ns
t _{PLH}	Low-to-high level, high-to-low level output			10	18	
t PHL	propagation time from input \overline{E} to output $\overline{O_{P=Q}}$			16	20	ns

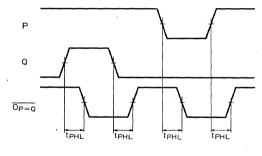
Note 3: Measurement circuit

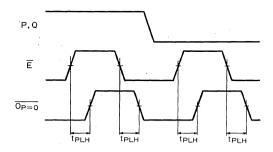


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P,P}, Z_O = 50Ω

 (2) C_L includes probe and jig capacitance.

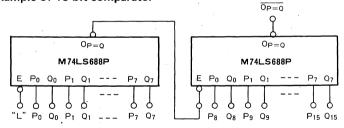
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Example of 16-bit comparator





MITSUBISHI LSTTLS

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS689P is a semiconductor integrated circuit containing two 8-bit words comparator functions with enable input and open collector output.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input (E)
- Open collector output
- Operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

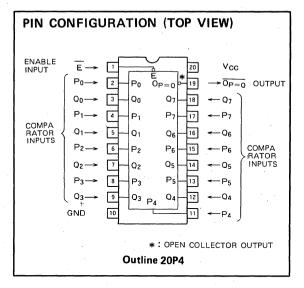
FUNCTIONAL DESCRIPTION

When enable input \overline{E} is low, two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at output $\overline{O_{P=0}}$.

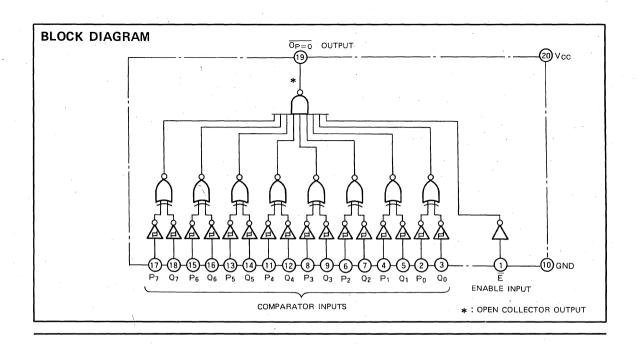
When E is high, $\overline{O_{P=Q}}$ is high in spite of $P_0 \sim P_7$ and $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application in M74LS688P.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	O _{P=Q}	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	Ņο	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	. Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	





8-RIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

P, Q	Ē	0 _{P=0}
P=Q	L	L
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	Н	Н

Note 1: 'X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V ₁	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	τ
T _{stg}	Storage temperature range		-65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Param			Limits		Unit
Sylfibol	Faran	neter	Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _O =5.5V	0		100	μΑ
	Low-level output current	V _{OL} ≦0.4V	0		12	mA
loL	2011 10101 001,001 00110111	V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			11-1-
		, lest c	l est conditions		Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{T+} V _{T-}	Hysteresis width	V _{CC} =4.75V	V _{CC} =4.75V		0.4		V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC}	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
Гон	High-level output current	$V_{CC} = 4.75V, V_1 = 2$	V _{CC} =4.75V, V _I =2V, V _I =0.8V, V _O =5.5V			100	μΑ
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =12mA		0.25	0.4	V
			I _{OL} =24mA		0.35	0.5	V
Чн	High-level input current	V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =2.7V			20	μΑ
		V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =10V			0.1	mA
lı∟	Low-level input current	V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =0.4V			-0.2	mΑ
Icc	Supply current	V _{CC} =5.25V (No	V _{CC} =5.25V (Note 2)		40	65	· mA

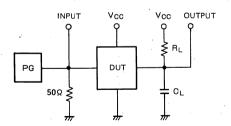
^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C. Note 2: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, Ta=25°C, unless otherwise noted)

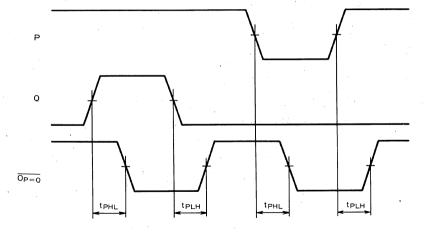
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	Unit
tpLH	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3) All other input pins in low-state.		23	40	ns
t PHL				21	35	
t plh	Low-to-high level, high-to-low level output propagation time from inputs Q to output Op=Q			23	40	ns
t PHL				21	35	
t pLH	Low-to-high level high-to-low level output propagation time from input E to output $\overline{O_{P=Q}}$			22	35	ns
t _{PHL}				20	30	

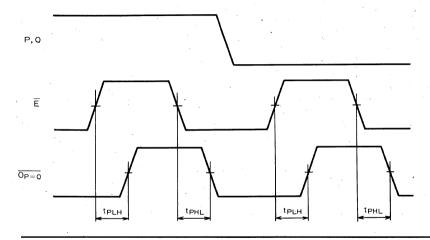
8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_W = 500ns, V_P = 3 V_P .P, Z_0 = 50 Ω
- (2) C_L includes probe and jig capacitance.





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